DATA SHEET

FB2040A
8-bit Futurebus+ transceiver

Product specification

1995 May 25

IC19 Data Handbook

Philips
Semiconductors

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8-bit Futurebus+ transceiver FB2040A

FEATURES

- 8-bit BTL transceivers
- Separate I/O on TTL A-port
- Inverting
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flat Pack

QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		4.4 3.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		3.4 3.2	ns
C_{OB}	Output capacitance ($\overline{B0}$ – $\overline{B7}$ only)		4	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{B7}$ only)		100	mA
I_{CC}	Supply current	Standby	4	mA
		AIn to $\overline{Bn}$ (outputs Low or High)	4	
		$\overline{Bn}$ to AOn (outputs Low)	22	
		$\overline{Bn}$ to AOn (outputs High)	12	

ORDERING INFORMATION

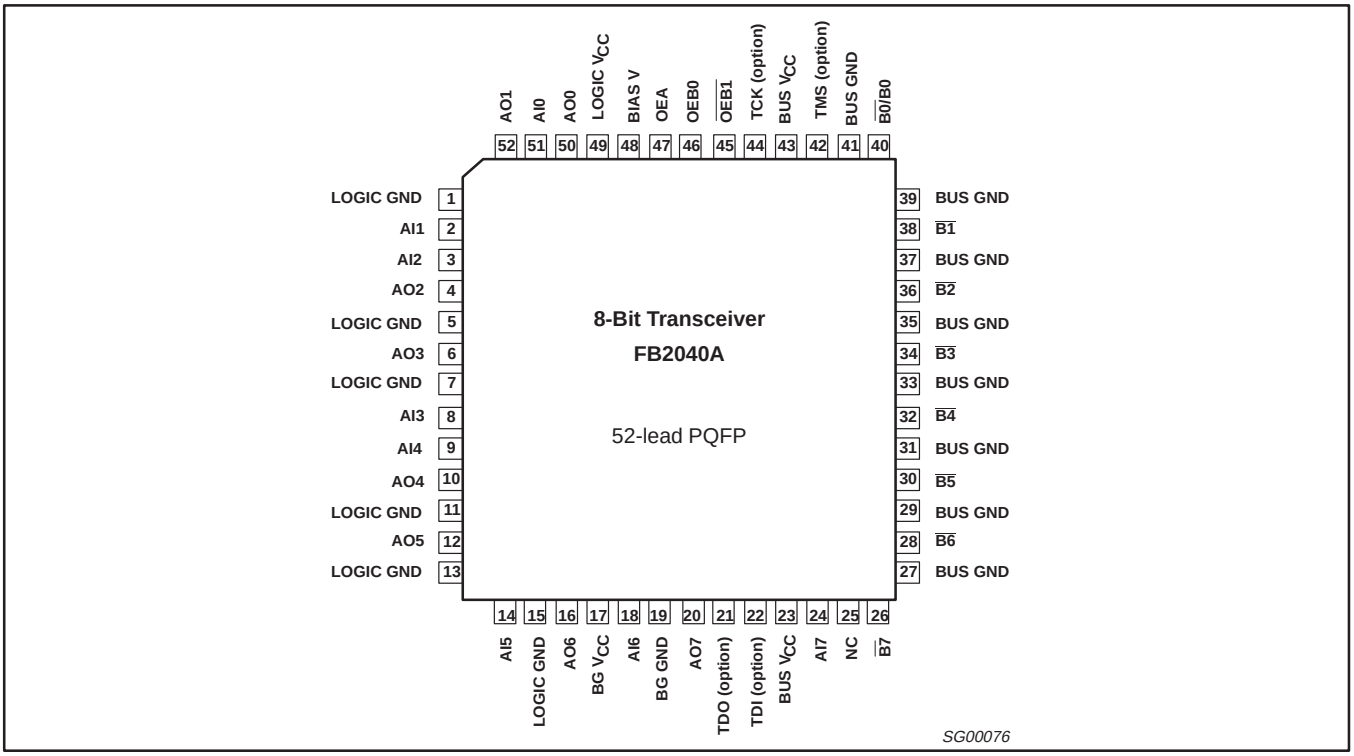
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2040BB	SOT379-1

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage	AI0 – AI7, OEB0, $\overline{OEB1}$, OEA	-1.2 to +7.0	V
		$\overline{B0}$ – $\overline{B7}$	-1.2 to +5.5	
I_{IN}	Input current		-18 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0 – A7	48	mA
		$\overline{B0}$ – $\overline{B7}$	200	
T_{amb}	Operating free-air temperature range		-40 to ++85	°C
T_{STG}	Storage temperature		-65 to +150	°C

PIN CONFIGURATION



DESCRIPTION

The FB2040A is an 8-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FB2040A is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to “Backplane Transceiver Logic” (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEA goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEA goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 2.5V.

The B-port has two output enables, OEB0 and $\overline{OEB1}$. When OEB0 is High and $\overline{OEB1}$ is Low the output is enabled. When OEB0 is Low or if $\overline{OEB1}$ is High, the B-port is inactive and is at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a “hard” signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

JTAG boundary scan pins are provided with signals TMS, TCK, TDI and TDO. TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally. Boundary scan functionality is not implemented at this time.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	51, 2, 3, 8, 9, 14, 18, 24	Input	Data inputs (TTL)
AO0 – AO7	50, 52, 4, 6, 10, 12, 16, 20	Output	3-state outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs. High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29, 27	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
BUS V_{CC}	23, 43	Power	Positive supply voltage
LOGIC V_{CC}	49	Power	Positive supply voltage
BG V_{CC}	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
BIAS V	48	Power	Live insertion pre-bias pin
TMS	42	Input	Test Mode Select (optional, if not implemented then no-connect)
TCK	44	Input	Test Clock (optional, if not implemented then no-connect)
TDI	22	Input	Test Data In (optional, if not implemented then shorted to TDO)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)
NC	25	NC	No Connect

FUNCTION TABLE

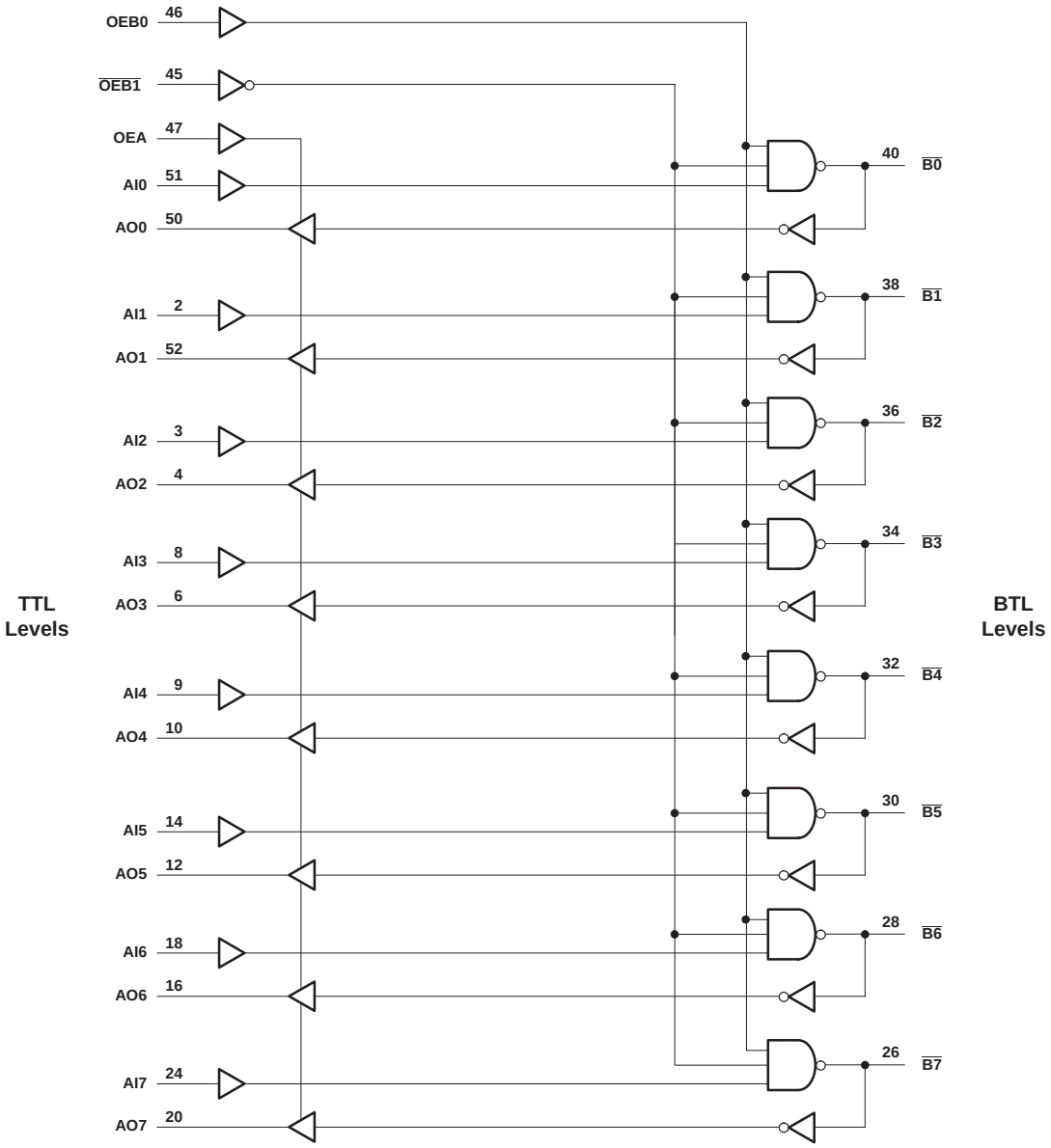
MODE	INPUTS					OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	AOn	$\overline{Bn}$*
AIn to $\overline{Bn}$	L	—	H	L	L	Z	H**
	H	—	H	L	L	Z	L
	L	—	H	L	H	L	H**
	H	—	H	L	H	H	L
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	H**
	X	X	X	H	X	X	H**
$\overline{Bn}$ to AOn	X	L	L	X	H	H	Input
	X	H	X	H	H	L	Input
	X	L	X	H	H	H	Input
	X	H	L	X	H	L	Input
Disable AOn outputs	—	X	X	X	L	Z	X

H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B7}$	2.0			V
		$\overline{B0}$ – $\overline{B7}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$–$\overline{B7}$			0.8	V
		$\overline{B0}$ – $\overline{B7}$			1.47	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO0 – AO7			-3	mA
I_{OL}	Low-level output current	AO0 – AO7			24	mA
		$\overline{B0}$ – $\overline{B7}$			100	
C_{OB}	Output capacitance on B port				5	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

LOGIC DIAGRAM FOR FB2040



NC = 25
LOGIC V_{CC} = 49
LOGIC GND = 1, 5, 7, 11, 13, 15
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48
BG V_{CC} = 17
BG GND = 19

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
V_{OH}	High-level output voltage	AO0 – AO7[3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5	2.85		V
V_{OL}	Low-level output voltage	AO0 – AO7[3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA		0.33	0.5	V
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 80mA	.75	1.0	1.10	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA			1.15	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-1.2	V
I_I	Input current at maximum input voltage	OEB0, $\overline{OEB1}$, OEA, AI0–AI7	V_{CC} = MAX, V_I = GND or 5.5V			±50	µA
I_{IH}	High-level input current	OEB0, $\overline{OEB1}$, OEA, AI0–AI7	V_{CC} = MAX, V_I = 2.7V			20	µA
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 2.1V			100	
I_{IL}	Low-level input current	OEB0, $\overline{OEB1}$, OEA, AI0–AI7	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 0.75V			-100	
I_{OZH}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O = 2.7V			50	µA
I_{OZL}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O = 0.5V			-50	µA
I_{OS}	Short-circuit output current[4]	AO0 – AO7 only	V_{CC} = MAX, V_O = 0.0V	-30		-150	mA
I_{CC}	Supply current (total)	I_{CCZ} (standby)	V_{CC} = MAX		19	30	mA
		I_{CCB}, AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		40	60	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		22	35	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		19	35	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

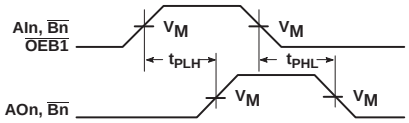
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	1.8 1.6	3.4 3.2	5.0 4.9	1.6 1.6	5.6 5.3	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 4, 5	1.0 1.0		5.0 5.0	1.5 1.5	5.5 5.5	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 4, 5	1.5 1.5	3.3 3.3	4.8 5.4	1.2 1.3	5.0 5.9	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	1.5 1.5	2.2 2.4	3.5 3.5	1.0 1.0	4.5 4.5	ns
$t_{SK}(o)$	Output skew between receivers in same package[1]	Waveform 3		0.4	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**B PORT LIMITS**					**UNIT**
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 9Ω		
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	2.9 1.6	4.4 3.3	5.0 4.8	2.3 1.5	5.5 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	2.9 1.9	4.7 3.5	5.9 5.1	2.6 1.8	7.8 5.7	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	3.0 1.7	5.3 3.2	6.3 4.8	2.7 1.5	8.0 5.7	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.4 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK}(o)$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	R_U = 16.5Ω			R_U = 16.5Ω		**UNIT**
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.0 1.7	4.5 3.3	6.4 4.8	2.3 1.6	6.9 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	3.0 2.0	4.8 3.5	6.0 5.2	2.7 1.9	7.9 5.7	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	3.1 1.8	5.4 3.3	6.4 4.9	2.8 1.6	8.1 5.7	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.5 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK}(o)$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns

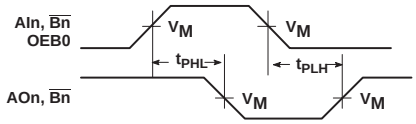
NOTES:

1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

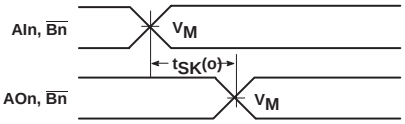
AC WAVEFORMS



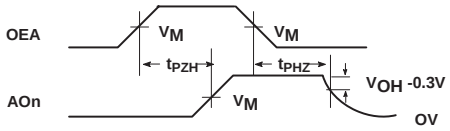
Waveform 1. Propagation Delay for Data or Output Enable to Output



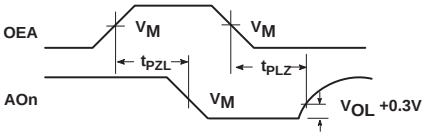
Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

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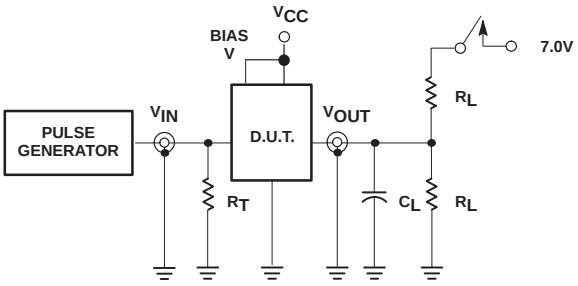
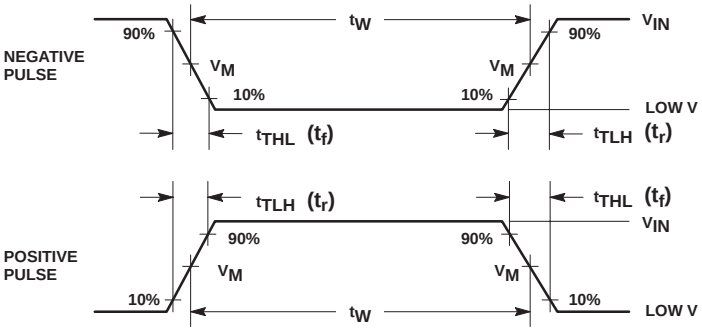
TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



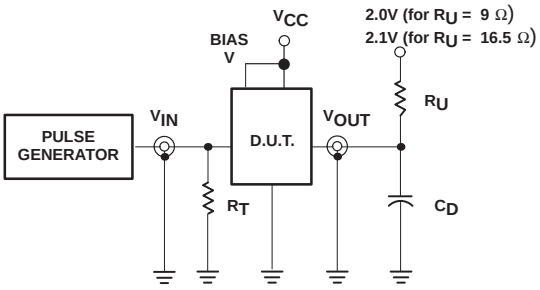
V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL} All other	closed open

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit for Outputs on B Port

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

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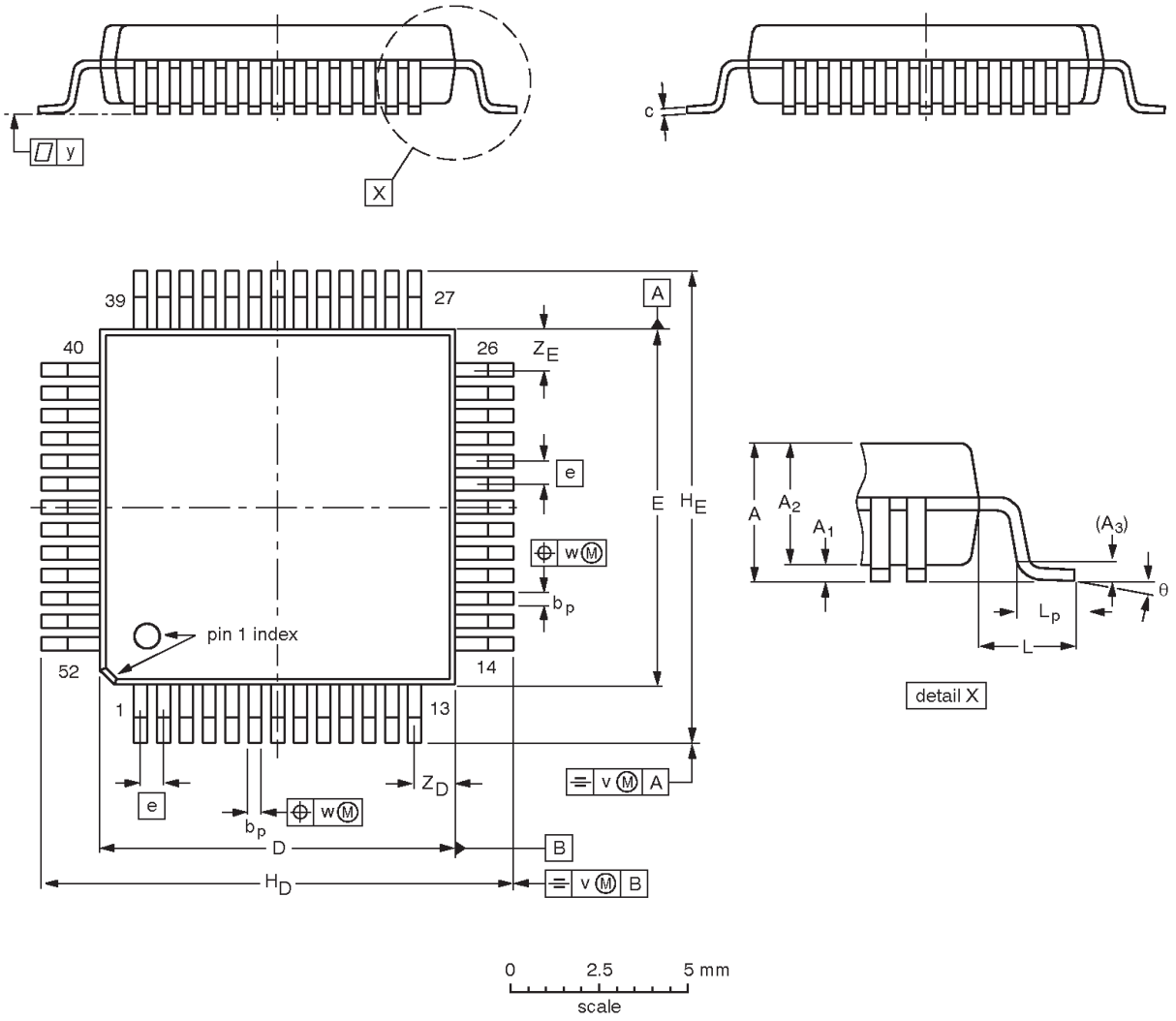
QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm SOT379-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT379-1		MO-108				~~95-02-04~~ 97-08-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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