# DATA SHEET

# SAA5246A

# Integrated VIP and Teletext (IVT1.0)

Product specification
Supersedes data of August 1992
File under Integrated Circuits, IC02

January 1993

**Philips**
**Semiconductors**

**PHILIPS**

# Integrated VIP and Teletext (IVT1.0)

# SAA5246A

## FEATURES

- Complete Teletext decoder in a 48-pin DIL or 64-pin QFP, integrated circuit
- Single +5 V power supply
- Both video and scan related synchronization modes are supported
- RGB interface to standard colour decoder ICs, push-pull output drive
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Data capture performance similar to SAA5231 (VIP2)
- Option for up to seven national languages
- Optional storage of packet 24 in the display memory
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic $\overline{ODD}$/EVEN output control with override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display.

## DESCRIPTION

The SAA5246A is a single-chip teletext decoder IC for decoding 625 line base World System Teletext transmissions. The teletext decoder hardware is based on the Enhanced Computer Controlled ECCT device (SAA5243) with some additional features.

The Video Input Processor section of the device uses mixed analog and digital designs in the data slicer and clock phase-locked-loop functions. As a result the number of external components are greatly reduced and no critical or adjustable components are required.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|--------|-----------|------|------|------|------|
| $V_{DD}$ | positive supply voltage | 4.5 | 5.0 | 5.5 | V |
| $I_{DD}$ | supply current | – | 64 | 128 | mA |
| $V_{syn}$ | sync amplitude | 0.1 | 0.3 | 0.6 | V |
| $V_{vid}$ | video amplitude | 0.7 | 1.0 | 1.4 | V |
| $f_{XTAL}$ | crystal frequency | – | 27 | – | MHz |
| $T_{amb}$ | operating ambient temperature | –20 | – | +70 | °C |

## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| SAA5246AP | 48 | DIL | plastic | SOT240AC3[1] |
| SAA5246AGP | 64 | QFP | plastic | SOT319DA3[2] |

### Notes

1. SOT240-1; 1996 November 22.
2. SOT319-3; 1996 November 22.

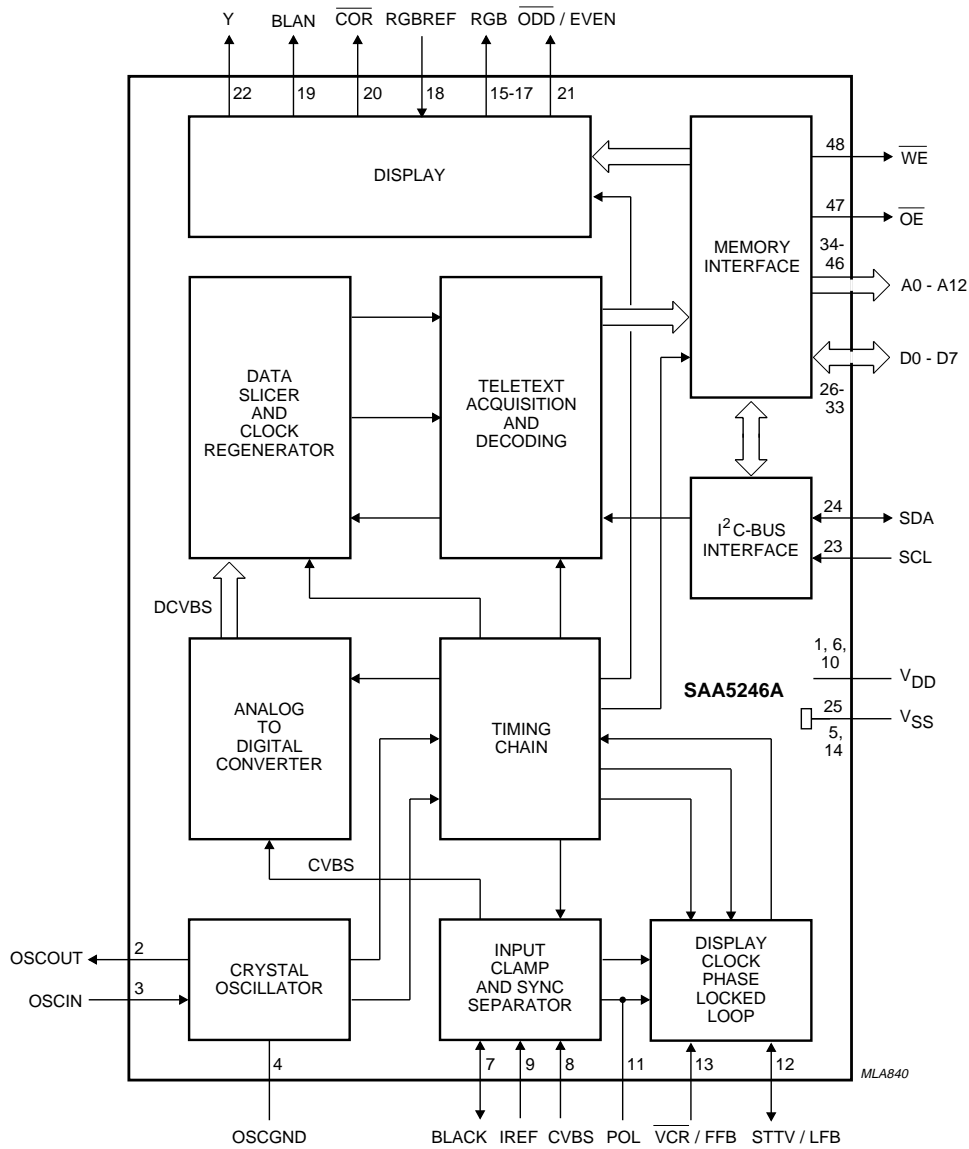# Integrated VIP and Teletext (IVT1.0)                     SAA5246A



Fig.1  Block diagram for SOT240 (DIL48) package.

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**PINNING**

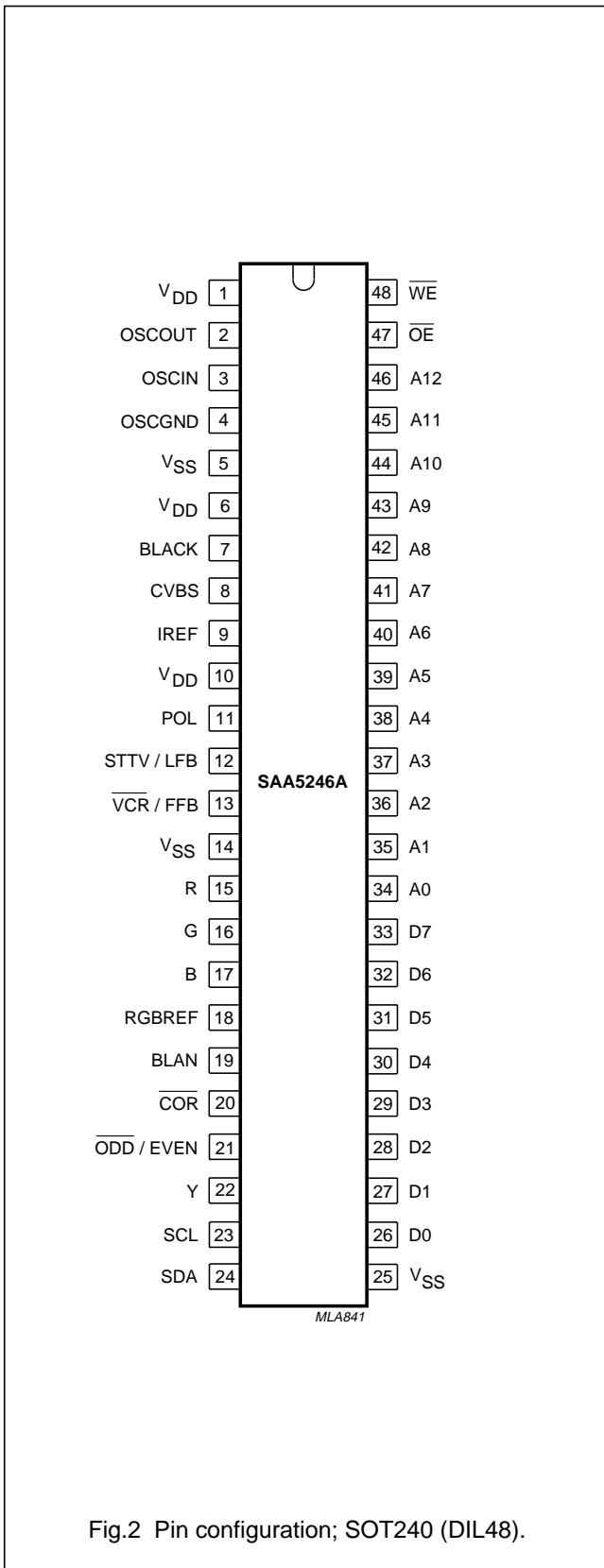| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | SOT240 | SOT319 | |
| OSCOUT | 2 | 27 | 27 MHz crystal oscillator output |
| OSCIN | 3 | 28 | 27 MHz crystal oscillator input |
| OSCGND | 4 | 29 | 0 V crystal oscillator ground |
| $V_{SS}$ | 5, 14, 25 | 26, 30, 31, 43, 58 | 0 V ground |
| BLACK | 7 | 35 | video black level storage pin, connected to ground via a 100 nF capacitor |
| CVBS | 8 | 36 | composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor |
| IREF | 9 | 37 | reference current input pin, connected to ground via a 27 kΩ resistor |
| $V_{DD}$ | 1, 6, 10 | 25, 32, 38 | +5 V positive supply |
| POL | 11 | 39 | STTV/LFB/FFB polarity selection pin |
| STTV/LFB | 12 | 40 | sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode) |
| $\overline{VCR}$/FFB | 13 | 42 | PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode) |
| R | 15 | 44 | dot rate character output of the RED colour information |
| G | 16 | 45 | dot rate character output of the GREEN colour information |
| B | 17 | 47 | dot rate character output of the BLUE colour information |
| RGBREF | 18 | 48 | input DC voltage to define the output high level on the RGB pins |
| BLAN | 19 | 52 | dot rate fast blanking output |
| $\overline{COR}$ | 20 | 53 | programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output |
| $\overline{ODD}$/EVEN | 21 | 54 | a 25 Hz output synchronized to the input CVBS field sync pulses to make a non-interlaced display by adjustment of the vertical deflection currents. |
| Y | 22 | 55 | dot rate character output of teletext foreground colour information. Open-drain output |
| SCL | 23 | 56 | serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device |
| SDA | 24 | 57 | serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device |
| D0-D5 | 26-31 | 60-64, 3 | data ports for the page SRAM |
| n.c. | – | 1, 2, 10, 11, 15, 18, 33, 34, 41, 46, 49 - 51, 59 | not connected |
| D6-D7 | 32, 33 | 4, 5 | data ports for the page SRAM |

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| SYMBOL | PIN | | DESCRIPTION |
|--------|--------|--------|-------------|
| | SOT240 | SOT319 | |
| A0-A12 | 34-46 | 6-9, 12-14, 16, 17, 19-22 | address output for the page SRAM |
| $\overline{OE}$ | 47 | 23 | output enable for the page SRAM |
| $\overline{WE}$ | 48 | 24 | write enable for the page SRAM |

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| Pin | Signal | | Pin | Signal |
|-----|--------|---|-----|--------|
| 1 | $V_{DD}$ | | 48 | $\overline{WE}$ |
| 2 | OSCOUT | | 47 | $\overline{OE}$ |
| 3 | OSCIN | | 46 | A12 |
| 4 | OSCGND | | 45 | A11 |
| 5 | $V_{SS}$ | | 44 | A10 |
| 6 | $V_{DD}$ | | 43 | A9 |
| 7 | BLACK | | 42 | A8 |
| 8 | CVBS | | 41 | A7 |
| 9 | IREF | | 40 | A6 |
| 10 | $V_{DD}$ | | 39 | A5 |
| 11 | POL | | 38 | A4 |
| 12 | STTV / LFB | | 37 | A3 |
| 13 | $\overline{VCR}$ / FFB | | 36 | A2 |
| 14 | $V_{SS}$ | | 35 | A1 |
| 15 | R | | 34 | A0 |
| 16 | G | | 33 | D7 |
| 17 | B | | 32 | D6 |
| 18 | RGBREF | | 31 | D5 |
| 19 | BLAN | | 30 | D4 |
| 20 | $\overline{COR}$ | | 29 | D3 |
| 21 | $\overline{ODD}$ / EVEN | | 28 | D2 |
| 22 | Y | | 27 | D1 |
| 23 | SCL | | 26 | D0 |
| 24 | SDA | | 25 | $V_{SS}$ |

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Fig.2  Pin configuration; SOT240 (DIL48).

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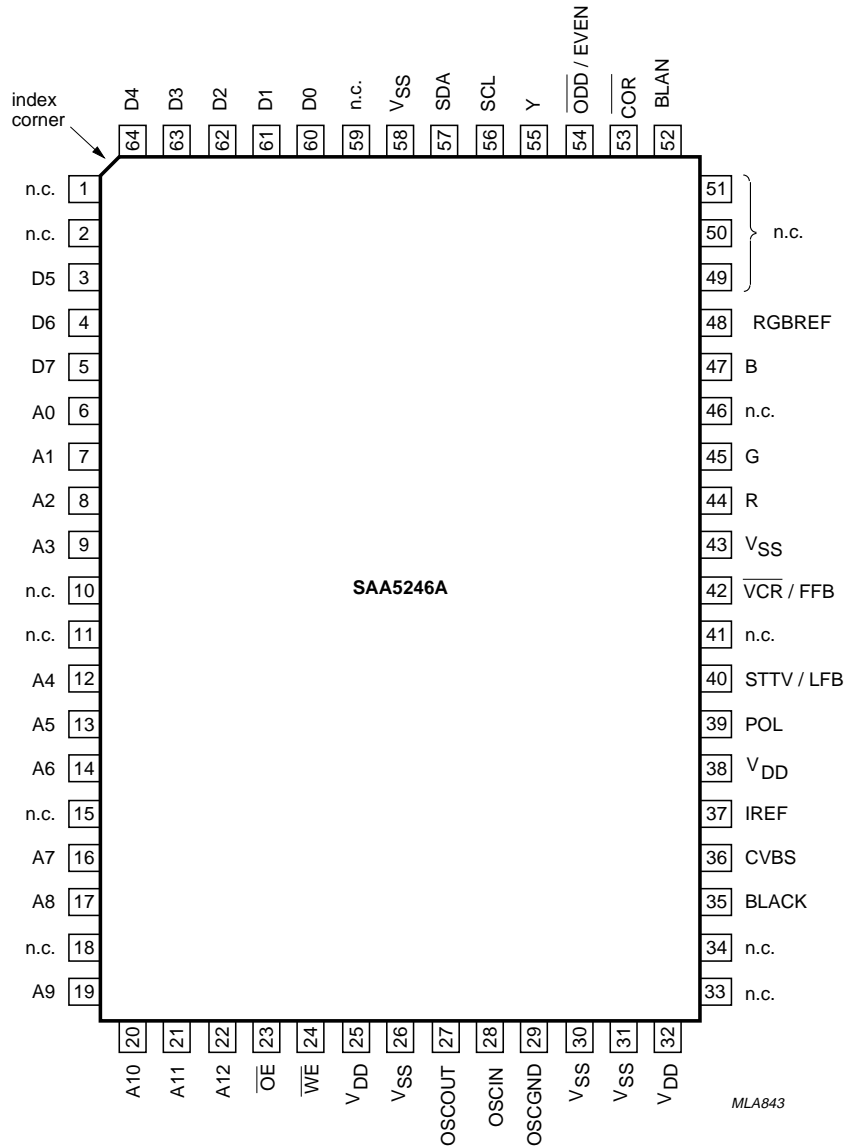
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Fig.3  Pin configuration; SOT319 (QFP64).

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## LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | supply voltage (all supplies) | −0.3 | 6.5 | V |
| $V_I$ | input voltage (any input) | −0.3 | $V_{DD}$ +0.5 | V |
| $V_O$ | output voltage (any output) | −0.3 | $V_{DD}$ +0.5 | V |
| $I_O$ | output current (each output) | − | ±10 | mA |
| $I_{IOK}$ | DC input or output diode current | − | ±20 | mA |
| $T_{amb}$ | operating ambient temperature | −20 | +70 | °C |
| $T_{stg}$ | storage temperature | −55 | +125 | °C |
| $V_{stat}$ | electrostatic handling (see note 1) | −2000 | +2000 | V |

**Note to the Limiting values**

1. Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

**Failure Rate**

The failure rate at $T_{amb}$ = 55 °C will be a maximum of 1000 FITS (1 FIT = $1 \times 10^{-9}$ failures per hour).

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### CHARACTERISTICS

$V_{DD}$ = 5 V $\pm$ 10%; $T_{amb}$ = $-20$ to +70 $^\circ$C, unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------|-----------|------------|------|------|------|------|
| **Supplies** | | | | | | |
| $V_{DD}$ | supply voltage range | | 4.5 | 5.0 | 5.5 | V |
| $I_{DD}$ | total supply current | | – | 64 | 128 | mA |
| **Inputs** | | | | | | |
| CVBS | | | | | | |
| $V_{syn}$ | sync amplitude | | 0.1 | 0.3 | 0.6 | V |
| $t_{syn}$ | delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge) | | $-150$ | 0 | +150 | ns |
| $t_{syd}$ | change in sync delay between all black and all white video input at nominal levels | | 0 | – | 25 | ns |
| $V_{vid(p-p)}$ | video input amplitude (peak-to-peak) | | 0.7 | 1.0 | 1.4 | V |
| | display PLL catching range | | $\pm$7 | – | – | % |
| $Z_{src}$ | source impedance | | – | – | 250 | $\Omega$ |
| $C_I$ | input capacitance | | – | – | 10 | pF |
| IREF | | | | | | |
| $R_g$ | resistor to ground | | – | 27 | – | k$\Omega$ |
| POL | | | | | | |
| $V_{IL}$ | LOW level input voltage | | $-0.3$ | – | +0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{DD}$+0.5 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 0 to $V_{DD}$ | $-10$ | – | +10 | $\mu$A |
| $C_I$ | input capacitance | | – | – | 10 | pF |
| LFB | | | | | | |
| $V_{IL}$ | LOW level input voltage | | $-0.3$ | – | +0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{DD}$+0.5 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 0 to $V_{DD}$ | $-10$ | – | +10 | $\mu$A |
| $I_I$ | input current | note 1 | $-1$ | – | +1 | mA |
| $t_{LFB}$ | delay between LFB front edge and input video line sync | | – | 250 | – | ns |
| $\overline{VCR}$/FFB | | | | | | |
| $V_{IL}$ | LOW level input voltage | | $-0.3$ | – | +0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{DD}$+0.5 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 0 to $V_{DD}$ | $-10$ | – | +10 | $\mu$A |
| $I_I$ | input current | note 1 | $-1$ | – | +1 | mA |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| RGBREF | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.3 | – | $V_{DD}$+0.5 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 0 to $V_{DD}$ | −10 | – | +10 | μA |
| $I_{DC}$ | DC current | | – | – | 10 | mA |
| SCL | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.3 | – | +1.5 | V |
| $V_{IH}$ | HIGH level input voltage | | 3.0 | – | $V_{DD}$+0.5 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 0 to $V_{DD}$ | −10 | – | +10 | μA |
| $f_{SCL}$ | clock frequency | | 0 | – | 100 | kHz |
| $t_r$ | input rise time | 10% to 90% | – | – | 2 | μs |
| $t_f$ | input fall time | 90% to 10% | – | – | 2 | μs |
| $C_I$ | input capacitance | | – | – | 10 | pF |
| **Inputs/outputs** | | | | | | |
| CRYSTAL OSCILLATOR (OSCIN; OSCOUT) | | | | | | |
| $f_{XTAL}$ | crystal frequency | | – | 27 | – | MHz |
| $V_{OSC}$ | oscillation amplitude (peak-to-peak value) | | – | 1.5 | – | V |
| $G_v$ | small signal voltage gain | | – | 1 | – | V/V |
| $G_m$ | mutual conductance | | 5 | – | – | mA/V |
| $C_I$ | input capacitance | | – | – | 10 | pF |
| $C_{FB}$ | feedback capacitance | | – | 1 | – | pF |
| BLACK | | | | | | |
| $C_{blk}$ | storage capacitor to ground | | – | 100 | – | nF |
| $I_{LI}$ | input leakage current | $V_I$ = 0 to $V_{DD}$ | −10 | – | +10 | μA |
| SDA | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.3 | – | +1.5 | V |
| $V_{IH}$ | HIGH level input voltage | | 3.0 | – | $V_{DD}$+0.5 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 0 to $V_{DD}$ | −10 | – | +10 | μA |
| $C_I$ | input capacitance | | – | – | 10 | pF |
| $t_r$ | input rise time | 10% to 90% | – | – | 2 | μs |
| $t_f$ | input fall time | 90% to 10% | – | – | 2 | μs |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = 3 mA | 0 | – | 0.5 | V |
| $t_f$ | output fall time | 3 V to 1 V | – | – | 200 | ns |
| $C_L$ | load capacitance | | – | – | 400 | pF |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| D0 TO D7 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.3 | – | +0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{DD}$+0.5 | V |
| $I_{LI}$ | input leakage current | | −10 | – | +10 | μA |
| $C_I$ | input capacitance | | – | – | 10 | pF |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = +1.6 mA | 0 | – | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OH}$ = −0.2 mA | 2.4 | – | $V_{DD}$ | V |
| $t_r$ | output rise time | 0.6 V to 2.2 V | – | – | 50 | ns |
| $t_f$ | output fall time | 2.2 V to 0.6 V | – | – | 50 | ns |
| $C_L$ | load capacitance | | – | – | 120 | pF |
| **Outputs** | | | | | | |
| STTV | | | | | | |
| $G_{stt}$ | gain of STTV relative to video input | | 0.9 | 1.0 | 1.1 | |
| $V_{tcs}$ | TCS amplitude | | 0.2 | 0.3 | 0.45 | V |
| $V_{DCs}$ | DC shift between TCS output and nominal video output | | – | – | 0.15 | V |
| $I_O$ | output drive current | | – | – | 3.0 | mA |
| $C_L$ | load capacitance | | – | – | 100 | pF |
| A0 TO A12 ADDRESS OUTPUT TO MEMORY | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = +1.6 mA | 0 | – | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OH}$ = −0.2 mA | 2.4 | – | $V_{DD}$ | V |
| $C_L$ | load capacitance | | – | – | 120 | pF |
| $t_r$ | output rise time | 0.6 V to 2.2 V | – | – | 50 | ns |
| $t_f$ | output fall time | 2.2 V to 0.6 V | – | – | 50 | ns |
| $\overline{OE}$, $\overline{WE}$ | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = +1.6 mA | 0 | – | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OH}$ = −0.2 mA | 2.4 | – | $V_{DD}$ | V |
| $C_L$ | load capacitance | | – | – | 120 | pF |
| $t_r$ | output rise time | 0.6 V to 2.2 V | – | – | 50 | ns |
| $t_f$ | output fall time | 2.2 V to 0.6 V | – | – | 50 | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| R, G AND B | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = 2 mA | 0 | – | 0.2 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OH}$ = −1.6 mA; RGBREF ≤ $V_{DD}$−2 V; note 2 | RGBREF −0.25 V | RGBREF | RGBREF +0.25 V | V |
| $I_{DC}$ | DC current | | – | – | −3.3 | mA |
| $|Z_o|$ | output impedance | | – | – | 200 | Ω |
| $C_L$ | load capacitance | | – | – | 50 | pF |
| $t_r$ | output rise time | 10% to 90% | – | – | 20 | ns |
| $t_f$ | output fall time | 90% to 10% | – | – | 20 | ns |
| BLAN | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = 0.2 mA | 0 | – | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OH}$ = −0.2 mA; $V_{DD}$ = 4.5 V; note 2 | 1.1 | – | – | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OH}$ = 0 mA; $V_{DD}$ = 5.5 V; note 2 | – | – | 2.8 | V |
| $C_L$ | load capacitance | | – | – | 50 | pF |
| $t_r$ | output rise time | 10% to 90% | – | – | 20 | ns |
| $t_f$ | output fall time | 90% to 10% | – | – | 20 | ns |
| $\overline{ODD}$/EVEN | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = +1.6 mA | 0 | – | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{OH}$ = −1.6 mA | $V_{DD}$−0.4 | – | $V_{DD}$ | V |
| $C_L$ | load capacitance | | – | – | 120 | pF |
| $t_r$ | output rise time | 0.6 to 2.2 V | – | – | 50 | ns |
| $t_f$ | output fall time | 2.2 to 0.6 V | – | – | 50 | ns |
| $\overline{COR}$ AND Y (OPEN DRAIN) | | | | | | |
| $V_{OH}$ | pull-up voltage at pin | | – | – | $V_{DD}$ | V |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = +2 mA | 0 | – | 0.4 | V |
| $V_{OL}$ | LOW level output voltage | $I_{OL}$ = +5 mA | 0 | – | 1.0 | V |
| $C_L$ | load capacitance | | – | – | 25 | pF |
| $t_f$ | output fall time | load resistor of 1.2 kΩ to $V_{DD}$; measured between $V_{DD}$ −0.5 and 1.5 V | – | – | 50 | ns |
| $I_{LO}$ | output leakage current | $V_I$ = 0 to $V_{DD}$ | −10 | – | +10 | μA |
| $T_{SK}$ | skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN | | – | – | 20 | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Timing** | | | | | | |
| MEMORY INTERFACE | | | | | | |
| $t_{CY}$ | cycle time | | – | 500 | – | ns |
| $t_{OE}$ | address change to $\overline{OE}$ LOW | | 55 | – | – | ns |
| $t_{ADDR}$ | address active time | | 450 | 500 | – | ns |
| $t_{rOEW}$ | $\overline{OE}$ pulse width read | | 295 | – | – | ns |
| $t_{wOEW}$ | $\overline{OE}$ pulse width write | | 100 | – | – | ns |
| $t_{ACC}$ | access time from address data valid | | – | – | 150 | ns |
| $t_{DH}$ | data hold time from $\overline{OE}$ HIGH or address change | | 0 | – | 150 | ns |
| $t_{WEW}$ | $\overline{WE}$ pulse width | | 100 | – | – | ns |
| $t_{DS}$ | data set-up time to $\overline{WE}$ HIGH | | 60 | – | – | ns |
| $t_{DHWE}$ | data hold time from $\overline{WE}$ HIGH | | 20 | – | – | ns |
| $t_{WR}$ | write recovery time | | 20 | – | – | ns |
| $t_{DE}$ | data enable from $\overline{WE}$ LOW | | 60 | – | – | ns |
| I²C-BUS | | | | | | |
| $t_{LOW}$ | clock LOW period | | 4 | – | – | µs |
| $t_{HIGH}$ | clock HIGH period | | 4 | – | – | µs |
| $t_{SU;DAT}$ | data set-up time | | 250 | – | – | ns |
| $t_{HD;DAT}$ | data hold time | | 170 | – | – | ns |
| $t_{SU;STO}$ | set-up time from clock HIGH to STOP | | 4 | – | – | µs |
| $t_{BUF}$ | START set-up time following a STOP | | 4 | – | – | µs |
| $t_{HD;STA}$ | START hold time | | 4 | – | – | µs |
| $t_{SU;STA}$ | START set-up time following clock LOW-to-HIGH transition | | 4 | – | – | µs |

**Notes to the characteristics**

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.

2. Can be pulled higher by external pull-up resistor, (maximum leakage current ≈ 200 µA).

Fig.4 Composite sync waveforms.
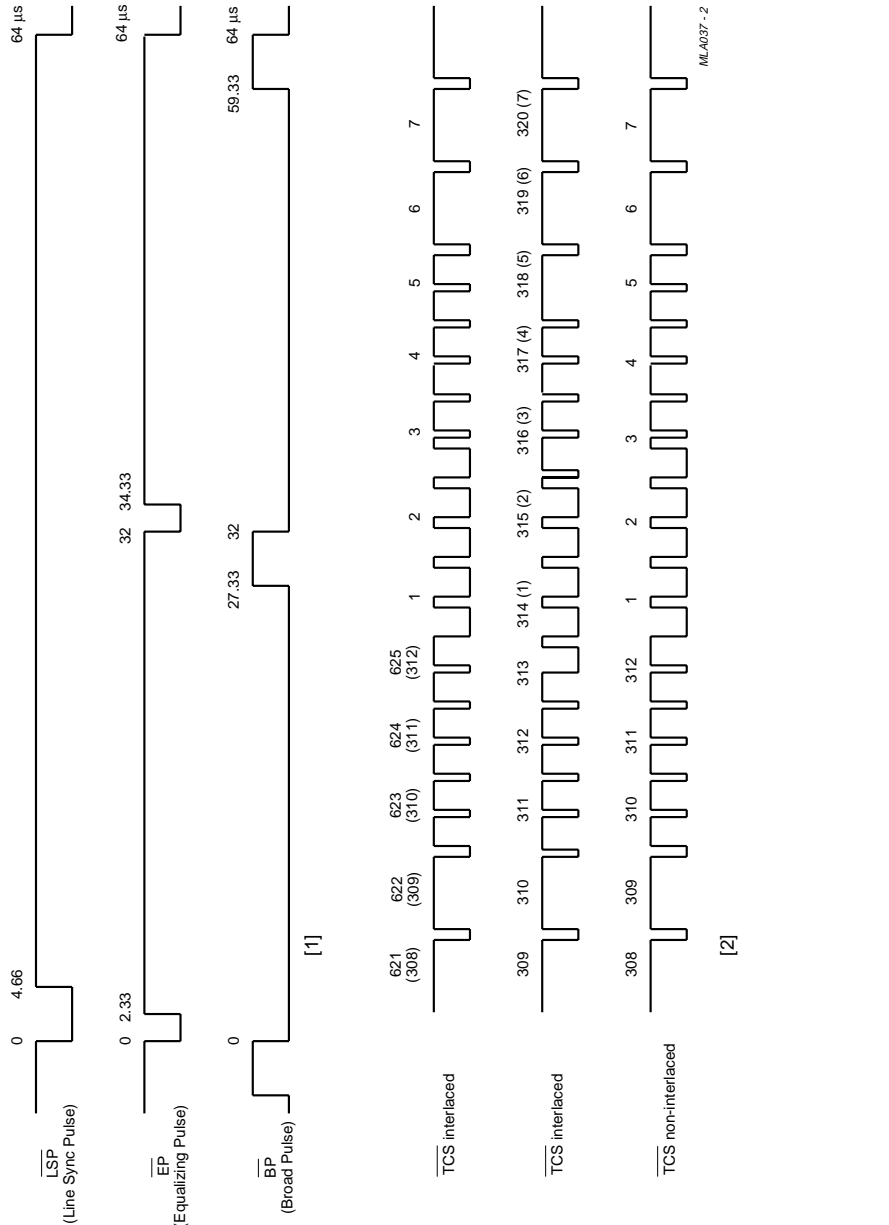
TCS is available on STTV/LFB pin.

[1] LSP, EP and BP are combined to give TCS as shown below. All timings measured from falling edge of LSP.

[2] Line numbers placed in the middle of the line. Equivalent count numbers in brackets.
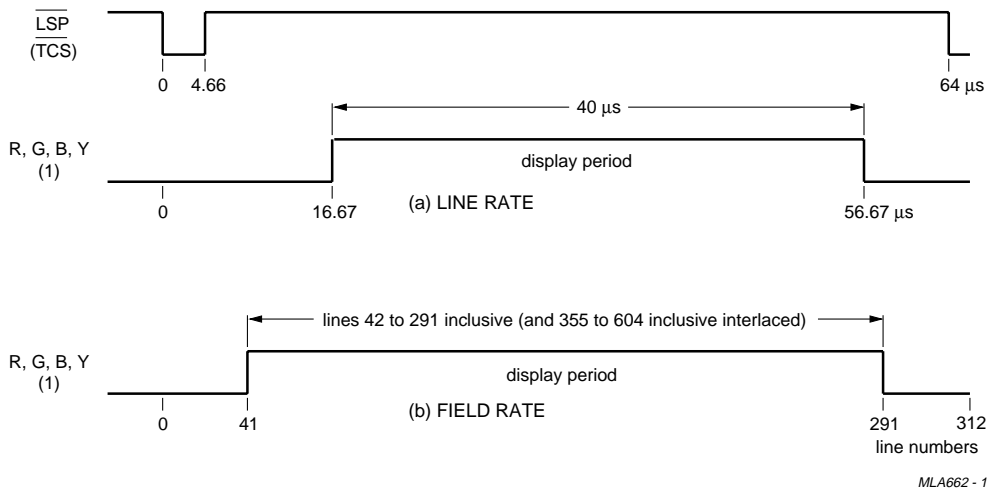
(1) also BLAN in character and box blanking

Fig.5  Display output timing (a) line rate (b) field rate.
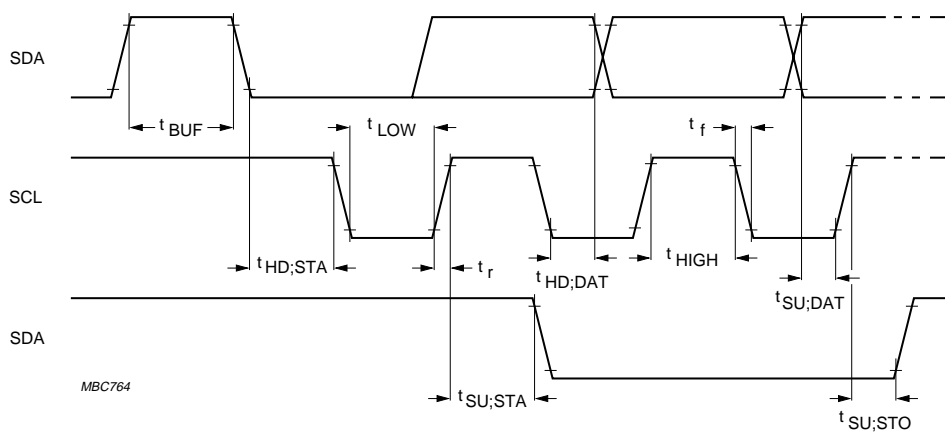


Fig.6  I²C-bus timing.

Fig.7 ODD/EVEN timing.
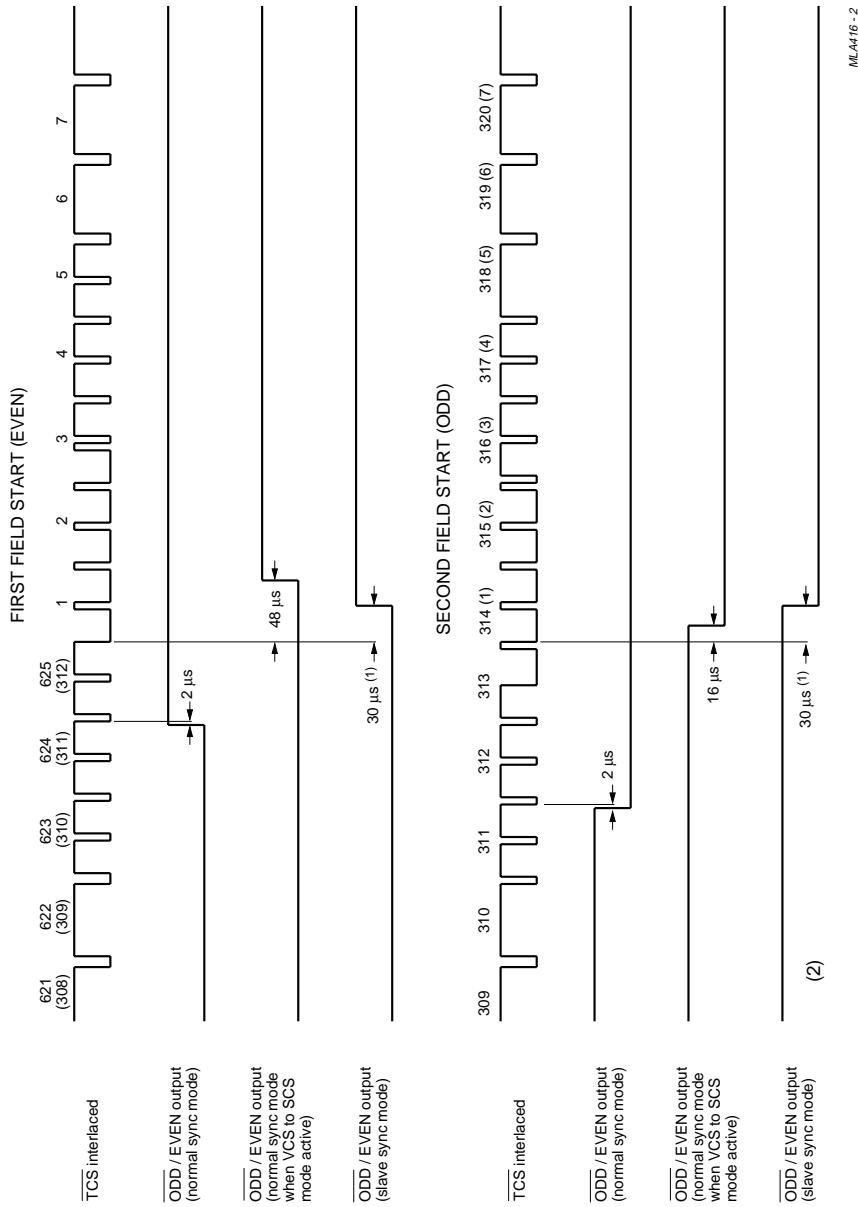
(1) or 62 µs if R1 D2.D1.D0 = 111.
(2) Line numbers placed in the middle of the line. Equivalent count numbers in brackets.

Fig.8 Memory interface timing (a) read (b) write.
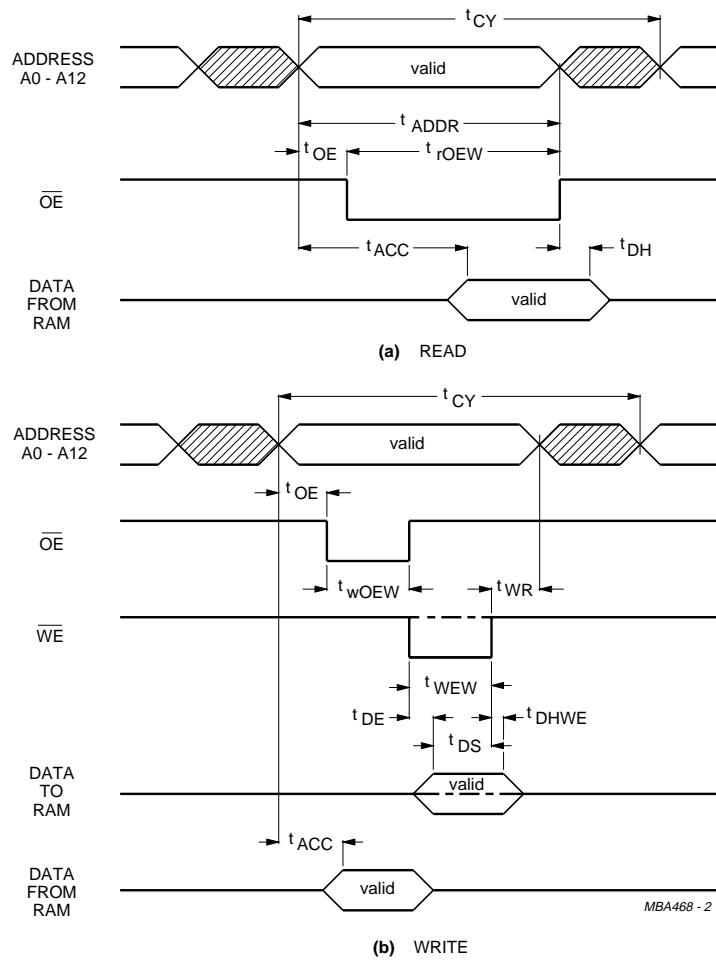
_ _ _ _ Level during flicker stopped cycle.

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**APPLICATION INFORMATION**



(1) Value dependent on application

Fig.9 Application diagram (SOT240).
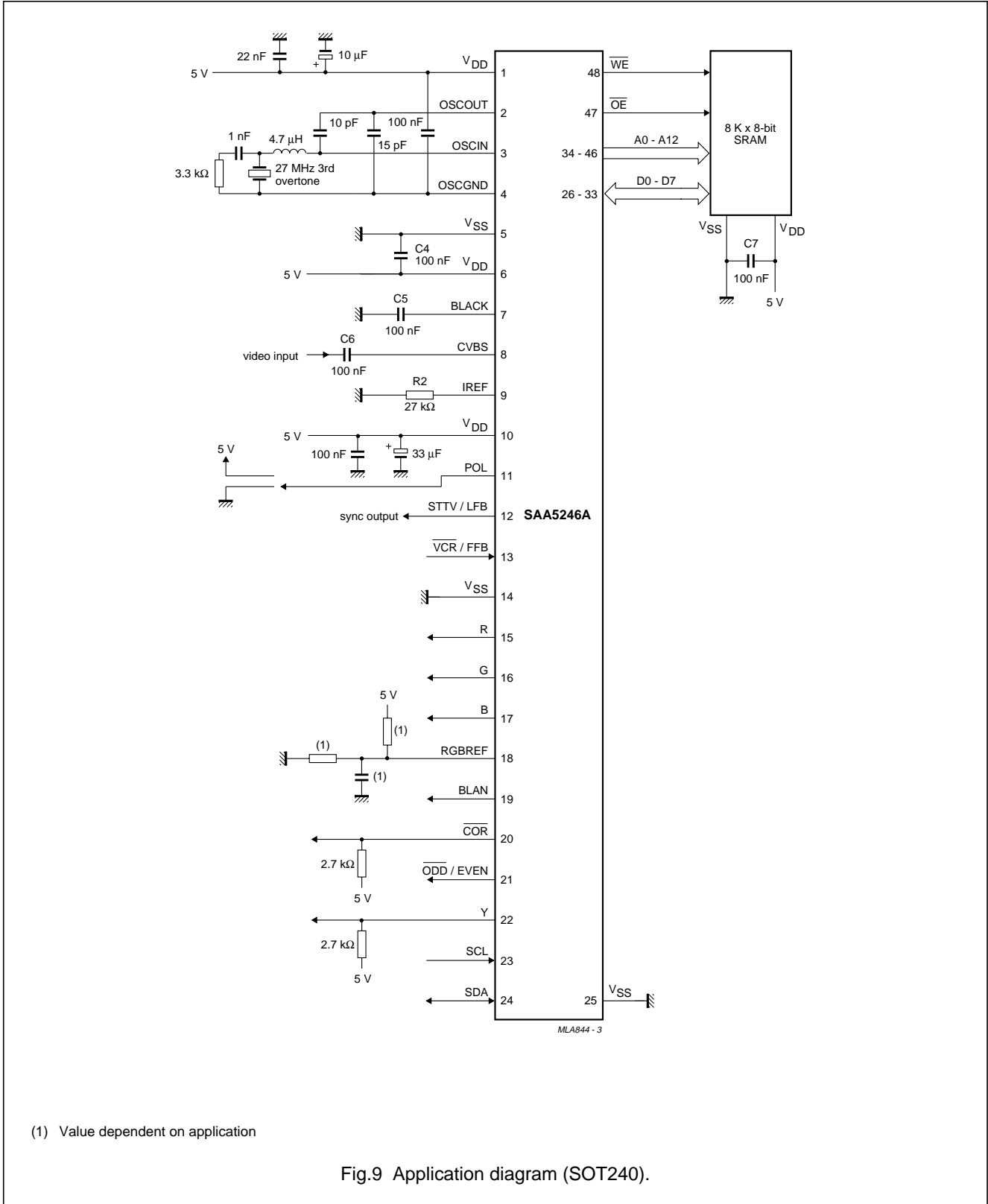
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**SAA5246A page memory organization**

The organization of the page memory is illustrated by Fig.10. The SAA5246A provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.
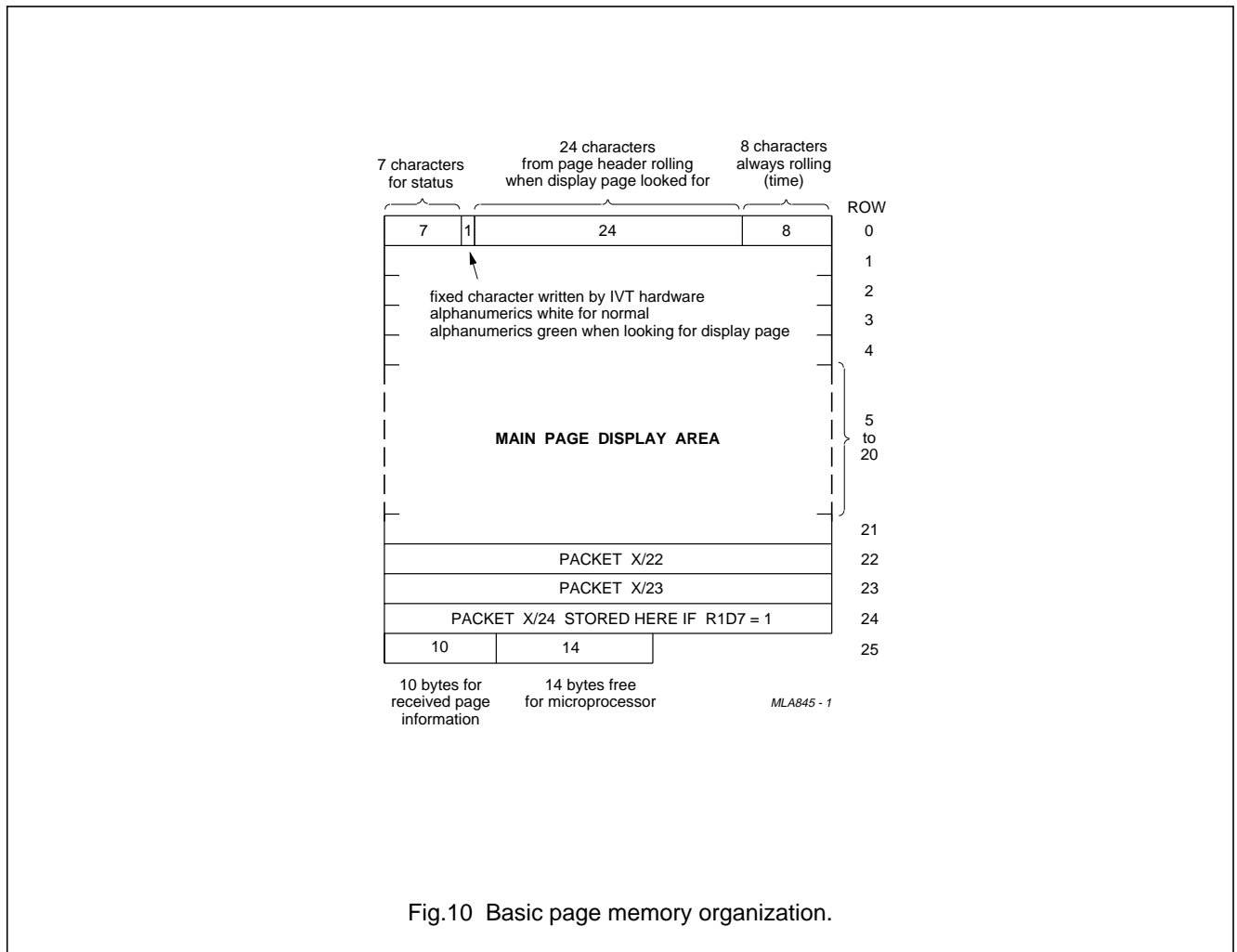


Fig.10 Basic page memory organization.

**Note to Fig.10**

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5246A to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microprocessor.

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**Table 1** Row 25 received control data format.

| D0 | PU0 | PT0 | MU0 | MT0 | HU0 | HT0 | C7 | C11 | MAG0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| D1 | PU1 | PT1 | MU1 | MT1 | HU1 | HT1 | C8 | C12 | MAG1 | 0 |
| D2 | PU2 | PT2 | MU2 | MT2 | HU2 | C5 | C9 | C13 | MAG2 | 0 |
| D3 | PU3 | PT3 | MU3 | C4 | HU3 | C6 | C10 | C14 | 0 | 0 |
| D4 | HAM.ER | HAM.ER | HAM.ER | HAM.ER | HAM.ER | HAM.ER | HAM.ER | HAM.ER | $\overline{FOUND}$ | 0 |
| D5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PBLF |
| D6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | |
| Column | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

**Where:**

Page number

| MAG | magazine |
|---|---|
| PU | page units |
| PT | page tens |
| PBLF | page being looked for |
| $\overline{FOUND}$ | LOW for page has been found |
| HAM.ER | Hamming error in corresponding byte |

Page sub-code

| MU | minutes units |
|---|---|
| MT | minutes tens |
| HU | hours units |
| HT | hours tens |
| C4-C14 | transmitted control bits. |

When in extension packet enabled mode the rows of information are organized as illustrated by Fig.11.

Row 23 of the extension page, as shown in Fig.11, contains packet 8/30. Packet 8/30 is mapped into the SAA5246A memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23
8/30/2 and 8/30/3 to Chapter 5 Row 23
8/30/4 to 8/30/15 to Chapter 6 Row 23
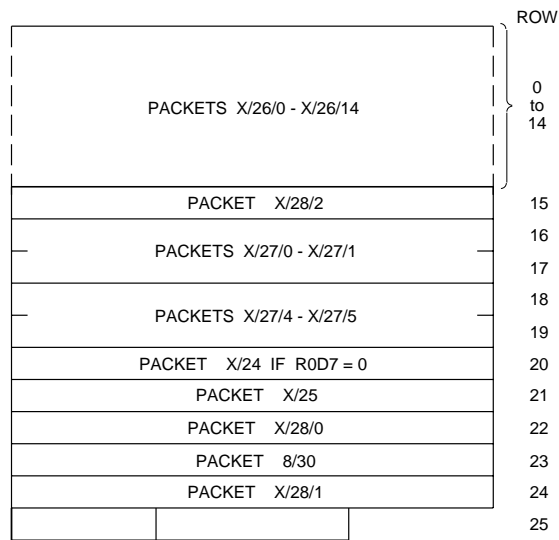
Fig.11  Organization of the extension memory.

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### Register maps

SAA5246A mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE; R11B is READ only. Register map (R3), for page requests, is shown in detail in Table 4.

**Table 2**  Register map.

| REGISTER | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Adv. control | 0 | X24 POS | FREE RUN PLL | AUTO $\overline{ODD}$/EVEN | DISABLE HDR ROLL | – | DISABLE $\overline{ODD}$/EVEN | VCR MODE | $\overline{R11}$/ R11B SELECT |
| Mode | 1 | VCS TO SCS | $\overline{7 + P}$/ 8-BIT | ACQ $\overline{ON}$/OFF | EXT. PACKET ENABLE | $\overline{DEW}$/ FULL FIELD | TCS ON FFB MODE | T1 | T0 |
| Page request address | 2 | HAM. CHECK | BANK SELECT A2 | ACQ CIRCUIT A1 | ACQ CIRCUIT A0 | TB | START COLUMN SC2 | START COLUMN SC1 | START COLUMN SC0 |
| Page request data | 3 | – | – | – | PRD4 | PRD3 | PRD2 | PRD1 | PRD0 |
| Display chapter | 4 | – | – | – | – | – | A2 | A1 | A0 |
| Display control (normal) | 5 | BKGND OUT | BKGND IN | COR OUT | COR IN | TEXT OUT | TEXT IN | PON OUT | PON IN |
| Display control (newsflash /subtitle) | 6 | BKGND OUT | BKGND IN | COR OUT | COR IN | TEXT OUT | TEXT IN | PON OUT | PON IN |
| Display mode | 7 | STATUS TOP | CURSOR ON | REVEAL ON | BOTTOM HALF | DOUBLE HEIGHT | BOX ON 24 | BOX ON 1-23 | BOX ON 0 |
| Active chapter | 8 | – | – | – | – | CLEAR MEM. | A2 | A1 | A0 |
| Cursor row | 9 | – | – | – | R4 | R3 | R2 | R1 | R0 |
| Cursor column | 10 | – | – | C5 | C4 | C3 | C2 | C1 | C0 |
| Cursor data | 11 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Device status | 11B | $\overline{625}$/525 SYNC | ROM VER R4 | ROM VER R3 | ROM VER R2 | ROM VER R1 | ROM VER R0 | DATA QUALITY | VCS SIGNAL QUALITY |

**Notes to Table 2**

1. '−' indicates a bit which does not exist and must be written to logic 0 for future compatibility.

2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.

3. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.

4. TB must be set to logic 0 for normal operation.

5. The I$^2$C-bus slave address is 0010001.

**Register description**

**R0 ADVANCED CONTROL - auto increments to Register 1**

| | |
|---|---|
| R11/R11B SELECT | Selects reading of R11 or R11B |
| VCR MODE | Selects short time constant of PLL when logic 1 |
| DISABLE $\overline{ODD}$/EVEN | Forces $\overline{ODD}$/EVEN output LOW when logic 1 |
| DISABLE HDR ROLL | Disables green rolling header and time |
| AUTO $\overline{ODD}$/EVEN | When set forces $\overline{ODD}$/EVEN low if any TV picture displayed, if DISABLE $\overline{ODD}$/EVEN = 0 |
| FREE RUN PLL | Will force the PLL to free run in all conditions |
| X24 POS | Automatic display of FASTEXT prompt row when logic 1 |

**R1 MODE - auto increments to Register 2**

| | |
|---|---|
| T0, T1 | Interlace/non-interlace 312/313 line control (see Table 4) |
| TCS ON FFB MODE | Text composite sync or direct sync select (see Table 4 for FFB mode selection) |
| $\overline{DEW}$/FULL FIELD | Field-flyback or full channel mode |
| EXT. PACKET ENABLE | Allocates 2K bytes memory per chapter |
| ACQ $\overline{ON}$/OFF | Acquisition circuits turned off when logic 1 |
| $\overline{7+P}$/8-BIT | 7 bits with parity checking or 8-bit mode |
| VCS TO SCS | When logic 1 enables display of messages with 60 Hz input signal |

**R2 PAGE REQUEST ADDRESS - auto increments to Register 3**

| | |
|---|---|
| HAM.CHECK | When logic 1 enables Hamming 8/4 checking of extension packet 27/0, 27/1 and 8/30/x |
| COL SC0 - SC2 | Point to start column for page request data (see Table 3) |
| TB | Must be logic 0 for normal operation |
| ACQ CIRCUIT | Selects one of four acquisition circuits |
| BANK SELECT | Selects which bank of four chapters is being accessed, when EXT. PACKET ENABLE = 0 |

**R3 PAGE REQUEST DATA - does not auto increment (see Table 3)**

**R4 DISPLAY CHAPTER - auto increments to Register 5**

determines which of the 8 pages is displayed

**R5 NORMAL DISPLAY CONTROL - auto increments to Register 6**

| | |
|---|---|
| PON | Picture on |
| TEXT | Text on |
| COR | Contrast reduction on |
| BKGND | Background colour on |

These functions have IN and OUT referring to inside and outside the boxing function respectively.

**R6 NEWSFLASH DISPLAY - auto increments to Register 7**

| | |
|---|---|
| PON | Picture on |
| TEXT | Text on |
| COR | Contrast reduction on |
| BKGND | Background colour on |

These functions have IN and OUT referring to inside and outside the boxing function respectively.

**R7 DISPLAY MODE - does not auto increment**

| | |
|---|---|
| BOX ON 0 | Boxing function allowed on Row 0 |
| BOX ON 1-23 | Boxing function allowed on Row 1-23 |
| BOX ON 24 | Boxing function allowed on Row 24 |
| DOUBLE HEIGHT | To display double height text |
| BOTTOM HALF | To select bottom half of page when DOUBLE HEIGHT = 1 |
| REVEAL ON | To reveal concealed text |
| CURSOR ON | To display cursor |
| STATUS TOP | Row 25 displayed above or below the main text |

**R8 ACTIVE CHAPTER - auto increments to Register 9**

| | |
|---|---|
| A0 to A2 | Active chapter |
| CLEAR MEMORY | When set to 1, clears the display memory. This bit is automatically reset |

**R9 CURSOR ROW - auto increments to Register 10**

| | |
|---|---|
| R0 to R4 | Active row for data written to or read from memory via the $I^2C$-bus |

**R10 CURSOR COLUMN - auto increments to Register 11 or 11B**

| | |
|---|---|
| C0 to C5 | Active column for data written to or read from memory via the $I^2C$-bus |

**R11 CURSOR DATA - does not auto increment**

| | |
|---|---|
| D0 to D7 | Data read from/written to memory via $I^2C$, at location pointed to by R8, R9 and R10. This location automatically increments each time R11 is accessed |

**R11B DEVICE STATUS - does not auto increment**

| | |
|---|---|
| VCS SIGNAL QUALITY | Indicates that the video signal quality is good and PLL is phase locked to input video when = 1 |
| DATA QUALITY | If good Teletext data is detected then = 1 |
| ROM VER R0 to R4 | Indicated language/ROM variant. See Table 6 - Table 13. |
| $\overline{625}$/525 SYNC | If the input video is a 525 line signal when = 1 |

**Table 3**   Register map for page requests (R3).

| START COLUMN | PRD4 | PRD3 | PRD2 | PRD1 | PRD0 |
|---|---|---|---|---|---|
| 0 | Do care<br>Magazine | $\overline{\text{HOLD}}$ | MAG2 | MAG1 | MAG0 |
| 1 | Do care<br>Page tens | PT3 | PT2 | PT1 | PT0 |
| 2 | Do care<br>Page units | PU3 | PU2 | PU1 | PU0 |
| 3 | Do care<br>Hours tens | X | X | HT1 | HT0 |
| 4 | Do care<br>Hours units | HU3 | HU2 | HU1 | HU0 |
| 5 | Do care<br>Minutes tens | X | MT2 | MT1 | MT0 |
| 6 | Do care<br>Minutes units | MU3 | MU2 | MU1 | MU0 |

**Notes to Table 3**

1. Abbreviations are as for Table 1 except for DO CARE bits.

2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page request. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.

3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated

4. Columns auto-increment on successive I²C-bus transmission bytes

5. "X' = Don' t care

**Table 4**   Interlace/non-interlace 312/313 line control and ODD/EVEN field detection option

| TCS ON<br>FFB MODE | T1 | T0 | RESULT |
|---|---|---|---|
| x | 0 | 0 | interlaced 312.5/312.5 lines |
| x | 0 | 1 | non-interlaced 312/313 lines (note 1) |
| x | 1 | 0 | non-interlaced 312/312 lines (note 1) |
| 0 | 1 | 1 | SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field<br>M7 version onwards |
| 1 | 1 | 1 | SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field<br>M7 version onwards |

**Notes to Table 4**

1. Reverts to interlaced mode if a newsflash or subtitle is being displayed.

2. 'x' = Don't care.

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## CLOCK SYSTEMS

### Crystal oscillator

The oscillator is a low amplitude, low distortion design operation at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.12.

**Table 5**  Crystal characteristics.

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **Crystal (27 MHz, 3rd overtone)** | | | | | |
| C1 | series capacitance | – | 1.7 | - | pF |
| C0 | parallel capacitance | – | 5.2 | – | pF |
| $C_L$ | load capacitance | – | 20 | – | pF |
| Rr | resonant resistance | – | – | 50 | $\Omega$ |
| R1 | series resistance | – | 20 | – | $\Omega$ |
| Xa | ageing | – | – | ±5 | $10^{-6}$/yr |
| Xj | adjustment tolerance | – | – | ±25 | $10^{-6}$ |
| Xd | drift | – | – | ±25 | $10^{-6}$ |
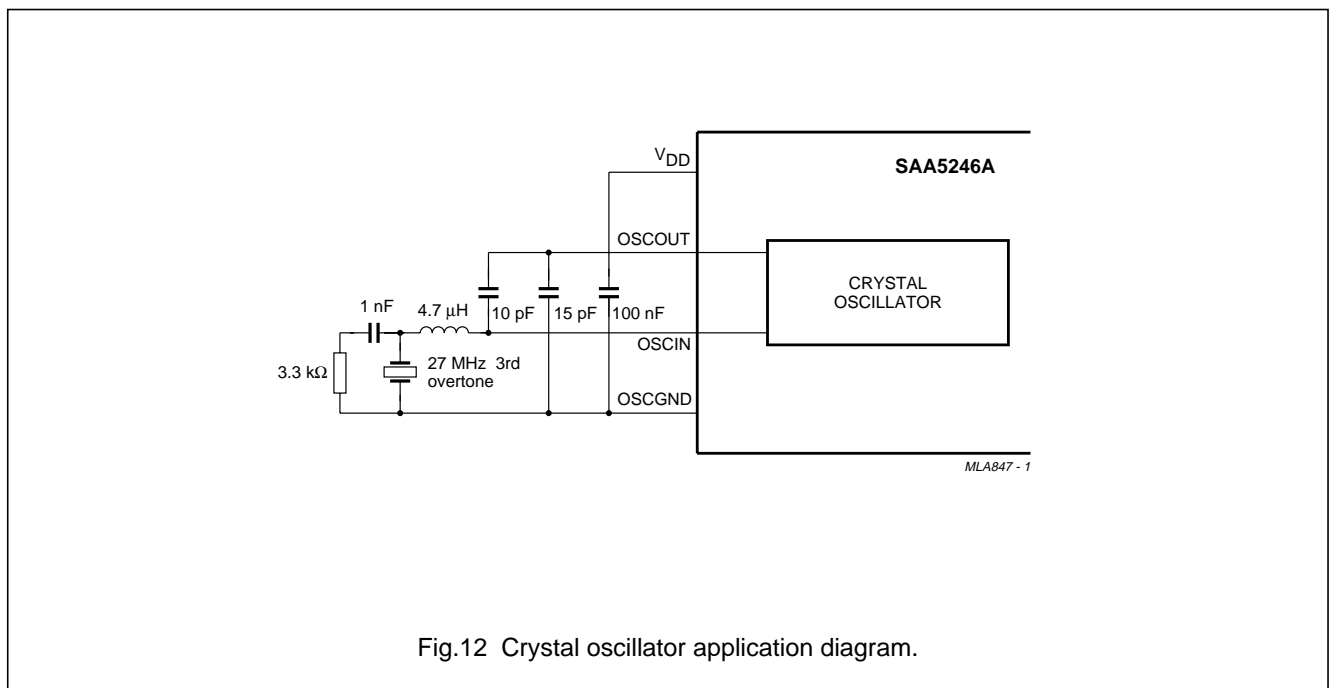


Fig.12  Crystal oscillator application diagram.

**Character sets**

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Tables 15 - 23 with reference to their table position in the basic character matrix illustrated in Table 14. The SAA5246A automatically decodes transmission bits C12 to C14. Tables 6 - 13 illustrate the character matrices.

Character bytes are listed as transmitted from b1 to b7.



Fig.13  Character format.
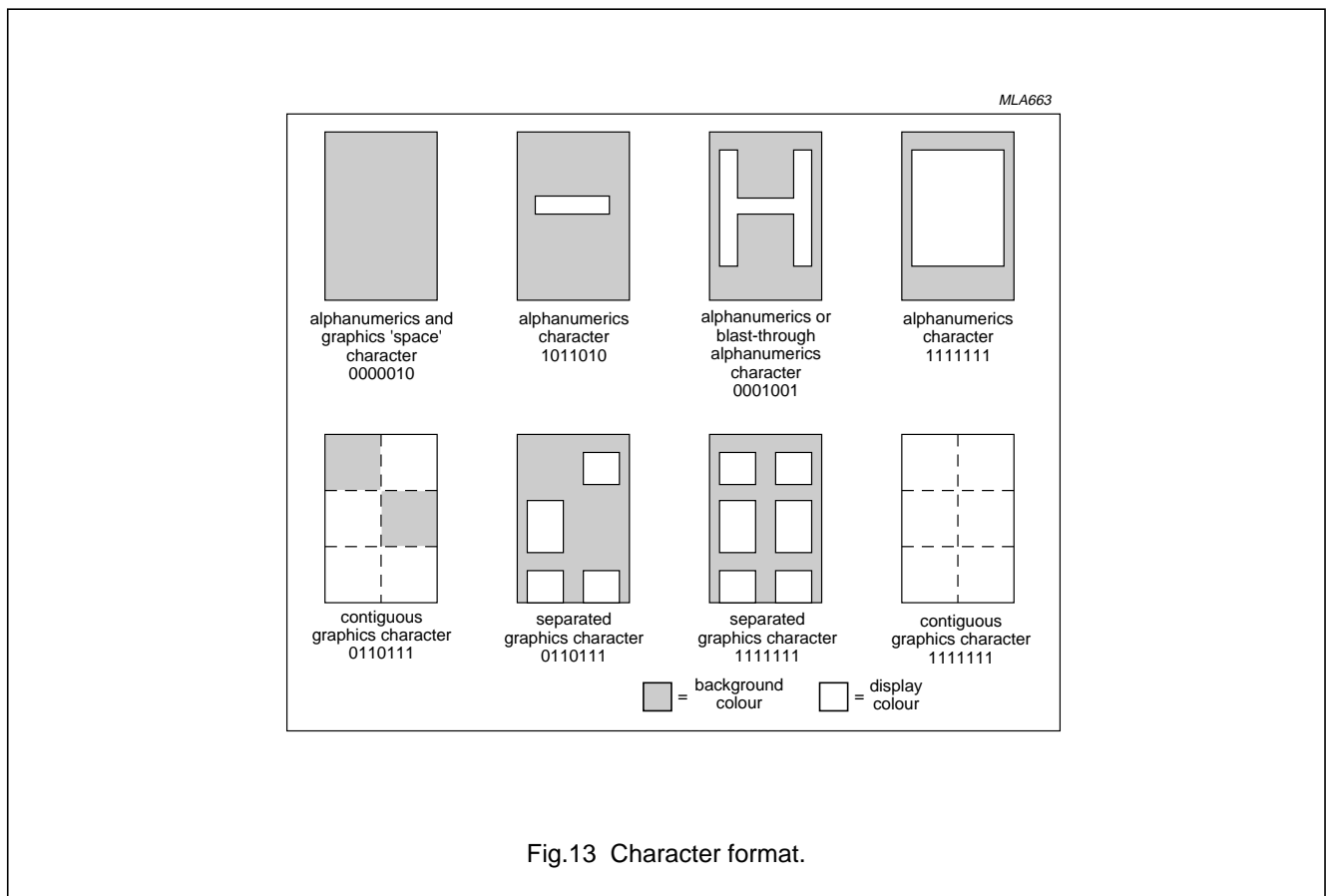
**Table 6**    SAA5246AP/E character data input decoding, West European languages.



MBA429

**Notes for character version number (00000) see Register 11B.**

1.   These control characters are reserved for compatibility with other data codes.

2.   These control characters are presumed before each row begins.

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**Table 7**  SAA5246AP/H character data input decoding, East European languages



MLA961

**Notes for character version number (00001) see Register 11B**

1. These control characters are reserved for compatibility with other data codes.

2. These control characters are presumed before each row begins.

**Table 8** SAA5246AP/T character data input decoding, West European and Turkish languages.

| BITS b8 b7 b6 b5 / b4 b3 b2 b1 | row | column 0 | 1 | 2 | 2a | 3 | 3a | 4 | 5 | 6 | 6a | 7 | 7a | 8 | 9 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 0 0 0 | 0 | alpha-numerics black | graphics black | | | 0 | | § | P | ° | | p | | @ | İ | é | à | ı | Á |
| 0 0 0 1 | 1 | alpha-numerics red | graphics red | ! | | 1 | | A | Q | a | | q | | — | ı | ù | è | ¿ | Â |
| 0 0 1 0 | 2 | alpha-numerics green | graphics green | " | | 2 | | B | R | b | | r | | ¼ | ş | á | â | ü | È |
| 0 0 1 1 | 3 | alpha-numerics yellow | graphics yellow | # | | 3 | | C | S | c | | s | | £ | | £ | é | ç | Î |
| 0 1 0 0 | 4 | alpha-numerics blue | graphics blue | $ | | 4 | | D | T | d | | t | | $ | ğ | $ | ï | $ | Ï |
| 0 1 0 1 | 5 | alpha-numerics magenta | graphics magenta | % | | 5 | | E | U | e | | u | | | | ã | Ä | º | Ó |
| 0 1 1 0 | 6 | alpha-numerics cyan | graphics cyan | & | | 6 | | F | V | f | | v | | | | ö | Ö | º | Ò |
| 0 1 1 1 | 7 | alpha-numerics white [2] | graphics white | ' | | 7 | | G | W | g | | w | | | | · | Ç | Ñ | Ú |
| 1 0 0 0 | 8 | flash | conceal display | ( | | 8 | | H | X | h | | x | | ‖ | ö | ò | ô | ñ | ı |
| 1 0 0 1 | 9 | steady [2] | contiguous graphics [2] | ) | | 9 | | I | Y | i | | y | | ¾ | ç | è | û | è | Ù |
| 1 0 1 0 | 10 | end box [2] | separated graphics [2] | * | | : | | J | Z | j | | z | | ÷ | ü | ì | ç | à | ↓ |
| 1 0 1 1 | 11 | start box | ESC [1] | + | | ; | | K | Ä | k | | ä | | ← | Ş | ° | ë | á | É |
| 1 1 0 0 | 12 | normal height [2] | black background [2] | , | | < | | L | Ö | l | | ö | | ½ | Ö | ç | ê | é | ä |
| 1 1 0 1 | 13 | double height | new background | - | | = | | M | Ü | m | | ü | | → | Ç | → | ù | í | Û |
| 1 1 1 0 | 14 | SO [1] | hold graphics | . | | > | | N | ^ | n | | ß | | ↑ | Ü | ↑ | î | ó | Ã |
| 1 1 1 1 | 15 | SI [1] | release graphics [2] | / | | ? | | O | _ | o | | | | # | Ğ | # | # | ú | ı |

MBA431

**Notes for character version number (00010) see Register 11B.**

1. These control characters are reserved for compatibility with other data codes
2. These control characters are presumed before each row begins.

**Table 9**  SAA5246AP/J character data input decoding, Jugoslav languages



**Notes for character version number (00011) see Register 11B**

1.  * These control characters are reserved for compatibility with other data codes.

2.  ** These control characters are presumed before each row begins.

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# SAA5246A

**Table 10** SAA5246AP/K character data input decoding, French and Arabic languages.



MLA972 - 1

**Notes for character version number (00100) see Register 11B.**

1. These control characters are reserved for compatibility with other data codes.

2. These control characters are presumed before each row begins.

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**Table 11** SAA5246AP/L character data input decoding, Arabic and Hebrew languages.



*MLA963 - 1*

**Note for character version number (00100) see Register 11B.**

1. These control characters are reserved for compatibility with other data codes.

2. These control characters are presumed before each row begins.

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## SAA5246A

**Table 12** SAA5246AP/I character data input decoding, Greek and Turkish languages.



*MLA964 - 1*

**Note for character version number (00110) see Register 11B.**

1. * These control characters are reserved for compatibility with other data codes.

2. ** These control characters are presumed before each row begins.

# Integrated VIP and Teletext (IVT1.0)

# SAA5246A

**Table 13** SAA5246AP/S character data input decoding, English and Thai languages.

| BITS $b_8$ $b_7$ $b_6$ $b_5$ / $b_4 b_3 b_2 b_1$ | column 0 | 1 | 2 | 2a | 3 | 3a | 4 | 5 | 6 | 6a | 7 | 7a | 8 | 9 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| row | | | | | | | | | | | | | | | | | | |
| 0 0 0 0 — 0 | alpha-numerics black | graphics black | | | | | | | | | | | | | | | | |
| 0 0 0 1 — 1 | alpha-numerics red | graphics red | | | | | | | | | | | | | | | | |
| 0 0 1 0 — 2 | alpha-numerics green | graphics green | | | | | | | | | | | | | | | | |
| 0 0 1 1 — 3 | alpha-numerics yellow | graphics yellow | | | | | | | | | | | | | | | | |
| 0 1 0 0 — 4 | alpha-numerics blue | graphics blue | | | | | | | | | | | | | | | | |
| 0 1 0 1 — 5 | alpha-numerics magenta | graphics magenta | | | | | | | | | | | | | | | | |
| 0 1 1 0 — 6 | alpha-numerics cyan | graphics cyan | | | | | | | | | | | | | | | | |
| 0 1 1 1 — 7 | alpha-numerics white ** | graphics white | | | | | | | | | | | | | | | | |
| 1 0 0 0 — 8 | flash | conceal display | | | | | | | | | | | | | | | | |
| 1 0 0 1 — 9 | steady ** | contiguous graphics ** | | | | | | | | | | | | | | | | |
| 1 0 1 0 — 10 | end box ** | separated graphics | | | | | | | | | | | | | | | | |
| 1 0 1 1 — 11 | start box | TWIST | | | | | | | | | | | | | | | | |
| 1 1 0 0 — 12 | normal height ** | black back-ground ** | | | | | | | | | | | | | | | | |
| 1 1 0 1 — 13 | double height | new back-ground | | | | | | | | | | | | | | | | |
| 1 1 1 0 — 14 | SO * | hold graphics | | | | | | | | | | | | | | | | |
| 1 1 1 1 — 15 | SI * | release graphics ** | | | | | | | | | | | | | | | | |

*MLA965 - 1*

**Note For character version number (00111) see Register 11B.**

1. * These control characters are reserved for compatibility with other data codes.
2. ** These control characters are presumed before each row begins.

**Notes to Table 6 - 13**

1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.

2. Characters may be referred to by column and row, For example 2/5 refers to %.

3. Black represents displayed colour. White represents background.

4. The SAA5246A national option characters are illustrated in Table

5. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only). Characters 5/12, 5/13, 5/14 and 5/15 are combined with 5/11 (S code only).

6. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 8.

7. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

**Table 14** SAA5146A basic character matrix.



Where: NC = national option character position.

**Table 15** SAA5246AP/E national option character set.



| LANGUAGE | PHCB [1] | | | CHARACTER POSITION (COLUMN / ROW) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C12 | C13 | C14 | 2 / 3 | 2 / 4 | 4 / 0 | 5 / 11 | 5 / 12 | 5 / 13 | 5 / 14 | 5 / 15 | 6 / 0 | 7 / 11 | 7 / 12 | 7 / 13 | 7 / 14 |
| ENGLISH | 0 | 0 | 0 | £ | $ | @ | ← | ½ | → | ↑ | # | ─ | ¼ | ‖ | ¾ | ÷ |
| GERMAN | 0 | 0 | 1 | # | $ | § | Ä | Ö | Ü | ^ | _ | ° | ä | ö | ü | ß |
| SWEDISH | 0 | 1 | 0 | # | ¤ | É | Ä | Ö | Å | Ü | _ | é | ä | ö | å | ü |
| ITALIAN [2] | 0 | 1 | 1 | £ | $ | é | ° | ç | → | ↑ | # | ù | à | ò | è | ì |
| FRENCH | 1 | 0 | 0 | é | ï | à | ë | ê | ù | î | # | è | â | ô | û | ç |
| SPANISH | 1 | 0 | 1 | ç | $ | ¡ | á | é | í | ó | ú | ¿ | ü | ñ | è | à |

*MEA559*

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

**Table 16** SAA5246AP/H national option character set.

| LANGUAGE | PHCB [1] | | | CHARACTER POSITION (COLUMN / ROW) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C12 | C13 | C14 | 2 / 3 | 2 / 4 | 4 / 0 | 5 / 11 | 5 / 12 | 5 / 13 | 5 / 14 | 5 / 15 | 6 / 0 | 7 / 11 | 7 / 12 | 7 / 13 | 7 / 14 |
| POLISH | 0 | 0 | 0 | # | ń | ą | Ż | Ś | Ł | ć | ó | ę | ż | ś | Ź | ź |
| GERMAN | 0 | 0 | 1 | # | $ | § | Ä | Ö | Ü | ^ | _ | ° | ä | ö | ü | ß |
| SWEDISH | 0 | 1 | 0 | # | ¤ | É | Ä | Ö | Å | Ü | _ | é | ä | ö | å | ü |
| SERBO-CROAT | 1 | 0 | 1 | # | ½ | Č | Ć | Ž | Đ | Š | ë | č | ć | ž | đ | š |
| CZECHOSLOVAKIA | 1 | 1 | 0 | # | ů | č | ť | ž | ý | í | ř | é | á | ě | ú | š |
| RUMANIAN | 1 | 1 | 1 | # | ¤ | Ţ | Â | Ş | Ă | Î | ı | ţ | â | ş | ă | î |

MLA966

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 14.

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**Table 17** SAA5246AP/T national option character set.

| LANGUAGE | PHCB [1] | | | CHARACTER POSITION (COLUMN / ROW) | | | | | | | | | | | | | |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | C12 | C13 | C14 | 2 / 3 | 2 / 4 | 4 / 0 | 5 / 11 | 5 / 12 | 5 / 13 | 5 / 14 | 5 / 15 | 6 / 0 | 7 / 11 | 7 / 12 | 7 / 13 | 7 / 14 |
| ENGLISH | 0 | 0 | 0 | £ | $ | @ | ← | ½ | → | ↑ | # | — | ¼ | ‖ | ¾ | ÷ |
| GERMAN | 0 | 0 | 1 | # | $ | § | Ä | Ö | Ü | ^ | _ | ° | ä | ö | ü | ß |
| TURKISH | 1 | 1 | 0 | Ŧ | ğ | İ | Ş | Ö | Ç | Ü | Ğ | ı | ş | ö | ç | ü |
| ITALIAN | 0 | 1 | 1 | £ | $ | é | ° | ç | → | ↑ | # | ù | à | ò | è | ì |
| FRENCH | 1 | 0 | 0 | é | ï | à | ë | ê | ù | î | # | è | â | ô | û | ç |
| SPANISH | 1 | 0 | 1 | ç | $ | ¡ | á | é | í | ó | ú | ¿ | ü | ñ | è | à |

*MBA430*

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 14.

## Integrated VIP and Teletext (IVT1.0)

## SAA5246A

**Table 18** SAA5246AP/J national option character set.

| LANGUAGE | PHCB [1] | | | CHARACTER POSITION (COLUMN / ROW) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C12 | C13 | C14 | 2 / 3 | 2 / 4 | 4 / 0 | 5 / 11 | 5 / 12 | 5 / 13 | 5 / 14 | 5 / 15 | 6 / 0 | 7 / 11 | 7 / 12 | 7 / 13 | 7 / 14 |
| SERBO-CROAT LATIN | 0 | 1 | 0 | # | Ë | Č | Ć | Ž | Đ | Š | ë | č | ć | ž | đ | š |
| SERBO-CROAT LATIN | 0 | 1 | 1 | # | Ë | Č | Ć | Ž | Đ | Š | ë | č | ć | ž | đ | š |
| HUNGARIAN SWEDISH | 0 | 1 | 1 | # | $ | É | Ä | Ö | Å | Ü | _ | é | ä | ö | å | ü |
| SERBO-CROAT LATIN | 0 | 1 | 1 | # | Ë | Č | Ć | Ž | Đ | Š | ë | č | ć | ž | đ | š |
| SERBO-CROAT | 0 | 1 | 1 | # | Ë | Č | Ć | Ž | Đ | Š | ë | č | ć | ž | đ | š |
| (RUMANIAN) | 0 | 1 | 1 | # | $ | Ţ | Ă | Ş | Â | Î | ı | ţ | ă | ş | ă | î |
| RUMANIAN | 0 | 1 | 1 | # | $ | Ţ | Ă | Ş | Â | Î | ı | ţ | ă | ş | ă | î |
| SERBO-CROATIC CYRILLIC | 1 | 0 | 0 | | | | | | | | | | | | |



(1) PHCB are the Page Header Control Bits. Other combinations default to Serbo-Croat Latin.

**Table 19** SAA5246AP/K national option character set.



| LANGUAGE | FRENCH | ARABIC |
|---|---|---|
| PHCB [1] (C12, C13, C14) | 1  0  0 | 1  1  1 |

MLA968 - 1

(1) PHCB are the Page Header Control Bits. Other combinations default to French.

## Integrated VIP and Teletext (IVT1.0)

## SAA5246A

**Table 20** SAA5246AP/L national option character set.



MLA967

(1) PHCB are the Page Header Control Bits. Other combinations default to Hebrew English.

**Table 21** SAA5246AP/I national option character set.



|  | | | | | | |  | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 5 | 6 | 7 | | 2 | 3 | 4 | 5 | 6 | 7 |

| LANGUAGE | TURKISH | GREEK |
|---|---|---|
| PHCB [1] (C12, C13, C14) | 1 1 0 | 1 1 1 |

MLA969 - 1

(1) PHCB are the Page Header Control Bits. Other combinations default to Turkish.

**Table 22** SAA5246AP/S national option character set (part A).



| | English ( 0    0    0 ) TWIST not invoked | PHCB [1] $(C_{12}, C_{13}, C_{14})$ |
| | OR | |
| | Thai ( 0    1    0 ) and TWIST invoked | PHCB [1] $(C_{12}, C_{13}, C_{14})$ |

MLA971a

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Integrated VIP and Teletext (IVT1.0)

SAA5246A

**Table 23** SAA5246AP/S national option character set (part B).



| | 0 | 1 | 2 | 2a | 3 | 3a | 4 | 5 | 6 | 6a | 7 | 7a | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 14a | 15 | 15a |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Thai ( 0   1   0 )
TWIST not invoked

OR

English ( 0   0   0 )
and TWIST invoked

*MLA971b*

(1)  PHCB are the Page Header Control Bits. Other combinations default to English.
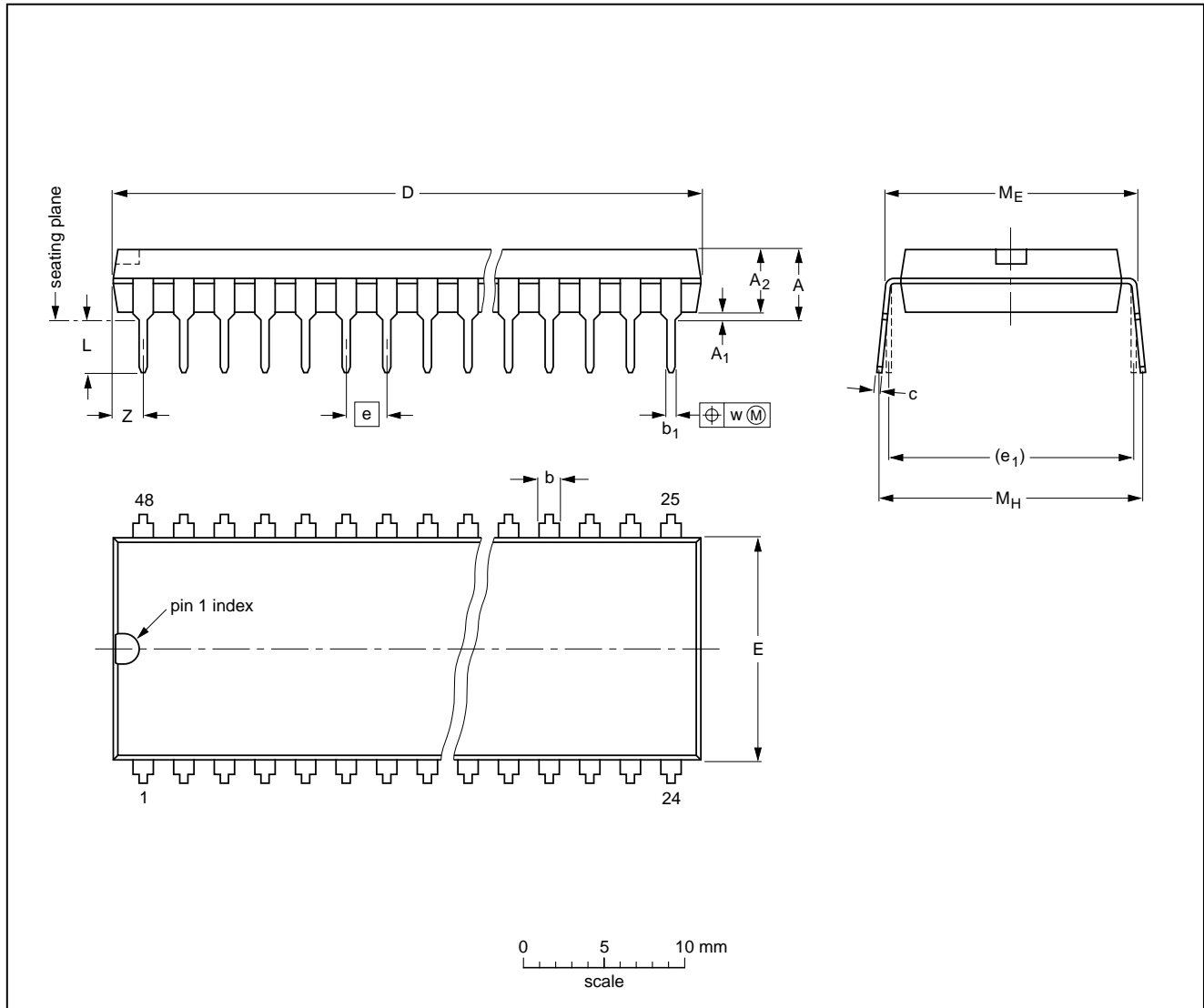
Integrated VIP and Teletext (IVT1.0)

SAA5246A

## PACKAGE OUTLINES

**DIP48: plastic dual in-line package; 48 leads (600 mil)**

**SOT240-1**



scale: 0 — 5 — 10 mm

**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A$_1$ min. | A$_2$ max. | b | b$_1$ | c | D$^{(1)}$ | E$^{(1)}$ | e | e$_1$ | L | M$_E$ | M$_H$ | w | Z$^{(1)}$ max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.9 | 0.36 | 4.06 | 1.4 1.14 | 0.53 0.38 | 0.36 0.23 | 62.60 61.60 | 14.22 13.56 | 2.54 | 15.24 | 3.90 3.05 | 15.88 15.24 | 18.46 15.24 | 0.254 | 2.1 |
| inches | 0.19 | 0.014 | 0.16 | 0.055 0.045 | 0.021 0.015 | 0.014 0.009 | 2.46 2.42 | 0.56 0.53 | 0.10 | 0.60 | 0.15 0.12 | 0.63 0.60 | 0.73 0.60 | 0.01 | 0.083 |

**Note**

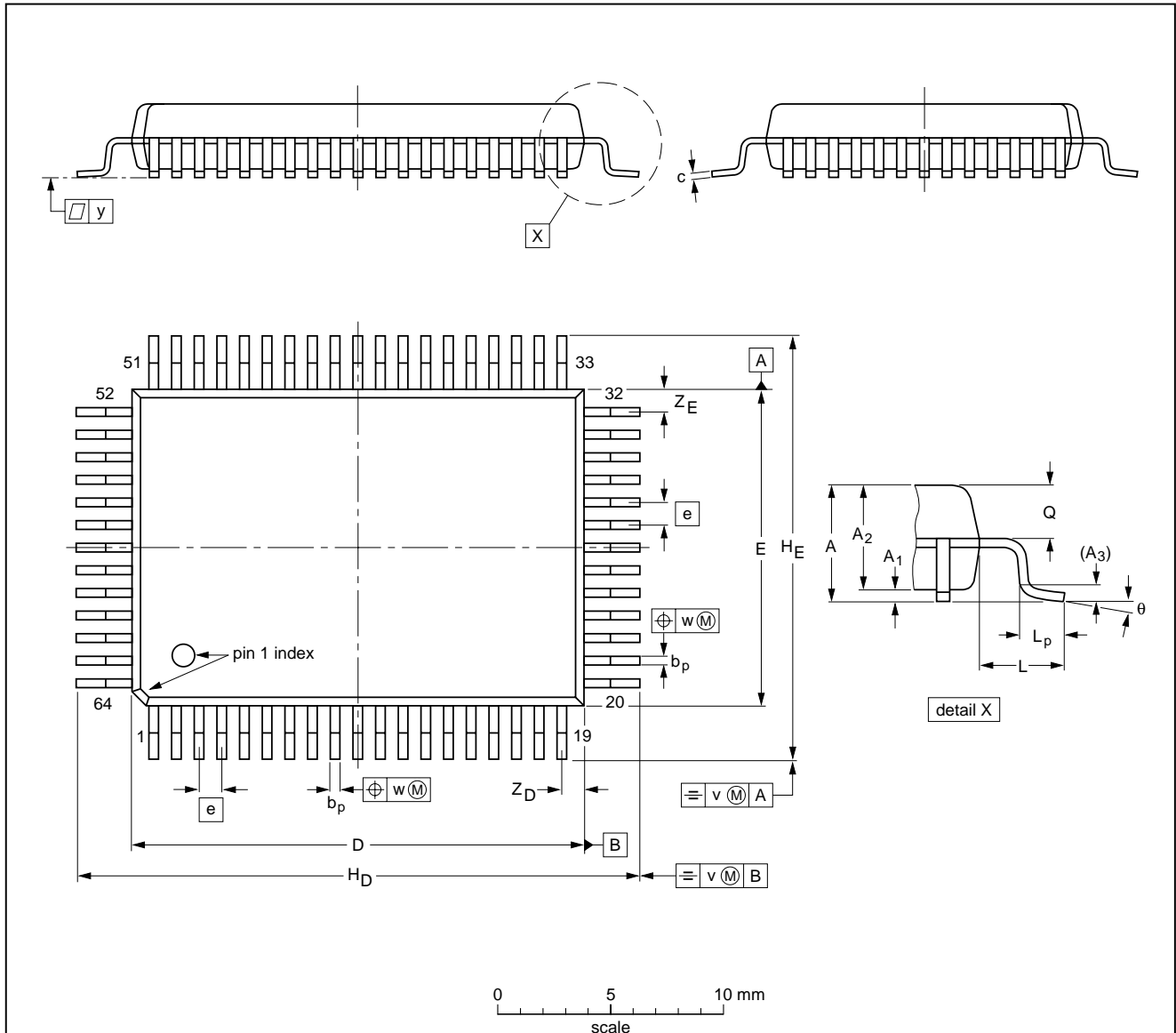1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT240-1 | | | | | | 92-11-17 95-01-25 |

# Integrated VIP and Teletext (IVT1.0)

# SAA5246A

**QFP64: plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 x 20 x 2.8 mm**          **SOT319-3**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D(1) | E(1) | e | H_D | H_E | L | Lₚ | Q | v | w | y | Z_D(1) | Z_E(1) | θ |
|------|--------|----|----|----|----|----|------|------|----|-----|-----|----|----|----|----|----|----|----|----|----|
| mm | 3.25 | 0.30 0.10 | 2.90 2.65 | 0.25 | 0.50 0.35 | 0.25 0.14 | 20.1 19.9 | 14.1 13.9 | 1 | 25.0 24.4 | 19.0 18.4 | 2.35 | 1.4 1.0 | 1.4 1.2 | 0.2 | 0.2 | 0.1 | 1.2 0.8 | 1.2 0.8 | 7° 0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|------|--|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT319-3 | | | | | | 94-03-22 95-02-04 |

## Integrated VIP and Teletext (IVT1.0)

**SAA5246A**

### SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### SDIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### QFP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**

- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

**Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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