

# DATA SHEET

## **SC28L92**

Dual Universal Asynchronous  
Receiver/Transmitter (DUART)

Preliminary specification

1998 Oct 05

IC19 Data Handbook

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

## SC28L92

### DESCRIPTION

The SC28L92 is a pin and function replacement for the SCC2692 and SC26C92 operating at 3.3 or 5 volts supply with added features and deeper FIFOs. Its configuration on power up is that of the 2692. Its differences from the 2692 are: 16 character receiver, 16 character transmit FIFOs, watch dog timer for each receiver, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (Neither the SC26C92 nor The SCC2692 is being discontinued.)

Pin programming will allow the device to operate with either the Motorola or Intel bus interface The bit 3 of the MR0a register allows the device to operate in an 8 byte FIFO mode if strict compliance with the SC26C92 FIFO structure is required

The Philips Semiconductors SC28L92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates; a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by 8 or 16 character FIFOs to minimize the potential of receiver overrun, transmitter underpin and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC28L92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC28L92 is available in two package versions: a 44-pin PLCC and 44-pin plastic quad flat pack (PQFP).

### FEATURES

- 3.3 or 5.0 volt operation
- Dual full-duplex independent asynchronous receiver/transmitters
- 16 character FIFOs for each receiver and transmitter
- Pin programming for 68K or 80xxx bus interface
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
- 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 23 fixed rates: 50 to 230.4k baud
  - Other baud rates to MHz at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loop back
  - Remote loop back
  - Multi-drop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate interrupt outputs that may be wire ORed.
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates:
  - 1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multi-drop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver time-out mode
- Single +3.3V or +5V power supply
- Powers up to emulate SCC2692 and S26C92

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**Dual Universal Asynchronous  
Receiver/Transmitter (DUART)**

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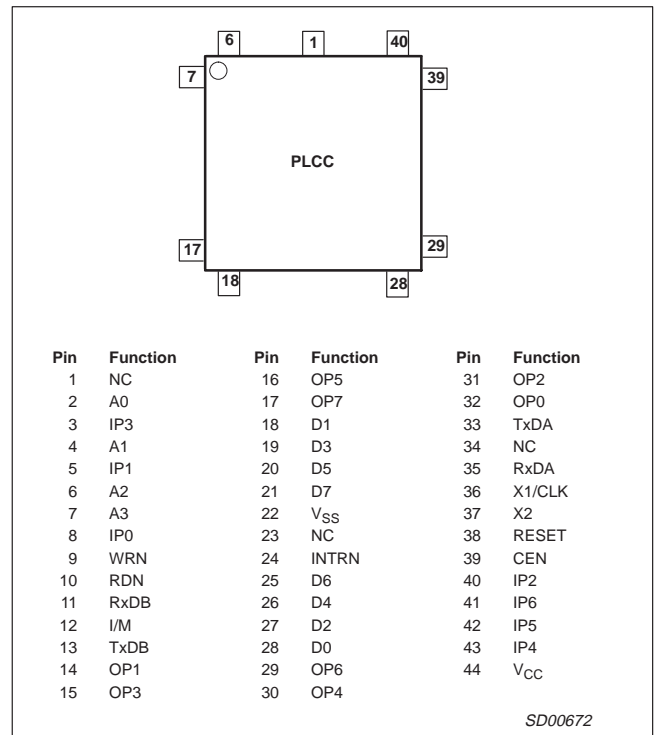
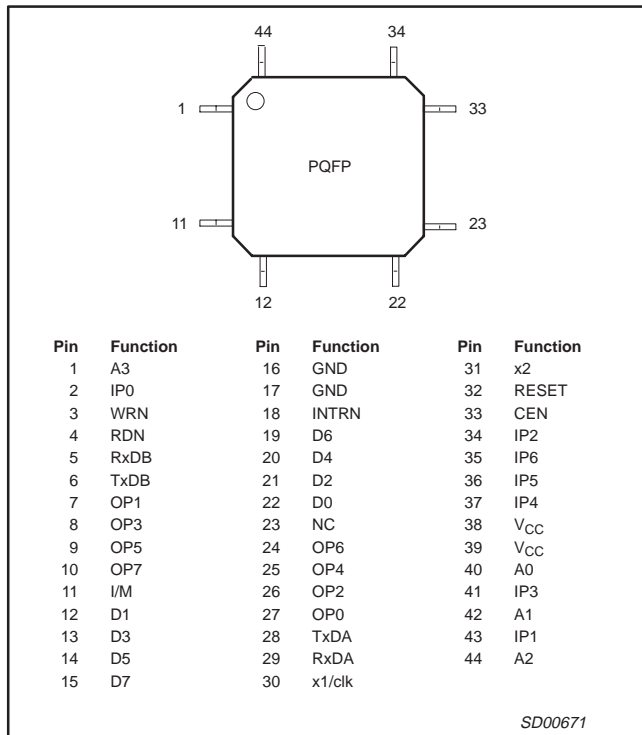
**SC28L92****ORDERING INFORMATION**

DESCRIPTION	INDUSTRIAL	DRAWING NUMBER
	$V_{CC} = +3.3 +5V \pm 10\%$ ,	
	$T_A = -40 \text{ to } +85^\circ\text{C}$	
44-Pin Plastic Leaded Chip Carrier (PLCC)	SC28L92A1A	SOT187-2
44-Pin Plastic Quad Flat Pack (PQFP)	SC28L92A1B	SOT307-2

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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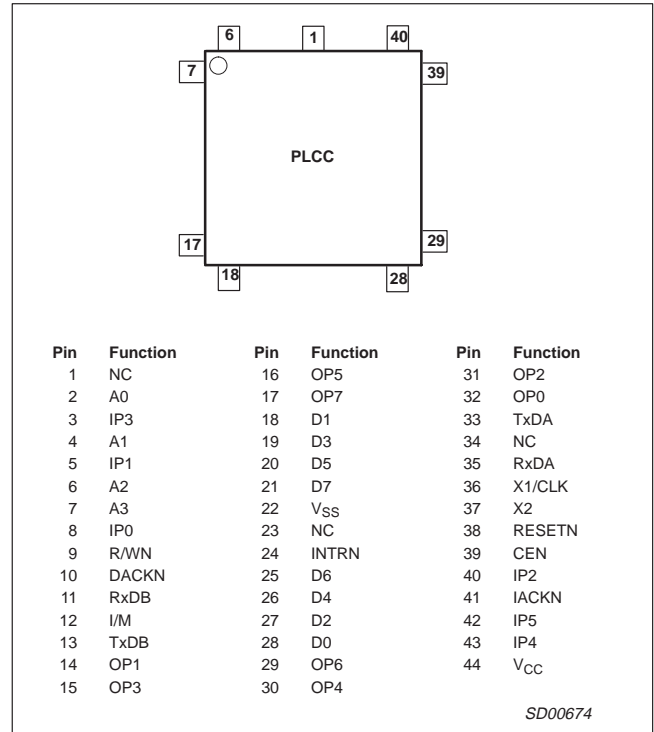
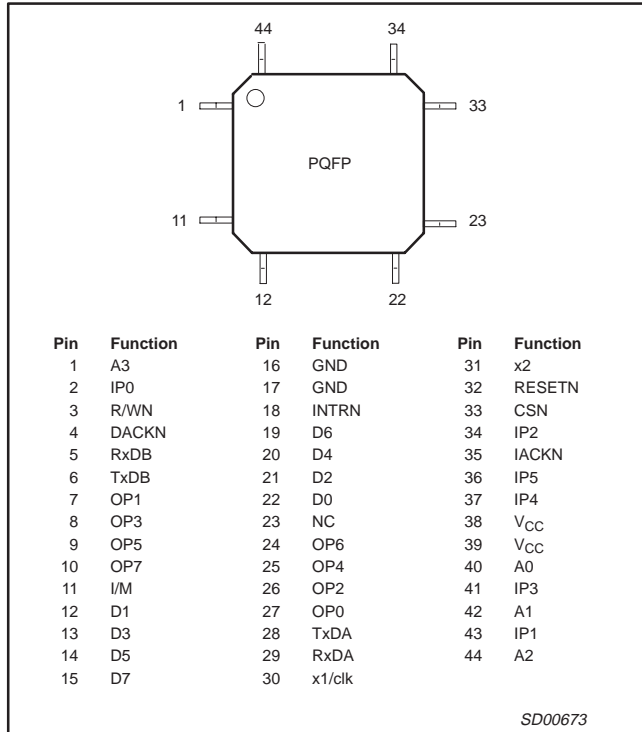
### PIN CONFIGURATION DIAGRAM 80XXX PIN CONFIGURATION



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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### PIN CONFIGURATION DIAGRAM 68XXX PIN CONFIGURATION



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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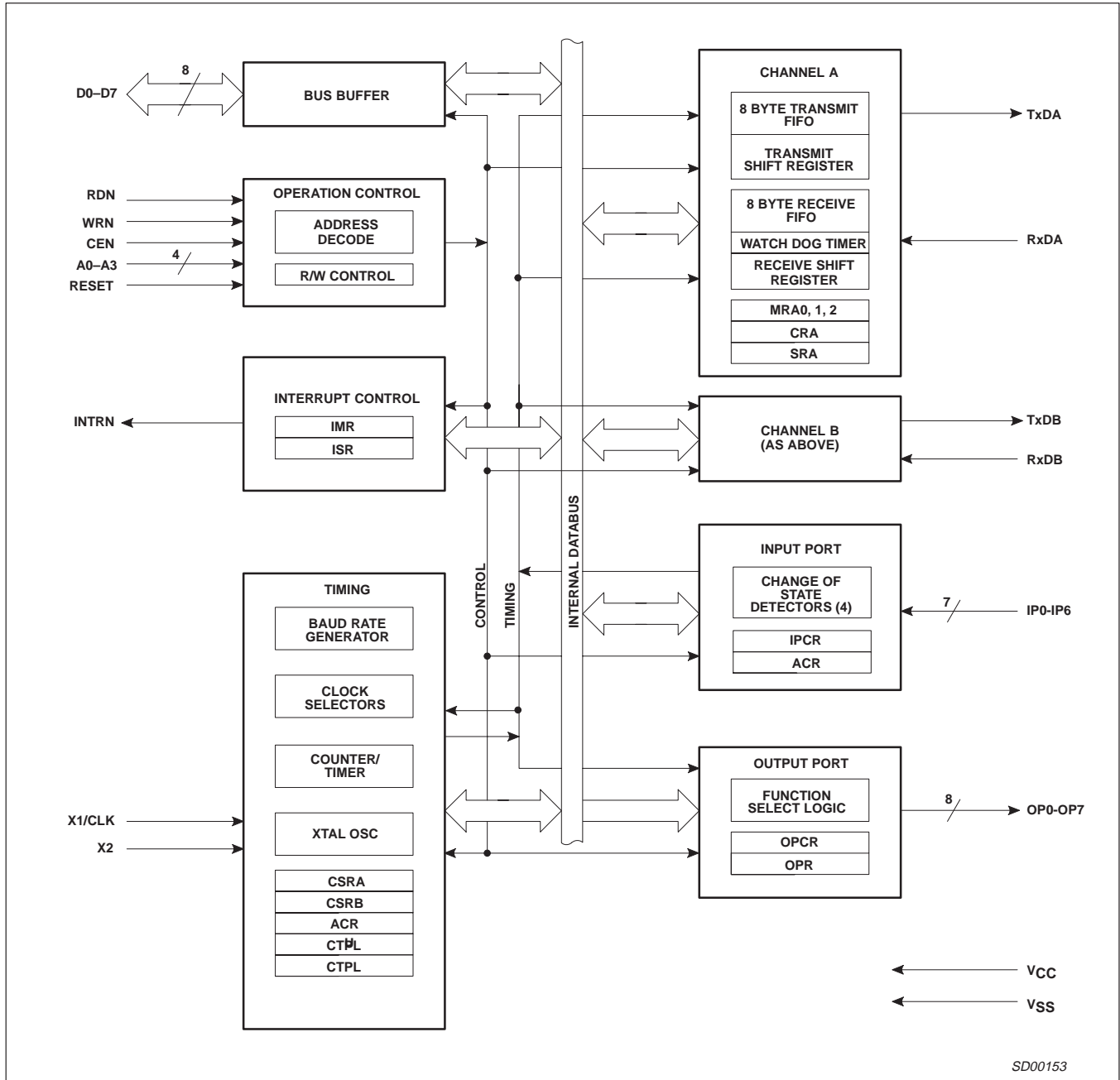


Figure 1. Block Diagram

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## PIN CONFIGURATION FOR 80XXX BUS INTERFACE (INTEL®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	<b>Bus Configuration:</b> When high or not connected configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	<b>Data Bus:</b> Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	<b>Chip Enable:</b> Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
WRN	I	<b>Write Strobe:</b> When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	<b>Read Strobe:</b> When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	<b>Address Inputs:</b> Select the DUART internal registers and ports for read/write operations.
RESET	I	<b>Reset:</b> A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	<b>Interrupt Request:</b> Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	<b>Crystal 1:</b> Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	<b>Crystal 2:</b> Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	<b>Channel A Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High; "space" is Low.
RxDB	I	<b>Channel B Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High; "space" is Low.
TxDA	O	<b>Channel A Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	<b>Channel B Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
OP0	O	<b>Output 0:</b> General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	<b>Output 1:</b> General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	<b>Output 2:</b> General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	<b>Output 3:</b> General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	<b>Output 4:</b> General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR[1] output.
OP5	O	<b>Output 5:</b> General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	<b>Output 6:</b> General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	<b>Output 7:</b> General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	<b>Input 0:</b> General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	<b>Input 1:</b> General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	<b>Input 2:</b> General-purpose input or counter/timer external clock input.
IP3	I	<b>Input 3:</b> General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	<b>Input 4:</b> General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	<b>Input 5:</b> General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	I	<b>Input 6:</b> General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V <sub>CC</sub>	Pwr	<b>Power Supply:</b> +3.3 or +5V supply input ±10%
GND	Pwr	<b>Ground</b>

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## PIN CONFIGURATION FOR 68XXX BUS INTERFACE (MOTOROLA®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	<b>Bus Configuration:</b> When low configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	<b>Data Bus:</b> Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	<b>Chip Enable:</b> Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
R/WN	I	<b>Read/Write:</b> Input Signal. When CSN is low R/WN high input indicates a read cycle; when low indicates a write cycle.
IACKN	I	<b>Interrupt Acknowledge:</b> Active low input indicating an interrupt acknowledge cycle. Usually asserted by the CPU in response to an interrupt request. When asserted places the interrupt vector on the bus and asserts DACKN.
DACKN	O	<b>Data Transfer Acknowledge:</b> A3-State active -low output asserted in a write, read, or interrupt acknowledge cycle to indicate proper transfer of data between the CPU and the DUART.
A0–A3	I	<b>Address Inputs:</b> Select the DUART internal registers and ports for read/write operations.
RESETN	I	<b>Reset:</b> A low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	<b>Interrupt Request:</b> Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	<b>Crystal 1:</b> Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	<b>Crystal 2:</b> Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	<b>Channel A Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	I	<b>Channel B Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	O	<b>Channel A Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	<b>Channel B Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
OP0	O	<b>Output 0:</b> General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	<b>Output 1:</b> General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	<b>Output 2:</b> General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	<b>Output 3:</b> General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	<b>Output 4:</b> General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR [1] output.
OP5	O	<b>Output 5:</b> General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	<b>Output 6:</b> General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	<b>Output 7:</b> General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	<b>Input 0:</b> General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	<b>Input 1:</b> General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	<b>Input 2:</b> General-purpose input or counter/timer external clock input.
IP3	I	<b>Input 3:</b> General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	<b>Input 4:</b> General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	<b>Input 5:</b> General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V <sub>CC</sub>	Pwr	<b>Power Supply:</b> +3.3 or +5V supply input ±10%
GND	Pwr	<b>Ground</b>



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	RATING	UNIT
$T_A$	Operating ambient temperature range <sup>2</sup>	Note 4	°C
$T_{STG}$	Storage temperature range	-65 to +150	°C
$V_{CC}$	Voltage from $V_{CC}$ to GND <sup>3</sup>	-0.5 to +7.0	V
$V_S$	Voltage from any pin to GND <sup>3</sup>	-0.5 to $V_{CC} + 0.5$	V
$P_D$	Package power dissipation (PLCC44)	2.4	W
$P_D$	Package power dissipation (PQFP44)	1.78	W
	Derating factor above 25°C (PLCC44)	19	mW/°C
	Derating factor above 25°C (PQFP44)	14	mW/°C

### NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
- For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
- This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameters are valid over specified temperature range.

## DC ELECTRICAL CHARACTERISTICS<sup>1, 2</sup>

$V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$V_{IL}$	Input low voltage				0.8	V
$V_{IH}$	Input high voltage (except X1/CLK)	0 to +70°C	2.4			
$V_{IH}$	Input high voltage (X1/CLK)	-40 to +85°C	2.5			V
$V_{IH}$	Input high voltage (X1/CLK)		$0.8 V_{CC}$			V
$V_{OL}$	Output low voltage	$I_{OL} = 2.4\text{mA}$			0.4	V
$V_{OH}$	Output high voltage (except OD outputs) <sup>3</sup>	$I_{OH} = -400\mu\text{A}$	$V_{CC} - 0.5$			V
$I_{IX1PD}$	X1/CLK input current - power down	$V_{IN} = 0$ to $V_{CC}$	-1		+1	$\mu\text{A}$
$I_{ILX1}$	X1/CLK input low current - operating	$V_{IN} = 0$	-100		0	$\mu\text{A}$
$I_{IHX1}$	X1/CLK input high current - operating	$V_{IN} = V_{CC}$	0		100	$\mu\text{A}$
$I_I$	Input leakage current: All except input port pins Input port pins	$V_{IN} = 0$ to $V_{CC}$ $V_{IN} = 0$ to $V_{CC}$	-1 -10		+1 +10	$\mu\text{A}$ $\mu\text{A}$
$I_{OZH}$	Output off current high, 3-State data bus	$V_{IN} = V_{CC}$			1	$\mu\text{A}$
$I_{OZL}$	Output off current low, 3-State data bus	$V_{IN} = 0\text{V}$	-1			$\mu\text{A}$
$I_{ODL}$	Open-drain output low current in off-state	$V_{IN} = 0$	-1			$\mu\text{A}$
$I_{ODH}$	Open-drain output high current in off-state	$V_{IN} = V_{CC}$			1	$\mu\text{A}$
$I_{CC}$	Power supply current <sup>4</sup> Operating mode Power down mode <sup>5</sup>	CMOS input levels CMOS input levels		2	25 10.0	mA $\mu\text{A}$

### NOTES:

- Parameters are valid over specified temperature range.
- Typical values are at +25°C, typical supply voltages, and typical processing parameters.
- Test conditions for outputs:  $C_L = 150\text{pF}$ , except interrupt outputs. Test conditions for interrupt outputs:  $C_L = 50\text{pF}$ ,  $R_L = 2.7\text{K}\Omega$  to  $V_{CC}$ .
- All outputs are disconnected. Inputs are switching between CMOS levels of  $V_{CC} - 0.2\text{V}$  and  $V_{SS} + 0.2\text{V}$ .
- See UART application note for power down currents of  $5\mu\text{A}$  or less.

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## AC CHARACTERISTICS (80XXX MODE)<sup>1, 2, 3</sup>

$V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
<b>Reset Timing (See Figure 2)</b>					
$t_{RES}$	Reset pulse width	200			ns
<b>Bus Timing<sup>5</sup> (See Figure 3)</b>					
$t_{AS}$	A0–A3 setup time to RDN, WRN Low	10			ns
$t_{AH}$	A0–A3 hold time from RDN, WRN low	45			ns
$t_{CS}$	CEN setup time to RDN, WRN low	0			ns
$t_{CH}$	CEN Hold time from RDN. WRN low	0			ns
$t_{RW}$	WRN, RDN pulse width (Low time)	110			ns
$t_{DD}$	Data valid after RDN low			90	ns
$t_{DA}$	RDN low to data bus active <sup>6</sup>	0			ns
$t_{DF}$	Data bus floating after RDN or CEN high			30	ns
$t_{DI}$	RDN or CEN high to data bus invalid <sup>7</sup>	0			ns
$t_{DS}$	Data bus setup time before WRN or CEN high (write cycle)	75			ns
$t_{DH}$	Data hold time after WRN high	8			ns
$t_{RWD}$	High time between read and/or write cycles <sup>5, 7</sup>	55			ns
<b>Port Timing<sup>5</sup> (See Figure 8)</b>					
$t_{PS}$	Port in setup time before RDN low (Read IP ports cycle)	0			ns
$t_{PH}$	Port in hold time after RDN high	0			ns
$t_{PD}$	OP port valid after WRN or CEN high (OPR write cycle)			110	ns
<b>Interrupt Timing (See Figure 10)</b>					
	INTRN (or OP3–OP7 when used as interrupts) negated from:				
	Read RxFIFO (RxRDY/FFULL interrupt)			100	ns
	Write TxFIFO (TxRDY interrupt)			100	ns
$t_{IR}$	Reset Command (delta break change interrupt)			100	ns
	Stop C/T command (Counter/timer interrupt)			100	ns
	Read IPCR (delta input port change interrupt)			100	ns
	Write IMR (Clear of change interrupt mask bit(s))			100	ns
<b>Clock Timing (See Figure 7)</b>					
$t_{CLK}$	X1/CLK high or low time	80			ns
$f_{CLK}$	X1/CLK frequency <sup>8</sup>	0.1	3.686	4	MHz
$f_{CTC}$	C/T Clk (IP2) high or low time (C/T external clock input)	55			ns
$f_{CTC}$	C/T Clk (IP2) frequency <sup>8</sup>	0		8	MHz
$t_{RX}$	RxC high or low time (16X)	30			ns
$f_{RX}$	RxC Frequency (16X)	0		16	MHz
	RxC Frequency (1x) <sup>8, 9</sup>	0		1	MHz
$t_{TX}$	TxC High or low time (16X)	30			ns
$f_{TX}$	TxC frequency (16X)			16	MHz
	TxC frequency (1X) <sup>8, 9</sup>	0		1	MHz

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
<b>Transmitter Timing, external clock (See Figure 11)</b>					
$t_{TXD}$	TxD output delay from TxC low (TxC input pin)			120	ns
$t_{TCS}$	Output delay from TxC output pin low to TxD data output	-30		30	ns
<b>Receiver Timing, external clock (See Figure 12)</b>					
$t_{RXS}$	RxD data setup time to RxC high	100			ns
$t_{RXH}$	RxD data hold time from RxC high	100			ns

**NOTES:**

- Parameters are valid over specified temperature range.
- All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4 V and 3.0 V with a transition time of 5 ns maximum. For X1/CLK this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input voltages of 0.8 V and 2.0 V and output voltages of 0.8 V and 2.0 V, as appropriate.
- Test conditions for outputs: CL = 150 pF, except interrupt outputs. Test conditions for interrupt outputs: CL = 50 pF, RL = 2.7 Kohm to V<sub>CC</sub>. Number 3 use 4.
- Typical values are at +25°C, typical supply voltages, and typical processing parameters.
- Timing is illustrated and referenced to the WRN and RDN Inputs. Also, CEN may be the "strobing" input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
- Guaranteed by characterization of sample units.
- If CEN is used as the "strobing" input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for tRWD to guarantee that any status register changes are valid.
- Minimum frequencies are not tested but are guaranteed by design.
- Clocks for 1X mode should be symmetrical.

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## AC CHARACTERISTICS (68XXX MODE)<sup>1, 2, 3</sup>

$V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise specified.

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ <sup>3</sup>	Max	
<b>Reset Timing</b>						
$t_{RES}$	4	RESET pulse width	200			ns
<b>Bus Timing<sup>5</sup></b>						
$t_{AS}$	5,6,7	A1–A4 setup time to CSN Low	10			ns
$t_{AH}$	5,6,7	A1–A4 hold time from CSN Low	45			ns
$t_{RWS}$	5,6,7	RWN setup time to CSN High	0			ns
$t_{RWH}$	5,6,7	RWN holdup time to CSN High	0			ns
$t_{CSW}^8$	5,6,7	CSN High pulse width	110			ns
$t_{CSD}^9$	5,6,7	CSN or IACKN High from DTACKN Low	20			ns
$t_{DD}$	5,6,7	Data valid from CSN or IACKN Low			175	ns
$t_{DA}^8$	5	RDN Low to data bus active	15			ns
$t_{DF}^8$	5,6,7	Data bus floating from CSN or IACKN High			125	ns
$t_{DI}^8$	5	RDN High to data bus invalid	20			ns
$t_{DS}$	5,6,7	Data setup time to CLK High	100			ns
$t_{DH}$	5,6,7	Data hold time from CSN High	0			ns
$t_{DAL}$	5,6,7	DTACKN Low from read data valid	0			ns
$t_{DCR}$	5,6,7	DTACKN Low (read cycle) from CLK High			125	ns
$t_{DCW}$	5,6,7	DTACKN Low (write cycle) form CLK High			125	ns
$t_{DAH}$	5,6,7	DTACKN High from CSN or IACKN High			100	ns
$t_{DAT}$	5,6,7	DTACKN High impedance from CSN or IACKN High			125	ns
$t_{CSC}^7$	5,6,7	CSN or IACKN setup time to clock High	90			ns
<b>Port Timing<sup>5</sup></b>						
$t_{PS}$	8	Port input setup time to CSN Low	0			ns
$t_{PH}$	8	Port input hold time from CSN High	0			ns
$t_{PD}$	8	Port output valid from CSN High			400	ns
<b>Interrupt Timing</b>						
$t_{IR}^{10}$	7	INTRN (or OP3–OP7 when used as interrupts) negated from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break interrupt) Stop C/T command (counter interrupt) Read IPCR (input port change interrupt) Write IMR (clear of interrupt mask bit)			100 100 100 100 100 100	ns ns ns ns ns ns
<b>Clock Timing</b>						
$t_{CLK}$	10	X1/CLK High or Low time	80			ns
$f_{CLK}^{11}$	10	X1/CLK frequency	0	3.6864	4	MHz
$t_{CTC}$	10	CTCLK (IP2) High or Low time	55			ns
$f_{CTC}^9$	10	CTCLK (IP2) frequency	100		4	MHz
$t_{RX}$	10	RxC High or Low time	50			ns
$f_{RX}^9$	10	RxC frequency (16X) (1X)	0.1 100		16 1	MHz MHz
$t_{TX}$	10	TxC High or Low time	50			ns
$f_{TX}^9$	10	TxC frequency (16X) (1X)	0 0		16 1	MHz MHz
<b>Transmitter Timing</b>						
$t_{TXD}$	11	TxD output delay from TxC external clock input on IP pin			350	ns
$t_{TCS}$	11	Output delay from TxC low at OP pin to TxD data output			150	ns
<b>Receiver Timing</b>						
$t_{RXS}$	12	RxD data setup time before RxC high at external clock input on IP pin	240			ns
$t_{RXH}$	12	RxD data hold time after RxC high at external clock input on IP pin	200			ns

### NOTES:

- Parameters are valid over specified temperature range.
- All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.

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3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs:  $C_L = 150\text{pF}$ , except interrupt outputs. Test condition for interrupt outputs:  $C_L = 50\text{pF}$ ,  $R_L = 2.7\text{k}\Omega$  to  $V_{CC}$ .
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
8. Guaranteed by characterization of sample units.
9. Minimum frequencies are not tested but are guaranteed by design.
10. 325ns maximum for  $T_A > 70^\circ\text{C}$ .
11. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.
12. See UART application note for power down currents less than 5 $\mu\text{A}$ .

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## Block Diagram

The SC28L92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

## Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

## Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

## Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer. When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration.

## FIFO Configuration

Each receiver and transmitter has a 16 byte FIFO. These FIFOs may be configured to operate at a fill capacity of either 8 or 16 bytes. This feature may be used if it is desired to operate the 28L92 in strict compliance with the 26C92. The 8 byte/16 byte mode is controlled by the MR0[3] bit. A 0 value for this bit sets the 8 bit mode (the default); a 1 sets the 16 byte mode.

The FIFO fill interrupt level automatically follow the programming of the MR0[3] bit. See tables 3 and 4.

## TIMING CIRCUITS

### Crystal Clock

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

### BRG

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud.

Programming bit 0 of MR0 to a "1" gives additional baud rates of 57.6kB, 115.2kB and 230.4kB. These will be in the 16X mode. A 3.6864 MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

## Counter/Timer (C/T)

The counter timer is a 16-bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor. The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR/CTUR Register descriptions.

## Communications Channels A and B

Each communications channel of the SC28L92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (Break, Framing and Parity Errors) are also FIFOed with each data character.

## Input Port

The inputs to this unlatched 7-bit (6-bit for 68xxx mode) port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25–50 ms, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4 KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25 ms (this assumes that the clock input is 3.6864 MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25 ms if the transition occurs "coincident with the first sample pulse". The 50  $\mu$ s time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25 ms later.



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## Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins drive a state which is the (pg. 9 start) complement of the Output Port Register (OPR). The OPR register is set and reset by writing to the SOPR and ROPR addresses. (See the description of the SOPR and ROPR registers). The output pins will drive the inverse data polarity of the OPR registers. The OPCR register conditions these output pins to be controlled by the OPR or by other signals in the chip. Output ports are driven high on hardware reset.

## OPERATION

### Transmitter

The SC28L92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC28L92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPT bits will be set in the status register. When a character is loaded to the transmit FIFO the TxEMPT bit will be reset. The TxEMPT will not set until: 1) the transmit FIFO is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit FIFO, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the TxFIFO while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the TxFIFO.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command. The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS option is enabled (MR2[4] = 1), the CTS input at IP0 or IP1 must be Low in order for the character to be transmitted. The transmitter will check the state of the CTS input at the beginning of each character transmitted. If it is found to be High, the transmitter will delay the transmission of any following characters until the CTS has returned to the low state. CTS going high during the serialization of a character will not affect that character.

The transmitter can also control the RTSN outputs, OP0 or OP1 via MR2[5]. When this mode of operation is set, the meaning of the OP0 or OP1 signals will usually be 'end of message'. See description of the MR2[5] bit for more detail.

### Receiver

The SC28L92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive FIFO and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the Rx FIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the Rx FIFO and the received break bit in the SR is set to 1. The RxD input must return to high for two (2) clock edges of the X1 crystal clock for the receiver to recognize the end of the break condition and begin the search for a start bit.

**This will usually require a high time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock.**

### Receiver FIFO

The Rx FIFO consists of a First-In-First-Out (FIFO) stack with a capacity of 8 or 16 characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all 8 or 16 stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the Rx FIFO outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

### Receiver Status Bits

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the Rx FIFO is read. Therefore the status register should be read prior to reading the FIFO.

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If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

## Receiver Reset and Disable

Receiver disable stops the receiver immediately—data being assembled in the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers.

A 'watchdog timer' is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is to alert the control processor that characters are in the RxFIFO which have not been read and/or the data stream has stopped. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the receiver shift register to the RxFIFO or a read of the RxFIFO is executed.

## Receiver Time-out Mode

In addition to the watch dog timer described in the receiver section, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time out intervals.

The time-out mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the RxFIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data

during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

The time-out mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the time-out mode for that channel. Writing a 'Cx' to CRA or CRB will disable the time-out mode. The time-out mode should only be used by one channel at once, since it uses the C/T. If, however, the time-out mode is enabled from both receivers, the time-out will occur only when **both** receivers have stopped receiving data for the time-out period. CTU and CTL must be loaded with a value greater than the normal receive character period. The time-out mode disables the regular START/STOP Counter commands and puts the ca/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Time-out Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

## Time Out Mode Caution

When operating in the special time out mode, it is possible to generate what appears to be a "false interrupt", i.e., an interrupt without a cause. This may result when a time-out interrupt occurs and then, BEFORE the interrupt is serviced, another character is received, i.e., the data stream has started again. (The interrupt latency is longer than the pause in the data stream.) In this case, when a new character has been received, the counter/timer will be restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR will show the "Counter Ready" bit not set. If nothing else is interrupting, this read of the ISR will return a x'00 character.

## Multi-drop Mode (9-bit or Wake-Up)

The DUART is equipped with a wake up mode for multi-drop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while

MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the TxFIFO.



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In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RxFIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RxFIFO. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

## PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has 3 mode registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register "Miscellaneous Commands". Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Philips Semiconductors UART software.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

**Table 1. SC28L92 register addressing READ (RDN = 0), WRITE (WRN = 0)**

0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RxFIFOA)	Tx Holding Register A (TxFIFOA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Preset Register (CTPU)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Preset Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RxFIFOB)	Tx Holding Register B (TxFIFOB)
1	1	0	0	Interrupt vector (68K mode)	Interrupt vector (68K mode)
1	1	0	0	General purpose register (Intel mode)	General purpose register (Intel mode)
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command (SOPR)
1	1	1	1	Stop Counter Command	Reset output Port Bits Command (ROPR)

**NOTE:**

1. The three MR registers are accessed via the MR Pointer and Commands 0x1n and 0xBn (where n = represents receiver and transmitter enable bits)

The following named registers are the same for Channels A and B				
Mode	Register	MRnA	MRnB	R/W
Status	Register	SRA	SRB	R only
Clock	Select	CSRA	CSRB	W only
Command	Register	CRA	CRB	W only
Receiver	FIFO	RxFIFOA	RxFIFOB	R only
Transmitter	FIFO	TxFIFOA	TxFIFOB	W only

These are support functions for both Channels		
Register Name	Register	R/W
Input Port Change Register	IPCR	R
Auxiliary Control Register	ACR	W
Interrupt Status Register	ISR	R
Interrupt Mask Register	IMR	W
Counter Timer Upper Value	CTU	R
Counter Timer Lower Value	CTL	R
Counter Timer Preset Upper	CTPU	W
Counter Timer Preset Lower	CTPL	W
Input Port Register	IPR	R
Output Configuration Register	OPCR	W
Set Output Port	Bits	W
Reset Output Port	Bits	W

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**Table 2. Register bit formats**

**MR0 – MODE REGISTER 0**

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR0	WATCHDOG	RxINT BIT 2		TxINT (1:0)	FIFO SIZE	BAUD RATE EXTENDED II	TEST 2	BAUD RATE EXTENDED 1

**MR1 – MODE REGISTER 1**

Bit 7	Bit 6	Bit 5	Bit 4:3	Bit 2	Bit 1:0
RxRTS Control	ISR Read Mode	Error Mode	Parity Mode	Parity Type	Bits per Character

**MR2 – MODE REGISTER 2**

Bits 7:6	Bit 5	Bit 4	Bit 3:2	Bit 1:0
Channel Mode	TxRTS Control	CTSN Enable Tx	RxINT	Stop Length

**CSR – CLOCK SELECT REGISTER**

Bits 7:4	Bits 43:0
Receiver Clock, Select Code	Transmitter Clock select code,

**CR –COMMAND REGISTER**

Bits 7:4	Bit 3	Bit 2	Bit 1	Bit 0
Channel Command codes	Disable Tx	Enable Tx	Enable Tx	Enable Rx

**SR – CHANNEL STATUS REGISTER**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Received Break	Framing Error	Parity Error	Overrun Error	TxE <sub>MT</sub>	TxRDY	RxFULL	RxRDY

**IMR – INTERRUPT MASK REGISTER (ENABLES INTERRUPTS)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change Input Port	Change Break B	RxRDY B	TxRDYB	Counter Ready	Change Break A	RxRDY A	TxRDY A

**ISR – INTERRUPT STATUS REGISTER**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change Input Port	Change Break B	RxRDY B	TxRDYB	Counter Ready	Change Break A	RxRDY A	TxRDY A

**CTPU – COUNTER TIMER PRESET REGISTERS, UPPER**

Bits 7:0
8 MSB of the BRG Timer divisor.

**CTPL – COUNTER TIMER PRESET REGISTER, LOWER**

Bits 7:0
8 LSB of the BRG Timer divisor.

**ACR – COUNTER TIMER PRESET REGISTER**

Bit 7	Bit 6:4	Bit 3	Bit 2	Bit 1	Bit 0
Baud Group	Counter Timer mode and clock select	Enable IP3	Enable IP2	Enable IP1	Enable IP0

**IPCR – INPUT PORT CHANGE REGISTER**

Bit 7	Bit 6:4	Bit 3	Bit 2	Bit 1	Bit 0
Baud Group	Counter Timer mode and clock select	Enable IP3	Enable IP2	Enable IP1	Enable IP0

**IPR – INPUT PORT REGISTER**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
State of IP	State of IP 6	State of IP 5	State of IP 4	State of IP 3	State of IP 2	State of IP 1	State of IP 0

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## REGISTER DESCRIPTIONS Mode Registers

### MR0a

MR0 Mode Register 0 MR0 is accessed by setting the MR pointer to 0 via the command register command B.

	Bit 7	BIT 6	BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>MR0A</b> <b>MR0B</b> MR0B[3:0] are reserved	<b>Rx WATCHDOG</b> 0 = Disable 1 = Enable	<b>RxINT BIT 2</b> See Tables in MR0 description	<b>TxINT (1:0)</b> See table #4	<b>FIFO SIZE</b> 0 = 8 byte FIFO 1 = 16 byte FIFO	<b>BAUD RATE EXTENDED II</b> 0 = Normal 1 = Extend II	<b>TEST 2</b> Set to 0	<b>BAUD RATE EXTENDED I</b> 0 = Normal 1 = Extend

**MR0[7]**—This bit controls the receiver watch dog timer. 0 = disable, 1 = enable. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the Rx FIFO that has not been read. This situation may occur when the byte count of the last part of a message is not large enough to generate an interrupt.

**MR0[6]**—Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the FIFO that generates the receiver interrupt.

**MR0[6] MR1[6]** Note that this control is split between MR0 and MR1. This is for backward compatibility to the SC2692 and SCN2681.

**Table 3. Receiver FIFO interrupt fill level (MR0(3) = 0)**

MR0[6] MR1[6]	Interrupt Condition
00	1 or more bytes in FIFO (Rx RDY)
01	3 or more bytes in FIFO
10	6 or more bytes in FIFO
11	8 bytes in FIFO (Rx FULL)

**Table 3a. Receiver FIFO interrupt fill level(MR0(3)=1)**

MR0[6] MR1[6]	Interrupt Condition
00	1 or more bytes in FIFO (Rx RDY)
01	8 or more bytes in FIFO
10	12 or more bytes in FIFO
11	16 bytes in FIFO (Rx FULL)

For the receiver these bits control the number of FIFO positions filled when the receiver will attempt to interrupt. After the reset the receiver FIFO is empty. The default setting of these bits cause the receiver to attempt to interrupt when it has one or more bytes in it.

**MR0[5:4]**—Tx interrupt fill level.

**Table 4. Transmitter FIFO interrupt fill level MR0(3) = 0**

MR0[5:4]	Interrupt Condition
00	8 bytes empty (Tx EMPTY)
01	4 or more bytes empty
10	6 or more bytes empty
11	1 or more bytes empty (Tx RDY)

**Table 4a. Transmitter FIFO interrupt fill level MR0(3) = 1**

MR0[5:4]	Interrupt Condition
00	16 bytes empty (Tx EMPTY)
01	8 or more bytes empty
10	12 or more bytes empty
11	1 or more bytes empty (Tx RDY)

For the transmitter these bits control the number of FIFO positions empty when the transmitter will attempt to interrupt. After the reset the transmit FIFO has 8 bytes empty. It will then attempt to interrupt as soon as the transmitter is enabled. The default setting of the MR0 bits (5:4) condition the transmitter to attempt to interrupt only when it is completely empty. As soon as one byte is loaded, it is no longer empty and hence will withdraw its interrupt request.

**MR0[3]**—Selects the FIFO depth at 8 or 16 bytes. See Tables 3 and 4

**MR0[2:0]**—These bits are used to select one of the six baud rate groups.

See Table 5 for the group organization.

- 000 Normal mode
- 001 Extended mode I
- 100 Extended mode II

Other combinations of MR2[2:0] should not be used

**Note:** MR0[3:0] are not used in channel B and should be set to 0.

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## MR1A

MR1 Mode Register 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Rx CONTROLS RTS	RxINT BIT 1	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHARACTER	
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multi-drop Mode		0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8	

**NOTE:**

In block error mode, block error conditions must be cleared by using the error reset command (command 4x) or a receiver reset.

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CR command 1. After reading or writing MR1A, the pointer will point to MR2A.

**MR1A[7]—Channel A Receiver Request-to-Send Control (Flow Control)**

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0].

MR1A[7] = 1 causes RTSAN to be negated (OP0 is driven to a '1' [VCC]) upon receipt of a valid start bit if the Channel A FIFO is full. This is the beginning of the reception of the ninth byte. If the FIFO is not read before the start of the tenth byte, an overrun condition will occur and the tenth byte will be lost. However, the bit in OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

**MR1[6]**—Bit 1 of the receiver interrupt control. See description under MR0[6].

**MR1A[5]—Channel A Error Mode Select**

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block'

mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

**MR1A[4:3]—Channel A Parity Mode Select**

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multi-drop mode described in the Operation section.

**MR1A[2]—Channel A Parity Type Select**

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multi-drop mode it selects the polarity of the A/D bit.

**MR1A[1:0]—Channel A Bits Per Character Select**

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

**MR2A—Channel A Mode Register 2**

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

## MR2 MODE REGISTER 2

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE		Tx CONTROLS RTS	CTS ENABLE Tx	STOP BIT LENGTH NOTE: Add 0.5 to binary codes 0–7 for 5 bit character lengths.			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop		0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

**NOTE:**

Add 0.5 to values shown for 0–7 if channel is programmed for 5 bits/char.

**MR2A[7:6]—Channel A Mode Select**

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently.

MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is relocked and retransmitted on the TxDA output.

2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.

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6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loop back mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loop back mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA out-put.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of auto echo or remote loop back modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in auto echo by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in auto echo mode until the entire stop has been re-transmitted.

**MR2A[5]—Channel A Transmitter Request-to-Send Control** This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the Tx FIFO, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled.

This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A Tx FIFO.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

**MR2A[4]—Channel A Clear-to-Send Control** If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

**MR2A[3:0]—Channel A Stop Bit Length Select** This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the stop bit position (one bit time after the last data bit, or after the parity bit if enabled is sampled).

If an external 1X clock is used for the transmitter,

MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

## MR0B—Channel B Mode Register 0

MR0B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR0 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR0B, the pointer will point to MR1B.

The bit definitions for this register are identical to MR0A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs. MR0B[3:0] are reserved.

## MR1B—Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## MR2B—Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

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## CSRA—Channel A Clock Select Register

### CSRA[7:4]—Channel A Receiver Clock Select

This field selects the baud rate clock for the Channel A receiver. The field definition is shown in Table 5.

### CSR CLOCK SELECT REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSRA CSRB	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	See Text and table 5				See Text and table 5			

**Table 5.** Baud rate (base on a 3.6864MHz crystal clock)

CSRA[7:4]	MR0[0] = 0 (Normal Mode)		MR0[0] = 1 (Extended Mode I)		MR0[2] = 1 (Extended Mode II)	
	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	300	450	4,800	7,200
0001	110	110	110	110	880	880
0010	134.5	134.5	134.5	134.5	1,076	1,076
0011	200	150	1200	900	19.2K	14.4K
0100	300	300	1800	1800	28.8K	28.8K
0101	600	600	3600	3600	57.6K	57.6K
0110	1,200	1,200	7200	7,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1001	4,800	4,800	28.8K	28.8K	4,800	4,800
1010	7,200	1,800	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	57.6K	57.6K	9,600	9,600
1100	38.4K	19.2K	230.4K	115.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer	Timer	Timer
1110	IP4–16X	IP4–16X	IP4–16X	IP4–16X	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X	IP4–1X	IP4–1X	IP4–1X	IP4–1X

**NOTE:**

The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

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**Table 6. Bit rate generator characteristics**

Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (KHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

**NOTE:**

Duty cycle of 16X clock is 50% ± 1%

**CSRA[3:0]—Channel A Transmitter Clock Select**

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 5, except as follows:

CSRA[3:0]	
1110	1111
IP3-16X	IP3-1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

**CSRB—Channel B Clock Select Register**

**CSRB[7:4]—Channel B Receiver Clock Select**

This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 5, except as follows:

CSRB[7:4]	
1110	1111
IP6-1X	IP6-16X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

**CSRB[3:0]—Channel B Transmitter Clock Select**

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 5, except as follows:

CSRB[3:0]	
1110	1111
IP5-1X	IP5-16X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.



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## CRA—Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

### CR COMMAND REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB	MISCELLANEOUS COMMANDS				Disable Tx	Enable Tx	Disable Rx	Enable Rx
	See Text of Channel Command Register				1 = Yes 0 = No	1 = Yes 0 = No	1 = Yes 0 = No	1 = Yes 0 = No

#### NOTES:

Access to the miscellaneous commands should be separated by 3 X1 clock edges. A disabled transmitter cannot be loaded.

#### CRA[7:4]—Miscellaneous Commands

Execution of the commands in the upper four bits of this register must be separated by 3 X1 clock edges. Other reads or writes (including writes to the lower four bits) may be inserted to achieve this separation.

#### CRA[7:4]—Commands

0000	No command.	1010	Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset. (See also Watchdog timer description in the receiver section.)
0001	Reset MR pointer. Causes the Channel A MR pointer to point to MR1.	1011	Set MR pointer to '0'
0010	Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.	1100	Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued to force a reset of the ISR(3) bit
0011	Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.	1101	Not used.
0100	Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.	1110	Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.
0101	Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero	1111	Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only. For maximum power reduction input pins should be at V <sub>SS</sub> or V <sub>DD</sub> .
0110	Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the Tx FIFO, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.		
0111	Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.		
1000	Assert RTSN. Causes the RTSN output to be asserted (Low).		
1001	Negate RTSN. Causes the RTSN output to be negated (High)		

#### CRA[3]—Disable Channel A Transmitter

This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the Tx FIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

#### CRA[2]—Enable Channel A Transmitter

Enables operation of the Channel A transmitter. The TxRDY and TxEMT status bits will be asserted if the transmitter is idle.



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**CRA[1]—Disable Channel A Receiver**

This command terminates operation of the receiver immediately—a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multi-drop mode is programmed, the receiver operates even if it is disabled. See Operation section.

**CRA[0]—Enable Channel A Receiver**

Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

**CRB—Channel B Command Register**

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of commands "Ex" and "Fx" which are used for power down mode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

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## SRA—Channel A Status Register SR STATUS REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>SRA SRB</b>	<b>RECEIVED BREAK*</b>	<b>FRAMING ERROR*</b>	<b>PARITY ERROR*</b>	<b>OVERRUN ERROR</b>	<b>TxE<sub>MT</sub></b>	<b>TxRDY</b>	<b>FFULL</b>	<b>RxRDY</b>
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

\*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a “reset error status” command. In character mode they are discarded when the corresponding data character is read from the FIFO. In block error mode, the error-reset command (command 4x or receiver reset) must be used to clear block error conditions

**SRA[7]—Channel A Received Break** This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time two successive edges of the internal or external 1X clock. **This will usually require a high time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock.**

When this bit is set, the Channel A ‘change in break’ bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

This bit is reset by command 4 (0100) written to the command register or by receiver reset.

### SRA[6]—Channel A Framing Error

This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

### SRA[5]—Channel A Parity Error

This bit is set when the ‘with parity’ or ‘force parity’ mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multi-drop mode the parity error bit stores the receive A/D (Address/Data) bit.

### SRA[4]—Channel A Overrun Error

This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a ‘reset error status’ command.

### SRA[3]—Channel A Transmitter Empty (TxEMTA)

This bit will be set when the transmitter under runs, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the under run condition.

### SRA[2]—Channel A Transmitter Ready (TxRDYA)

This bit, when set, indicates that the transmit FIFO is not full and ready to be loaded with another character. This bit is cleared when the transmit FIFO is loaded by the CPU and there are (after this load) no more empty locations in the FIFO. It is set when a character is transferred to the transmit shift register. TxRDYA is reset when the transmitter is disabled and is set when the

transmitter is first enabled. Characters loaded to the Tx FIFO while this bit is 0 will be lost. This bit has different meaning from ISR[0].

### SRA[1]—Channel A FIFO Full (FFULLA)

This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the receive FIFO. If a character is waiting in the receive shift register because the FIFO is full, FFULLA will not be reset when the CPU reads the receive FIFO. This bit has different meaning from ISR1 when MR1 6 is programmed to a ‘1’.

### SRA[0]—Channel A Receiver Ready (RxRDYA)

This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receive FIFO, only if (after this read) there are no more characters in the FIFO.

## SRB—Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

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## OPCR—Output Port Configuration Register OPCR OUTPUT PORT CONFIGURATION REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0 = OPR[7] 1 = TxRDY B	0 = OPR[6] 1 = TxRDY A	0 = OPR[5] 1 = RxRDY/FFULL B	0 = OPR[4] 1 = RxRDY/FFULL A	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)		00 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)	

### OPCR[7]—OP7 Output Select

This bit programs the OP7 output to provide one of the following:

- 0 The complement of OPR[7].
- 1 The Channel B transmitter interrupt output which is the complement of ISR[4]. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[6]—OP6 Output Select

This bit programs the OP6 output to provide one of the following:

- 0 The complement of OPR[6].
- 1 The Channel A transmitter interrupt output which is the complement of ISR[0]. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[5]—OP5 Output Select

This bit programs the OP5 output to provide one of the following:

- 0 The complement of OPR[5].
- 1 The Channel B receiver interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[4]—OP4 Output Select

This field programs the OP4 output to provide one of the following:

- 0 The complement of OPR[4].
- 1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[3:2]—OP3 Output Select

This bit programs the OP3 output to provide one of the following:

- 00 The complement of OPR[3].
- 01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- 10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- 11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

### OPCR[1:0]—OP2 Output Select

This field programs the OP2 output to provide one of the following:

- 00 The complement of OPR[2].
- 01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- 10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- 11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

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## SOPR—Set the Output Port Bits (OPR)

SOPR[7:0]—Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect. This allows software to set individual bits with our keeping a copy of the OPR bit configuration.

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0
<b>Set OPR Bits</b>	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change

## ROPR—Reset Output Port Bits (OPR)

ROPR[7:0]—Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect. This allows software to reset individual bits with our keeping a copy of the OPR bit configuration.

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0
<b>Reset OPR Bits</b>	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change

## OPR Output Port Register

The output pins (OP pins) drive the compliment of the data written to this register.

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0
<b>OPR</b>	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low

## ACR Auxiliary Control Register

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	<b>BRG SET Select</b>	<b>Counter Timer Mode Mode and clock sour select</b>			<b>Delta IP3 int enable</b>	<b>Delta IP3 int enable</b>	<b>Delta IP3 int enable</b>	<b>Delta IP3 int enable</b>
<b>ACR</b>	0 = set 1 1 = set 2	See table 7			0 = off 1 = enabled	0 = off 1 = enabled	0 = off 1 = enabled	0 = off 1 = enabled

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# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## ACR—Auxiliary Control Register

### ACR[7]—Baud Rate Generator Set Select

This bit selects one of two sets of baud rates to be generated by the BRG (see Table 5).

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB.

Baud rate generator characteristics are given in Table 6.

### ACR[6:4]—Counter/Timer Mode And Clock Source Select

This field selects the operating mode of the counter/timer and its clock source as shown in Table 7

### ACR [3:0]—IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable

This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR [7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR [7], which results in the generation of an interrupt output if IMR [7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR [7].

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**Table 7. ACR 6:4 field definition**

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA - 1X clock of Channel A transmitter
010	Counter	TxCB - 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

**NOTE:**

The timer mode generates a square wave

### IPCR INPUT PORT CONFIGURATION REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>IPCR</b>	<b>Delta IP3</b>	<b>Delta IP3</b>	<b>Delta IP3</b>	<b>Delta IP3</b>	<b>IP 3</b>	<b>IP 2</b>	<b>IP 1</b>	<b>IP 0</b>
	0 = no change 1 = change	0 = no change 1 = change	0 = no change 1 = change	0 = no change 1 = change	0 = low 1 = High	0 = low 1 = High	0 = low 1 = High	0 = low 1 = High

**IPCR [7:4]—IP3, IP2, IP1, IP0 Change-of-State**

These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR [7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

**IPCR [3:0]—IP3, IP2, IP1, IP0 Change-of-State**

These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## ISR—Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR - the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to H'00' when the DUART is reset.

### ISR INTERRUPT STATUS REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR	INPPUT PORT CHANGE	DELTA Break B	RxRDY/ FFULL B	TxRDY B	Counter Ready	Delta Break A	RxRDY/ FFULL A	TxRDY A
	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled

#### ISR[7]—Input Port Change Status

This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

#### ISR[6]—Channel B Change In Break

This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

#### ISR[5]—RxB Interrupt

This bit indicates that the channel B receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

#### ISR[4]—TxB Interrupt

This bit indicates that the channel B transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

#### ISR[3]—Counter Ready.

In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

#### ISR[2]—Channel A Change in Break

This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

#### ISR[1]—RxA Interrupt

This bit indicates that the channel A receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

#### ISR[0]—TxA Interrupt

This bit indicates that the channel A transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

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## IMR—Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

### IMR INTERRUPT MASK REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR	INPPUT PORT CHANGE	Delta Break B	RxRDY/ FFULL B	TxRDY B	Counter Ready	Delta Break A	RxRDY/ FFULL A	TxRDY A
INTERRUPT	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled

## CTPU and CTPL – Counter/Timer Registers

### CTPU COUNTER TIMER PRESET UPPER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTPU	The lower eight (8) bits for the 16 bit counter timer preset register							

### CTPL COUNTER -TIMER PRESET LOW

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTPL	The Upper eight (8) bits for the 16 bit counter timer preset register							

The CTPU and CTPL hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTPU/CTPL registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer mode, the C/T generates a square wave whose period is twice the value (in C/T clock periods) of the CTPU and CTPL. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTPU and CTPL for a particular 1X data clock is shown below.

$$n = (\text{C/T Clock Frequency}) \text{ divided by } (2 \times 16 \times \text{Baud rate desired})$$

$$n = (\text{C/T Clock Frequency}) / (2 \times 16 \times \text{Baud rate desired})$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

If the value in CTPU and CTPL is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTPU and CTPL.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output. In the counter mode, the value C/T loaded into CTPU and CTPL by the CPU is counted down to 0.. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set.

The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTPU and CTPL at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTPU and CTPL.

When the C/T clock divided by 16 is selected, the maximum divisor becomes 1,048,575.

## Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register (except the 2681 and 68681) The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V ss).



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one ( $V_{DD}$ ).

### The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB. RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the ninth character is sensed. Transmission then stops with nine valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter. MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be.

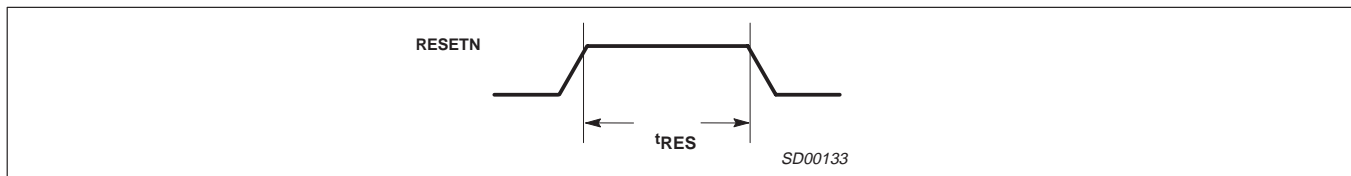


Figure 2. Reset Timing (80XXX mode)

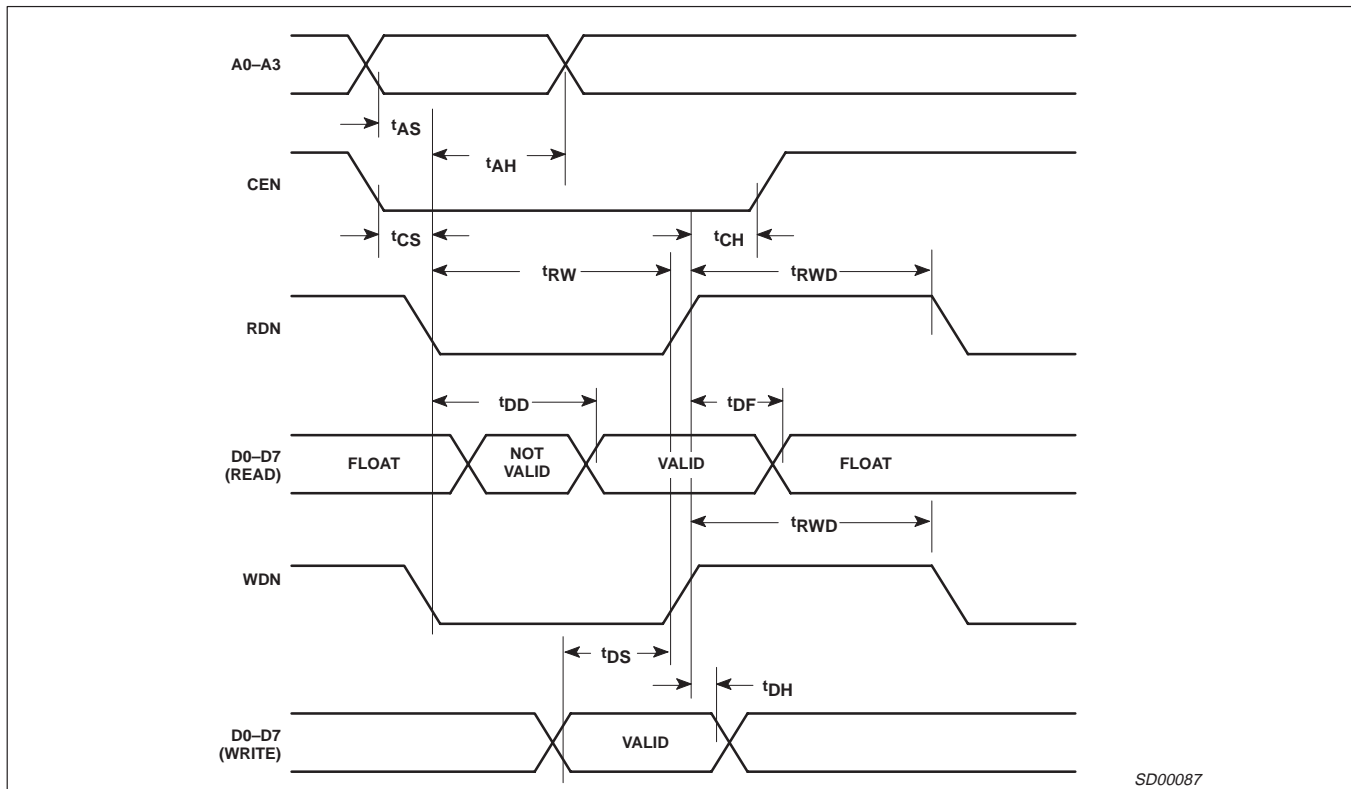


Figure 3. Bus Timing (80XXX mode)

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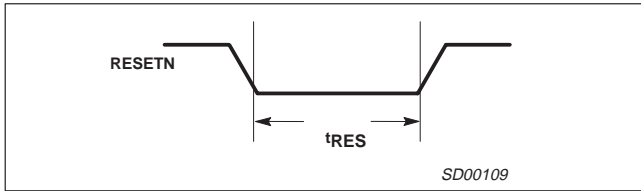


Figure 4. Reset Timing (68XXX mode)

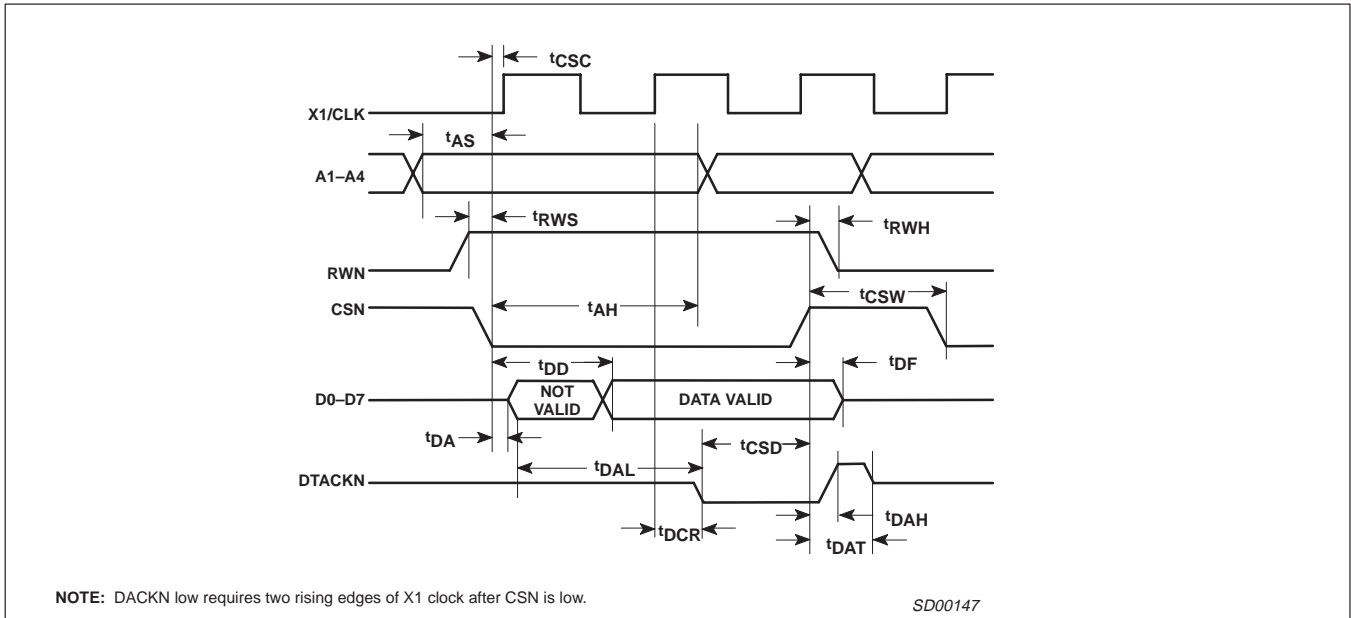


Figure 5. Bus Timing (Read Cycle) (68XXX mode)

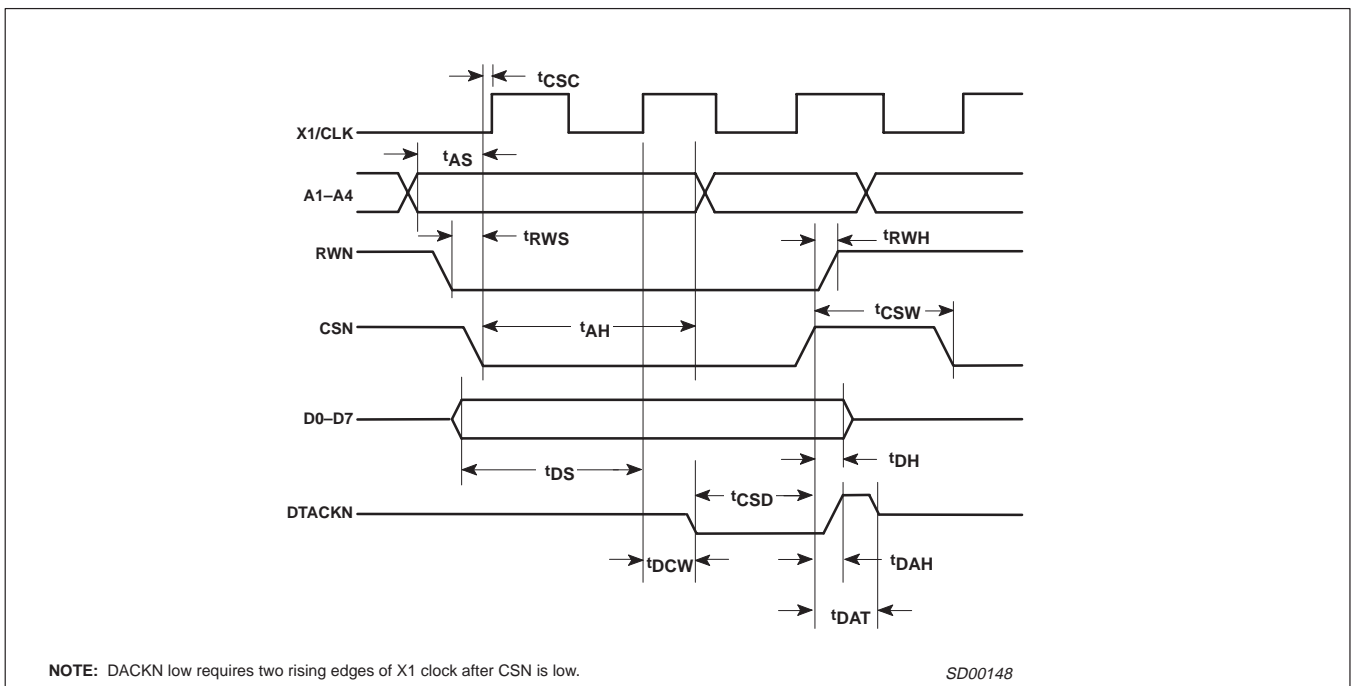


Figure 6. Bus Timing (Write Cycle) (68XXX mode)

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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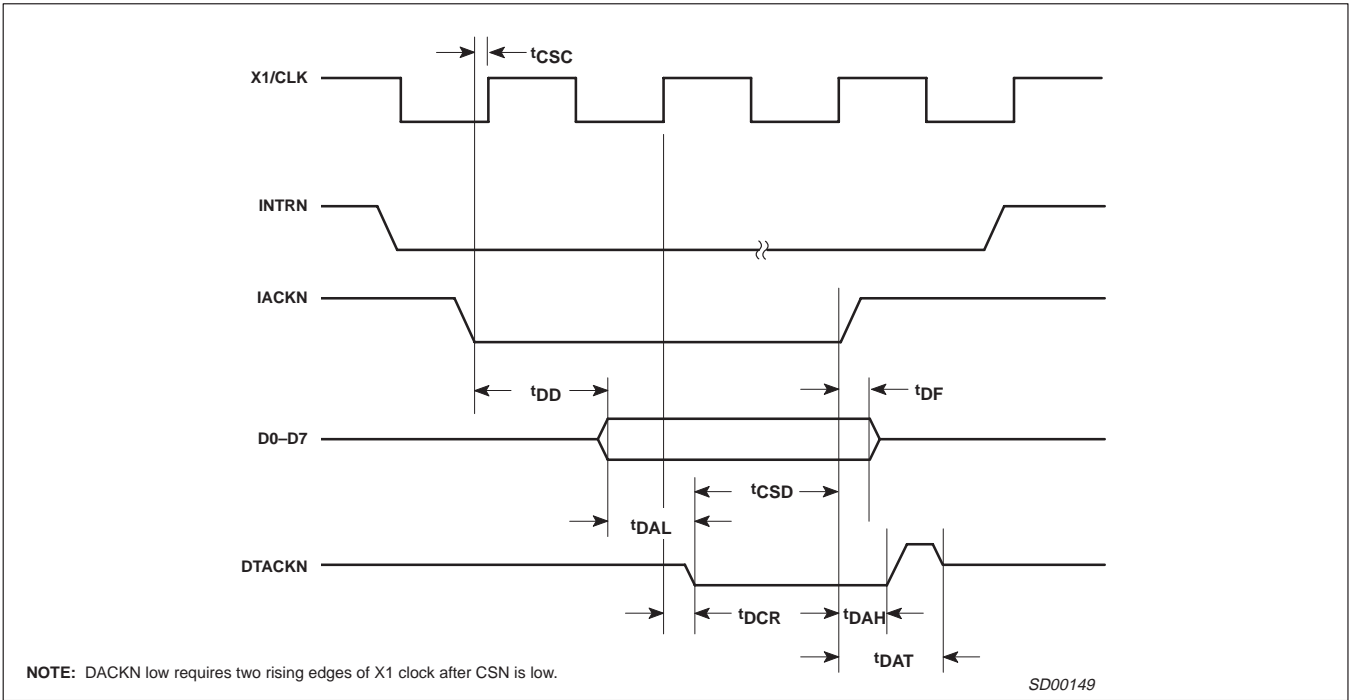


Figure 7. Interrupt Cycle Timing (68XXX mode)

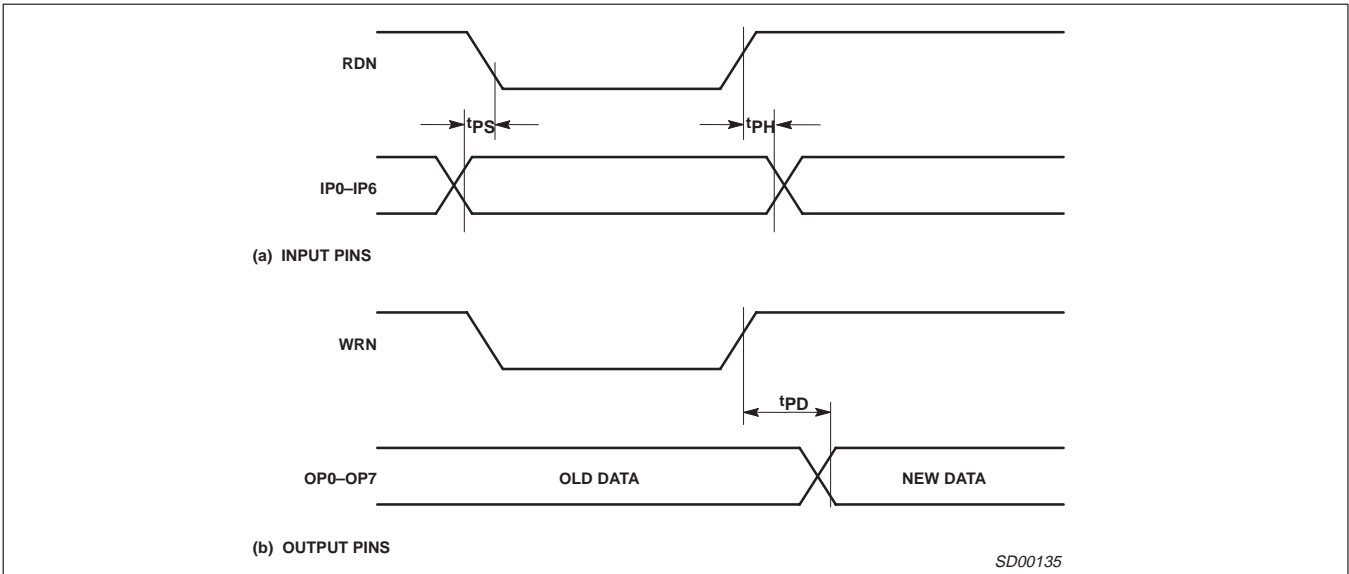


Figure 8. Port Timing

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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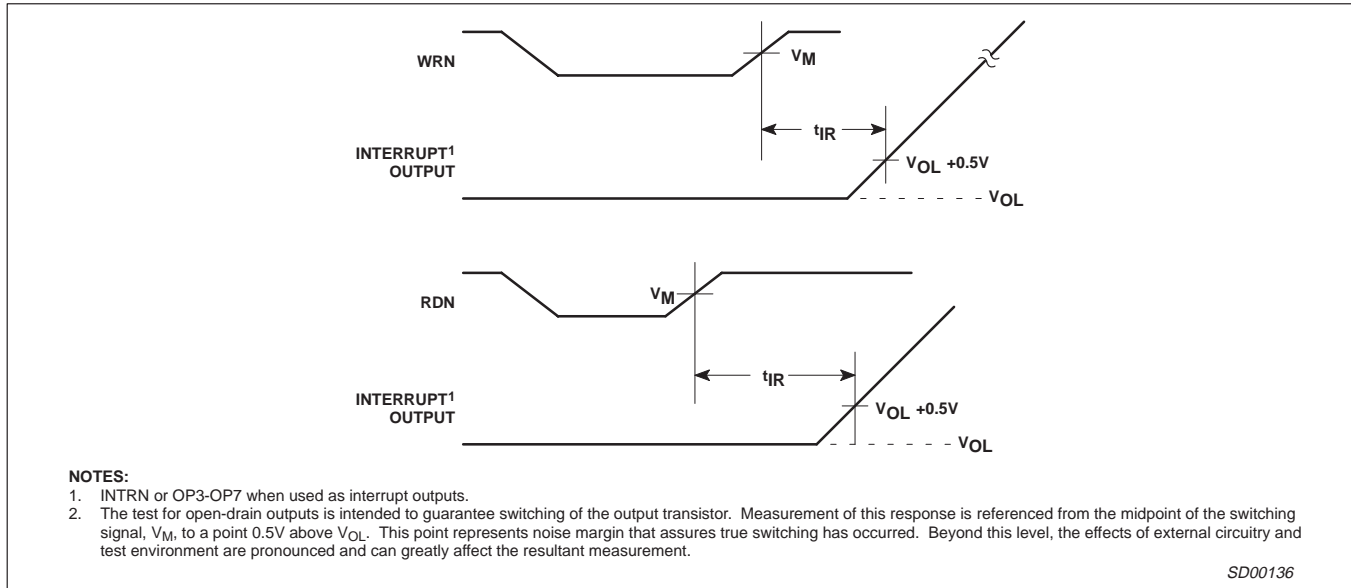


Figure 9. Interrupt Timing (80xxx mode)

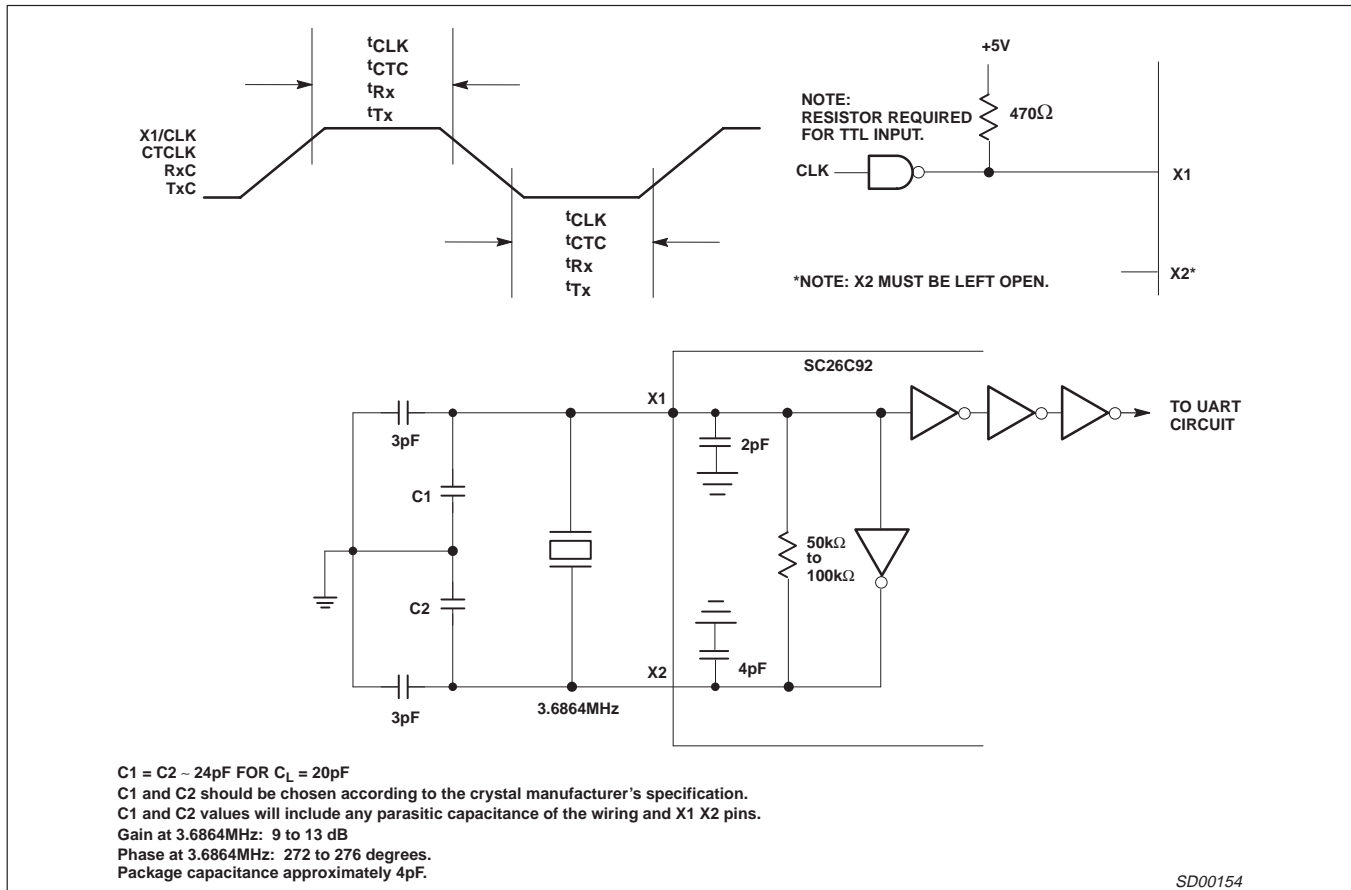


Figure 10. Clock Timing

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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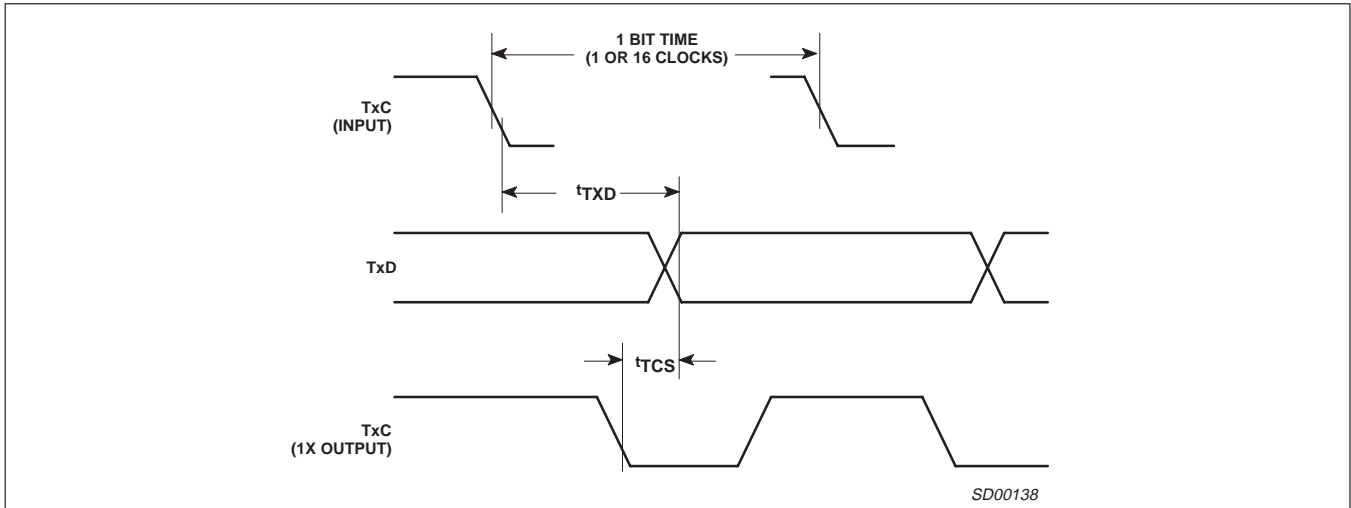


Figure 11. Transmitter External Clocks

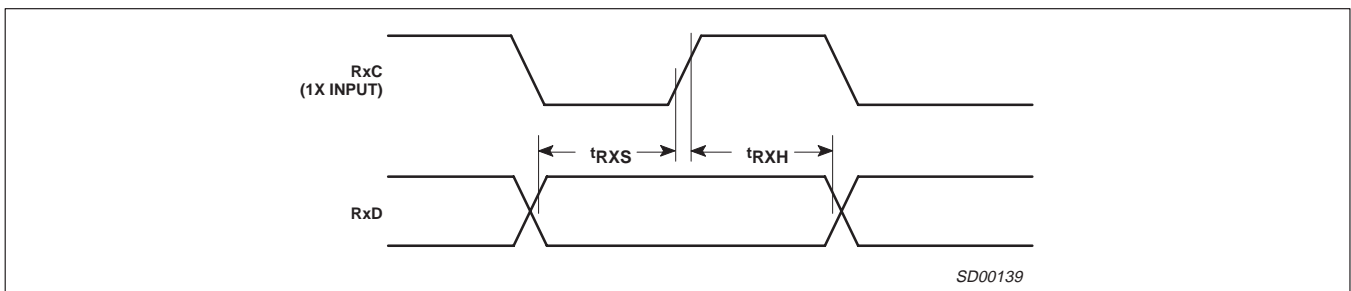
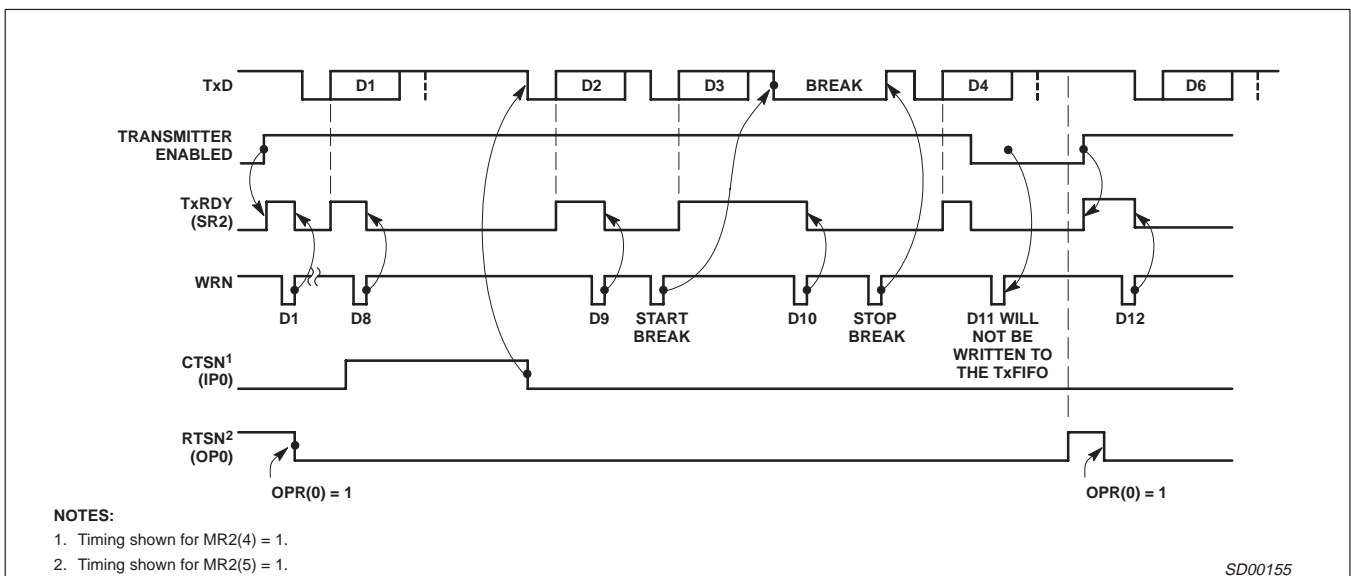


Figure 12. Receiver External Clock



- NOTES:
1. Timing shown for MR2(4) = 1.
  2. Timing shown for MR2(5) = 1.

Figure 13. Transmitter Timing

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# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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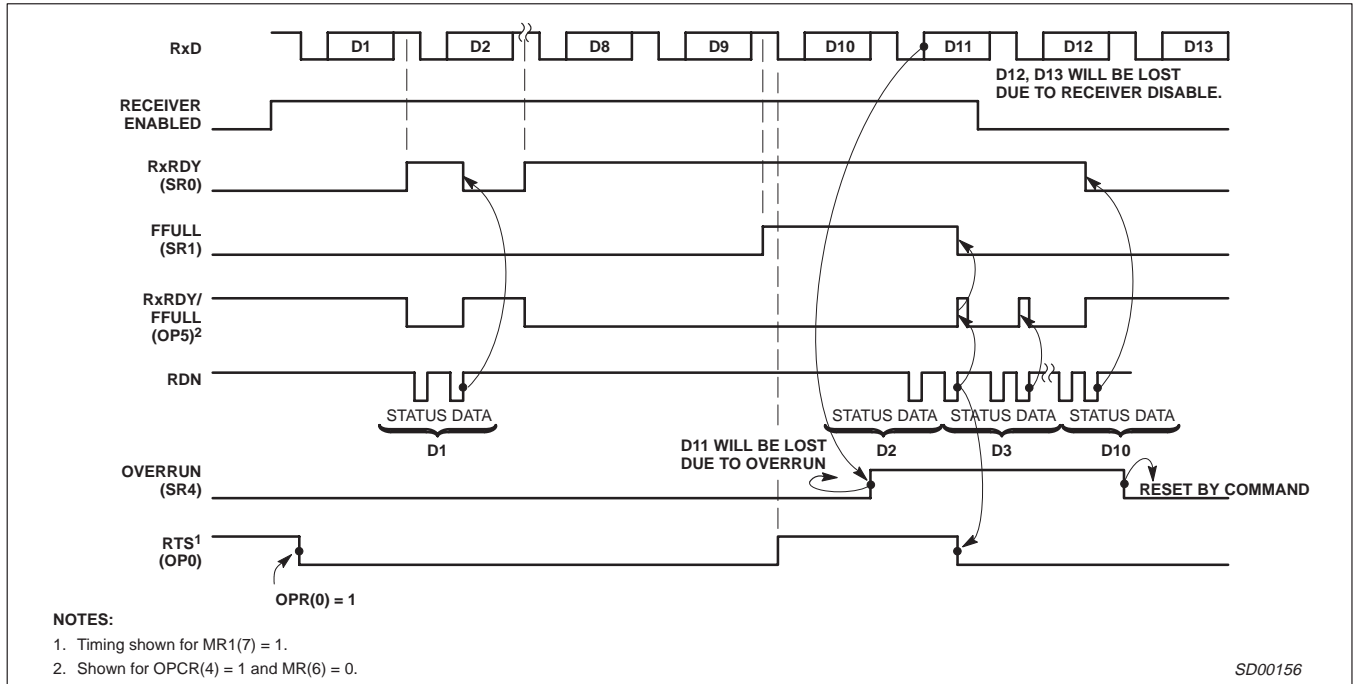


Figure 14. Receiver Timing

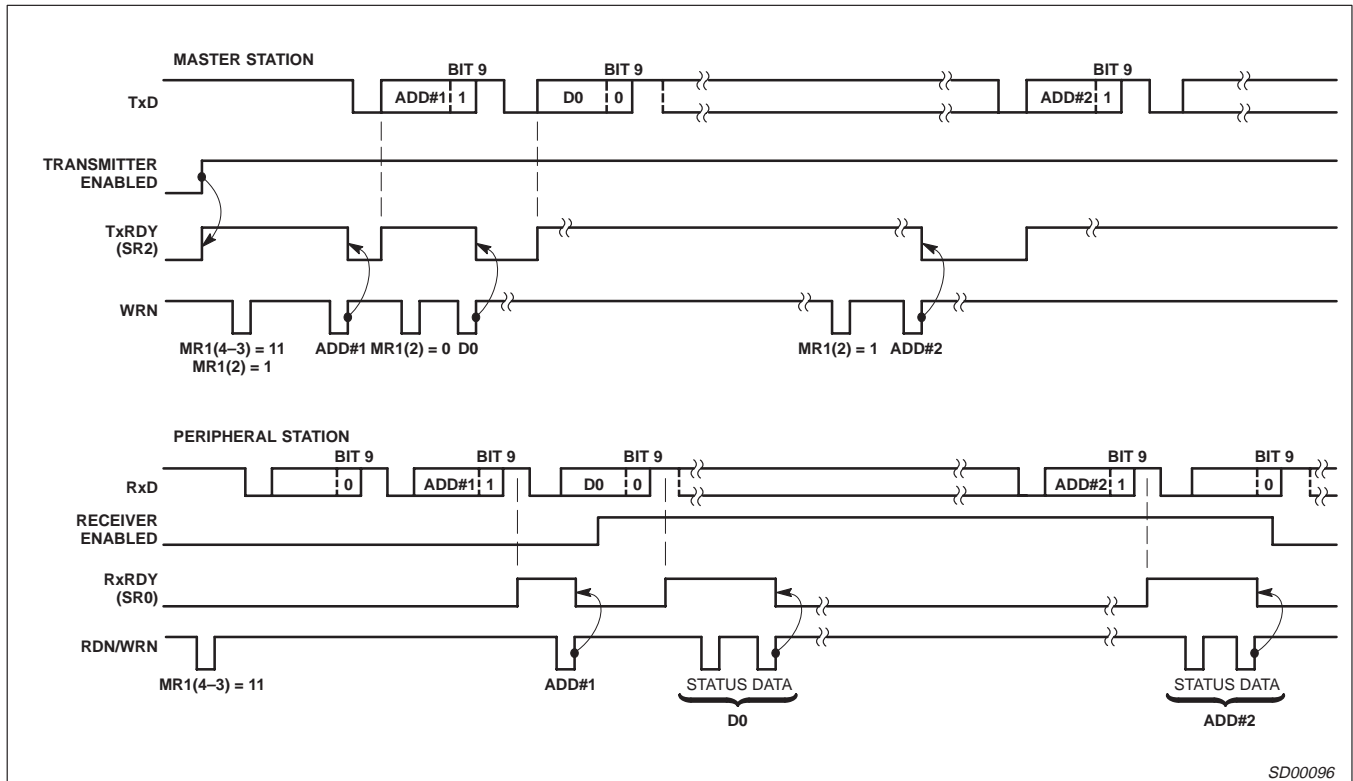


Figure 15. Wake-Up Mode

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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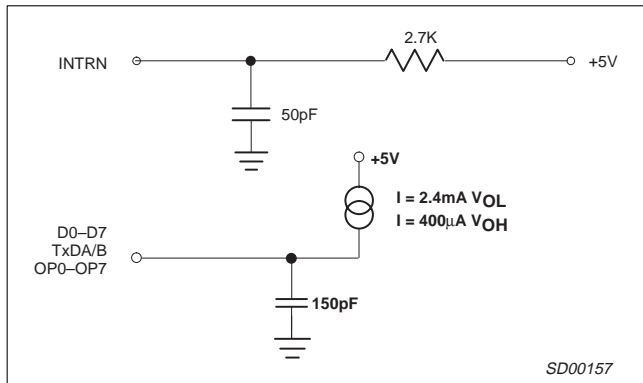


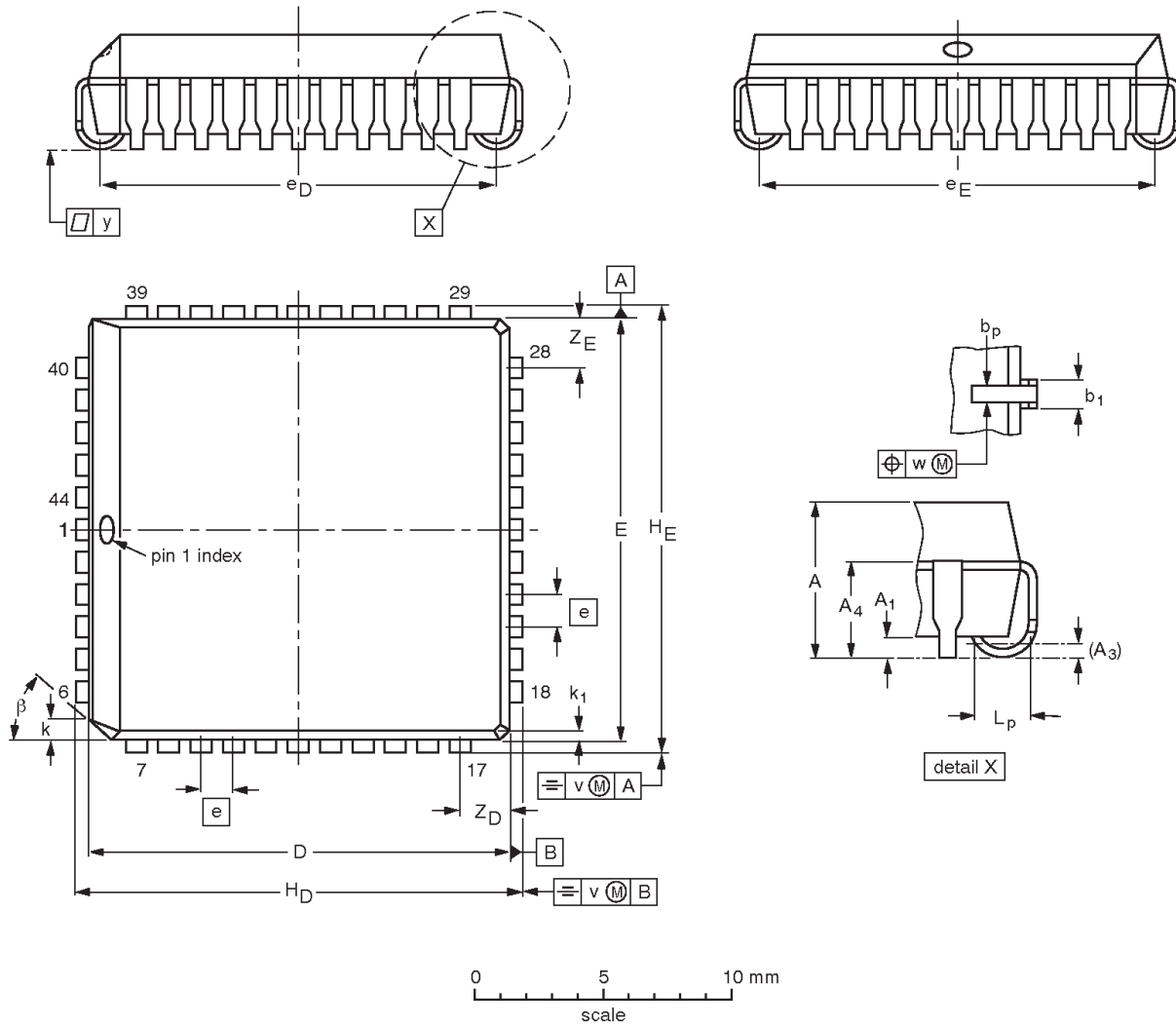
Figure 16. Test Conditions on Outputs

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

UNIT	A	A <sub>1</sub> min.	A <sub>3</sub>	A <sub>4</sub> max.	b <sub>p</sub>	b <sub>1</sub>	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>D</sub>	e <sub>E</sub>	H <sub>D</sub>	H <sub>E</sub>	k	k <sub>1</sub> max.	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup> max.	Z <sub>E</sub> <sup>(1)</sup> max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				95-02-25 97-12-16

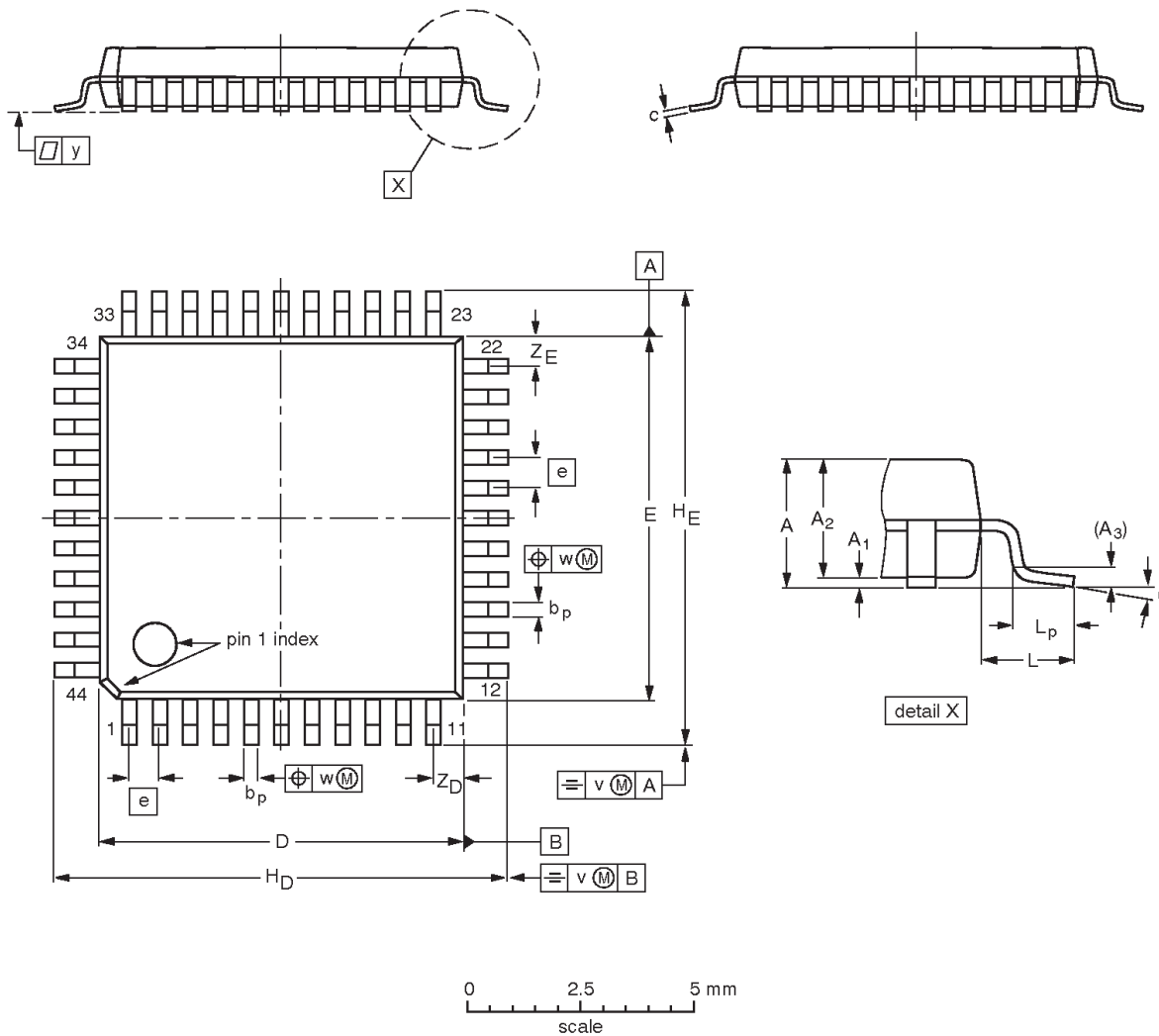


# Dual Universal Asynchronous Receiver/Transmitter (DUART)

## SC28L92

**QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm**

**SOT307-2**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						95-02-04 97-08-01

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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Date of release: 10-98

Document order number:

9397 750 04465

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# DATA SHEET

## **SC28L92**

Dual Universal Asynchronous  
Receiver/Transmitter (DUART)

Preliminary specification

1998 Oct 05

IC19 Data Handbook

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

## SC28L92

### DESCRIPTION

The SC28L92 is a pin and function replacement for the SCC2692 and SC26C92 operating at 3.3 or 5 volts supply with added features and deeper FIFOs. Its configuration on power up is that of the 2692. Its differences from the 2692 are: 16 character receiver, 16 character transmit FIFOs, watch dog timer for each receiver, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (Neither the SC26C92 nor The SCC2692 is being discontinued.)

Pin programming will allow the device to operate with either the Motorola or Intel bus interface The bit 3 of the MR0a register allows the device to operate in an 8 byte FIFO mode if strict compliance with the SC26C92 FIFO structure is required

The Philips Semiconductors SC28L92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates; a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by 8 or 16 character FIFOs to minimize the potential of receiver overrun, transmitter underpin and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC28L92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC28L92 is available in two package versions: a 44-pin PLCC and 44-pin plastic quad flat pack (PQFP).

### FEATURES

- 3.3 or 5.0 volt operation
- Dual full-duplex independent asynchronous receiver/transmitters
- 16 character FIFOs for each receiver and transmitter
- Pin programming for 68K or 80xxx bus interface
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
- 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 23 fixed rates: 50 to 230.4k baud
  - Other baud rates to MHz at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loop back
  - Remote loop back
  - Multi-drop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate interrupt outputs that may be wire ORed.
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates:
  - 1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multi-drop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver time-out mode
- Single +3.3V or +5V power supply
- Powers up to emulate SCC2692 and S26C92

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**Dual Universal Asynchronous  
Receiver/Transmitter (DUART)**

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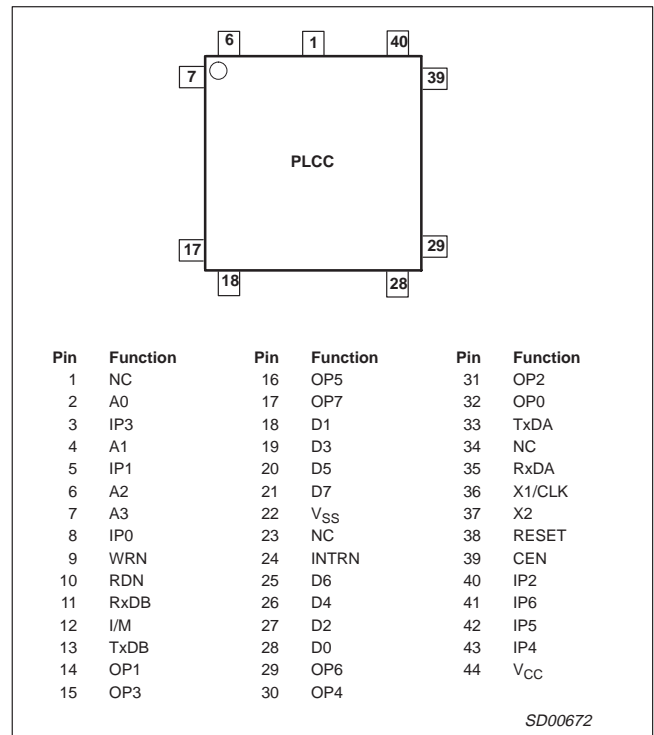
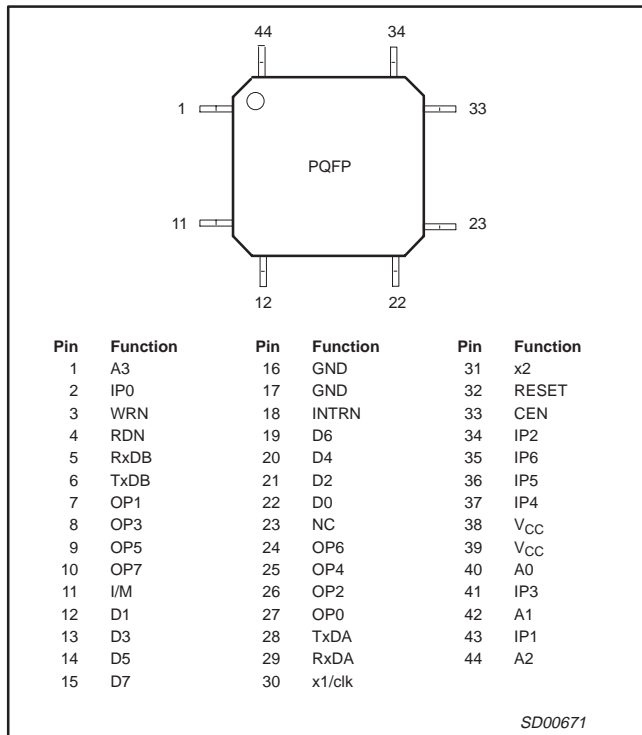
**SC28L92****ORDERING INFORMATION**

DESCRIPTION	INDUSTRIAL	DRAWING NUMBER
	$V_{CC} = +3.3 +5V \pm 10\%$ ,	
	$T_A = -40 \text{ to } +85^\circ\text{C}$	
44-Pin Plastic Leaded Chip Carrier (PLCC)	SC28L92A1A	SOT187-2
44-Pin Plastic Quad Flat Pack (PQFP)	SC28L92A1B	SOT307-2

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

## SC28L92

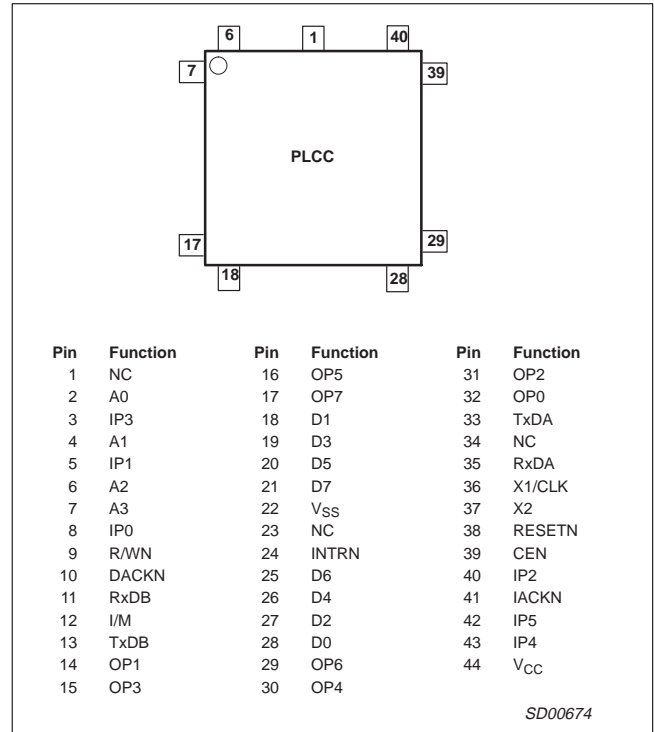
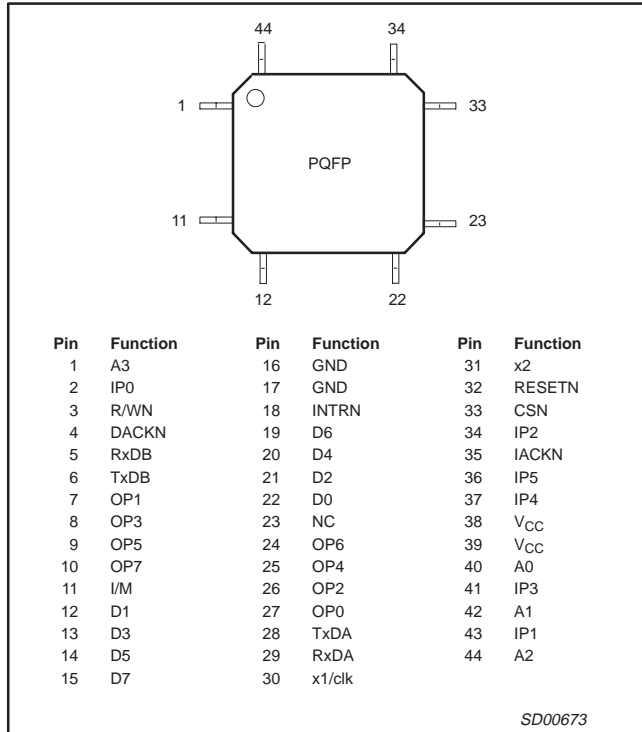
### PIN CONFIGURATION DIAGRAM 80XXX PIN CONFIGURATION



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

## SC28L92

### PIN CONFIGURATION DIAGRAM 68XXX PIN CONFIGURATION



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

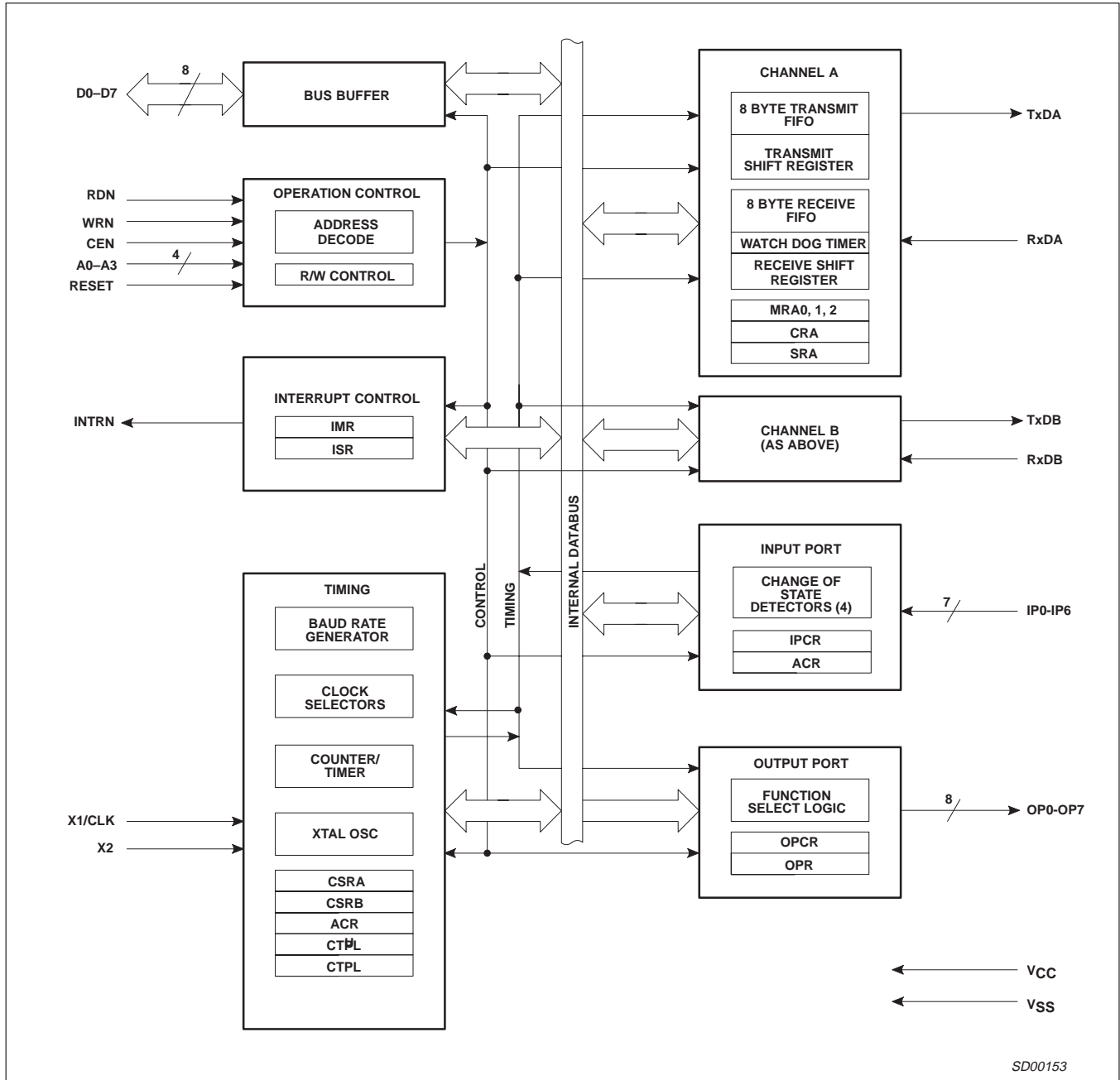


Figure 1. Block Diagram



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

## PIN CONFIGURATION FOR 80XXX BUS INTERFACE (INTEL®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	<b>Bus Configuration:</b> When high or not connected configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	<b>Data Bus:</b> Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	<b>Chip Enable:</b> Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
WRN	I	<b>Write Strobe:</b> When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	<b>Read Strobe:</b> When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	<b>Address Inputs:</b> Select the DUART internal registers and ports for read/write operations.
RESET	I	<b>Reset:</b> A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	<b>Interrupt Request:</b> Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	<b>Crystal 1:</b> Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	<b>Crystal 2:</b> Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	<b>Channel A Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High; "space" is Low.
RxDB	I	<b>Channel B Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High; "space" is Low.
TxDA	O	<b>Channel A Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	<b>Channel B Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
OP0	O	<b>Output 0:</b> General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	<b>Output 1:</b> General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	<b>Output 2:</b> General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	<b>Output 3:</b> General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	<b>Output 4:</b> General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR[1] output.
OP5	O	<b>Output 5:</b> General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	<b>Output 6:</b> General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	<b>Output 7:</b> General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	<b>Input 0:</b> General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	<b>Input 1:</b> General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	<b>Input 2:</b> General-purpose input or counter/timer external clock input.
IP3	I	<b>Input 3:</b> General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	<b>Input 4:</b> General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	<b>Input 5:</b> General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	I	<b>Input 6:</b> General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V <sub>CC</sub>	Pwr	<b>Power Supply:</b> +3.3 or +5V supply input ±10%
GND	Pwr	<b>Ground</b>

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## PIN CONFIGURATION FOR 68XXX BUS INTERFACE (MOTOROLA®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	<b>Bus Configuration:</b> When low configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	<b>Data Bus:</b> Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	<b>Chip Enable:</b> Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
R/WN	I	<b>Read/Write:</b> Input Signal. When CSN is low R/WN high input indicates a read cycle; when low indicates a write cycle.
IACKN	I	<b>Interrupt Acknowledge:</b> Active low input indicating an interrupt acknowledge cycle. Usually asserted by the CPU in response to an interrupt request. When asserted places the interrupt vector on the bus and asserts DACKN.
DACKN	O	<b>Data Transfer Acknowledge:</b> A3-State active -low output asserted in a write, read, or interrupt acknowledge cycle to indicate proper transfer of data between the CPU and the DUART.
A0–A3	I	<b>Address Inputs:</b> Select the DUART internal registers and ports for read/write operations.
RESETN	I	<b>Reset:</b> A low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	<b>Interrupt Request:</b> Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	<b>Crystal 1:</b> Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	<b>Crystal 2:</b> Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	<b>Channel A Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	I	<b>Channel B Receiver Serial Data Input:</b> The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	O	<b>Channel A Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	<b>Channel B Transmitter Serial Data Output:</b> The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
OP0	O	<b>Output 0:</b> General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	<b>Output 1:</b> General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	<b>Output 2:</b> General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	<b>Output 3:</b> General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	<b>Output 4:</b> General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR [1] output.
OP5	O	<b>Output 5:</b> General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	<b>Output 6:</b> General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	<b>Output 7:</b> General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	<b>Input 0:</b> General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	<b>Input 1:</b> General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	<b>Input 2:</b> General-purpose input or counter/timer external clock input.
IP3	I	<b>Input 3:</b> General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	<b>Input 4:</b> General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	<b>Input 5:</b> General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V <sub>CC</sub>	Pwr	<b>Power Supply:</b> +3.3 or +5V supply input ±10%
GND	Pwr	<b>Ground</b>

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	RATING	UNIT
$T_A$	Operating ambient temperature range <sup>2</sup>	Note 4	°C
$T_{STG}$	Storage temperature range	-65 to +150	°C
$V_{CC}$	Voltage from $V_{CC}$ to GND <sup>3</sup>	-0.5 to +7.0	V
$V_S$	Voltage from any pin to GND <sup>3</sup>	-0.5 to $V_{CC} + 0.5$	V
$P_D$	Package power dissipation (PLCC44)	2.4	W
$P_D$	Package power dissipation (PQFP44)	1.78	W
	Derating factor above 25°C (PLCC44)	19	mW/°C
	Derating factor above 25°C (PQFP44)	14	mW/°C

### NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
- For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
- This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameters are valid over specified temperature range.

## DC ELECTRICAL CHARACTERISTICS<sup>1, 2</sup>

$V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$V_{IL}$	Input low voltage				0.8	V
$V_{IH}$	Input high voltage (except X1/CLK)	0 to +70°C	2.4			
$V_{IH}$	Input high voltage (X1/CLK)	-40 to +85°C	2.5			V
$V_{IH}$	Input high voltage (X1/CLK)		$0.8 V_{CC}$			V
$V_{OL}$	Output low voltage	$I_{OL} = 2.4\text{mA}$			0.4	V
$V_{OH}$	Output high voltage (except OD outputs) <sup>3</sup>	$I_{OH} = -400\mu\text{A}$	$V_{CC} - 0.5$			V
$I_{IX1PD}$	X1/CLK input current - power down	$V_{IN} = 0$ to $V_{CC}$	-1		+1	$\mu\text{A}$
$I_{ILX1}$	X1/CLK input low current - operating	$V_{IN} = 0$	-100		0	$\mu\text{A}$
$I_{IHX1}$	X1/CLK input high current - operating	$V_{IN} = V_{CC}$	0		100	$\mu\text{A}$
$I_I$	Input leakage current: All except input port pins Input port pins	$V_{IN} = 0$ to $V_{CC}$ $V_{IN} = 0$ to $V_{CC}$	-1 -10		+1 +10	$\mu\text{A}$ $\mu\text{A}$
$I_{OZH}$	Output off current high, 3-State data bus	$V_{IN} = V_{CC}$			1	$\mu\text{A}$
$I_{OZL}$	Output off current low, 3-State data bus	$V_{IN} = 0\text{V}$	-1			$\mu\text{A}$
$I_{ODL}$	Open-drain output low current in off-state	$V_{IN} = 0$	-1			$\mu\text{A}$
$I_{ODH}$	Open-drain output high current in off-state	$V_{IN} = V_{CC}$			1	$\mu\text{A}$
$I_{CC}$	Power supply current <sup>4</sup> Operating mode Power down mode <sup>5</sup>	CMOS input levels CMOS input levels		2	25 10.0	mA $\mu\text{A}$

### NOTES:

- Parameters are valid over specified temperature range.
- Typical values are at +25°C, typical supply voltages, and typical processing parameters.
- Test conditions for outputs:  $C_L = 150\text{pF}$ , except interrupt outputs. Test conditions for interrupt outputs:  $C_L = 50\text{pF}$ ,  $R_L = 2.7\text{k}\Omega$  to  $V_{CC}$ .
- All outputs are disconnected. Inputs are switching between CMOS levels of  $V_{CC} - 0.2\text{V}$  and  $V_{SS} + 0.2\text{V}$ .
- See UART application note for power down currents of  $5\mu\text{A}$  or less.

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

## AC CHARACTERISTICS (80XXX MODE)<sup>1, 2, 3</sup>

$V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
<b>Reset Timing (See Figure 2)</b>					
$t_{RES}$	Reset pulse width	200			ns
<b>Bus Timing<sup>5</sup> (See Figure 3)</b>					
$t_{AS}$	A0–A3 setup time to RDN, WRN Low	10			ns
$t_{AH}$	A0–A3 hold time from RDN, WRN low	45			ns
$t_{CS}$	CEN setup time to RDN, WRN low	0			ns
$t_{CH}$	CEN Hold time from RDN. WRN low	0			ns
$t_{RW}$	WRN, RDN pulse width (Low time)	110			ns
$t_{DD}$	Data valid after RDN low			90	ns
$t_{DA}$	RDN low to data bus active <sup>6</sup>	0			ns
$t_{DF}$	Data bus floating after RDN or CEN high			30	ns
$t_{DI}$	RDN or CEN high to data bus invalid <sup>7</sup>	0			ns
$t_{DS}$	Data bus setup time before WRN or CEN high (write cycle)	75			ns
$t_{DH}$	Data hold time after WRN high	8			ns
$t_{RWD}$	High time between read and/or write cycles <sup>5, 7</sup>	55			ns
<b>Port Timing<sup>5</sup> (See Figure 8)</b>					
$t_{PS}$	Port in setup time before RDN low (Read IP ports cycle)	0			ns
$t_{PH}$	Port in hold time after RDN high	0			ns
$t_{PD}$	OP port valid after WRN or CEN high (OPR write cycle)			110	ns
<b>Interrupt Timing (See Figure 10)</b>					
	INTRN (or OP3–OP7 when used as interrupts) negated from:				
	Read RxFIFO (RxRDY/FFULL interrupt)			100	ns
	Write TxFIFO (TxRDY interrupt)			100	ns
$t_{IR}$	Reset Command (delta break change interrupt)			100	ns
	Stop C/T command (Counter/timer interrupt)			100	ns
	Read IPCR (delta input port change interrupt)			100	ns
	Write IMR (Clear of change interrupt mask bit(s))			100	ns
<b>Clock Timing (See Figure 7)</b>					
$t_{CLK}$	X1/CLK high or low time	80			ns
$f_{CLK}$	X1/CLK frequency <sup>8</sup>	0.1	3.686	4	MHz
$f_{CTC}$	C/T Clk (IP2) high or low time (C/T external clock input)	55			ns
$f_{CTC}$	C/T Clk (IP2) frequency <sup>8</sup>	0		8	MHz
$t_{RX}$	RxC high or low time (16X)	30			ns
$f_{RX}$	RxC Frequency (16X)	0		16	MHz
	RxC Frequency (1x) <sup>8, 9</sup>	0		1	MHz
$t_{TX}$	TxC High or low time (16X)	30			ns
$f_{TX}$	TxC frequency (16X)			16	MHz
	TxC frequency (1X) <sup>8, 9</sup>	0		1	MHz

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SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
<b>Transmitter Timing, external clock (See Figure 11)</b>					
$t_{TXD}$	TxD output delay from TxC low (TxC input pin)			120	ns
$t_{TCS}$	Output delay from TxC output pin low to TxD data output	-30		30	ns
<b>Receiver Timing, external clock (See Figure 12)</b>					
$t_{RXS}$	RxD data setup time to RxC high	100			ns
$t_{RXH}$	RxD data hold time from RxC high	100			ns

**NOTES:**

- Parameters are valid over specified temperature range.
- All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4 V and 3.0 V with a transition time of 5 ns maximum. For X1/CLK this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input voltages of 0.8 V and 2.0 V and output voltages of 0.8 V and 2.0 V, as appropriate.
- Test conditions for outputs: CL = 150 pF, except interrupt outputs. Test conditions for interrupt outputs: CL = 50 pF, RL = 2.7 Kohm to V<sub>CC</sub>. Number 3 use 4.
- Typical values are at +25°C, typical supply voltages, and typical processing parameters.
- Timing is illustrated and referenced to the WRN and RDN Inputs. Also, CEN may be the "strobing" input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
- Guaranteed by characterization of sample units.
- If CEN is used as the "strobing" input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for tRWD to guarantee that any status register changes are valid.
- Minimum frequencies are not tested but are guaranteed by design.
- Clocks for 1X mode should be symmetrical.

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## AC CHARACTERISTICS (68XXX MODE)<sup>1, 2, 3</sup>

$V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise specified.

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ <sup>3</sup>	Max	
<b>Reset Timing</b>						
$t_{RES}$	4	RESET pulse width	200			ns
<b>Bus Timing<sup>5</sup></b>						
$t_{AS}$	5,6,7	A1–A4 setup time to CSN Low	10			ns
$t_{AH}$	5,6,7	A1–A4 hold time from CSN Low	45			ns
$t_{RWS}$	5,6,7	RWN setup time to CSN High	0			ns
$t_{RWH}$	5,6,7	RWN holdup time to CSN High	0			ns
$t_{CSW}^8$	5,6,7	CSN High pulse width	110			ns
$t_{CSD}^9$	5,6,7	CSN or IACKN High from DTACKN Low	20			ns
$t_{DD}$	5,6,7	Data valid from CSN or IACKN Low			175	ns
$t_{DA}^8$	5	RDN Low to data bus active	15			ns
$t_{DF}^8$	5,6,7	Data bus floating from CSN or IACKN High			125	ns
$t_{DI}^8$	5	RDN High to data bus invalid	20			ns
$t_{DS}$	5,6,7	Data setup time to CLK High	100			ns
$t_{DH}$	5,6,7	Data hold time from CSN High	0			ns
$t_{DAL}$	5,6,7	DTACKN Low from read data valid	0			ns
$t_{DCR}$	5,6,7	DTACKN Low (read cycle) from CLK High			125	ns
$t_{DCW}$	5,6,7	DTACKN Low (write cycle) form CLK High			125	ns
$t_{DAH}$	5,6,7	DTACKN High from CSN or IACKN High			100	ns
$t_{DAT}$	5,6,7	DTACKN High impedance from CSN or IACKN High			125	ns
$t_{CSC}^7$	5,6,7	CSN or IACKN setup time to clock High	90			ns
<b>Port Timing<sup>5</sup></b>						
$t_{PS}$	8	Port input setup time to CSN Low	0			ns
$t_{PH}$	8	Port input hold time from CSN High	0			ns
$t_{PD}$	8	Port output valid from CSN High			400	ns
<b>Interrupt Timing</b>						
$t_{IR}^{10}$	7	INTRN (or OP3–OP7 when used as interrupts) negated from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break interrupt) Stop C/T command (counter interrupt) Read IPCR (input port change interrupt) Write IMR (clear of interrupt mask bit)			100 100 100 100 100 100	ns ns ns ns ns ns
<b>Clock Timing</b>						
$t_{CLK}$	10	X1/CLK High or Low time	80			ns
$f_{CLK}^{11}$	10	X1/CLK frequency	0	3.6864	4	MHz
$t_{CTC}$	10	CTCLK (IP2) High or Low time	55			ns
$f_{CTC}^9$	10	CTCLK (IP2) frequency	100		4	MHz
$t_{RX}$	10	RxC High or Low time	50			ns
$f_{RX}^9$	10	RxC frequency (16X) (1X)	0.1 100		16 1	MHz MHz
$t_{TX}$	10	TxC High or Low time	50			ns
$f_{TX}^9$	10	TxC frequency (16X) (1X)	0 0		16 1	MHz MHz
<b>Transmitter Timing</b>						
$t_{TXD}$	11	TxD output delay from TxC external clock input on IP pin			350	ns
$t_{TCS}$	11	Output delay from TxC low at OP pin to TxD data output			150	ns
<b>Receiver Timing</b>						
$t_{RXS}$	12	RxD data setup time before RxC high at external clock input on IP pin	240			ns
$t_{RXH}$	12	RxD data hold time after RxC high at external clock input on IP pin	200			ns

### NOTES:

- Parameters are valid over specified temperature range.
- All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.

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3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs:  $C_L = 150\text{pF}$ , except interrupt outputs. Test condition for interrupt outputs:  $C_L = 50\text{pF}$ ,  $R_L = 2.7\text{k}\Omega$  to  $V_{CC}$ .
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
8. Guaranteed by characterization of sample units.
9. Minimum frequencies are not tested but are guaranteed by design.
10. 325ns maximum for  $T_A > 70^\circ\text{C}$ .
11. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.
12. See UART application note for power down currents less than 5 $\mu\text{A}$ .



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## Block Diagram

The SC28L92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

## Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

## Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

## Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer. When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration.

## FIFO Configuration

Each receiver and transmitter has a 16 byte FIFO. These FIFOs may be configured to operate at a fill capacity of either 8 or 16 bytes. This feature may be used if it is desired to operate the 28L92 in strict compliance with the 26C92. The 8 byte/16 byte mode is controlled by the MR0[3] bit. A 0 value for this bit sets the 8 bit mode (the default); a 1 sets the 16 byte mode.

The FIFO fill interrupt level automatically follow the programming of the MR0[3] bit. See tables 3 and 4.

## TIMING CIRCUITS

### Crystal Clock

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

### BRG

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud.

Programming bit 0 of MR0 to a "1" gives additional baud rates of 57.6kB, 115.2kB and 230.4kB. These will be in the 16X mode. A 3.6864 MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

## Counter/Timer (C/T)

The counter timer is a 16-bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor. The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR/CTUR Register descriptions.

## Communications Channels A and B

Each communications channel of the SC28L92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (Break, Framing and Parity Errors) are also FIFOed with each data character.

## Input Port

The inputs to this unlatched 7-bit (6-bit for 68xxx mode) port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25–50 ms, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4 KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25 ms (this assumes that the clock input is 3.6864 MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25 ms if the transition occurs "coincident with the first sample pulse". The 50  $\mu$ s time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25 ms later.



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## Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins drive a state which is the (pg. 9 start) complement of the Output Port Register (OPR). The OPR register is set and reset by writing to the SOPR and ROPR addresses. (See the description of the SOPR and ROPR registers). The output pins will drive the inverse data polarity of the OPR registers. The OPCR register conditions these output pins to be controlled by the OPR or by other signals in the chip. Output ports are driven high on hardware reset.

## OPERATION

### Transmitter

The SC28L92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC28L92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPT bits will be set in the status register. When a character is loaded to the transmit FIFO the TxEMPT bit will be reset. The TxEMPT will not set until: 1) the transmit FIFO is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit FIFO, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the TxFIFO while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the TxFIFO.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command. The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS option is enabled (MR2[4] = 1), the CTS input at IP0 or IP1 must be Low in order for the character to be transmitted. The transmitter will check the state of the CTS input at the beginning of each character transmitted. If it is found to be High, the transmitter will delay the transmission of any following characters until the CTS has returned to the low state. CTS going high during the serialization of a character will not affect that character.

The transmitter can also control the RTSN outputs, OP0 or OP1 via MR2[5]. When this mode of operation is set, the meaning of the OP0 or OP1 signals will usually be 'end of message'. See description of the MR2[5] bit for more detail.

### Receiver

The SC28L92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive FIFO and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the Rx FIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the Rx FIFO and the received break bit in the SR is set to 1. The RxD input must return to high for two (2) clock edges of the X1 crystal clock for the receiver to recognize the end of the break condition and begin the search for a start bit.

**This will usually require a high time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock.**

### Receiver FIFO

The Rx FIFO consists of a First-In-First-Out (FIFO) stack with a capacity of 8 or 16 characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all 8 or 16 stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the Rx FIFO outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

### Receiver Status Bits

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the Rx FIFO is read. Therefore the status register should be read prior to reading the FIFO.

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If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

## Receiver Reset and Disable

Receiver disable stops the receiver immediately—data being assembled in the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers.

A 'watchdog timer' is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is to alert the control processor that characters are in the RxFIFO which have not been read and/or the data stream has stopped. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the receiver shift register to the RxFIFO or a read of the RxFIFO is executed.

## Receiver Time-out Mode

In addition to the watch dog timer described in the receiver section, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time out intervals.

The time-out mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the RxFIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data

during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

The time-out mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the time-out mode for that channel. Writing a 'Cx' to CRA or CRB will disable the time-out mode. The time-out mode should only be used by one channel at once, since it uses the C/T. If, however, the time-out mode is enabled from both receivers, the time-out will occur only when **both** receivers have stopped receiving data for the time-out period. CTU and CTL must be loaded with a value greater than the normal receive character period. The time-out mode disables the regular START/STOP Counter commands and puts the ca/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Time-out Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

## Time Out Mode Caution

When operating in the special time out mode, it is possible to generate what appears to be a "false interrupt", i.e., an interrupt without a cause. This may result when a time-out interrupt occurs and then, BEFORE the interrupt is serviced, another character is received, i.e., the data stream has started again. (The interrupt latency is longer than the pause in the data stream.) In this case, when a new character has been received, the counter/timer will be restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR will show the "Counter Ready" bit not set. If nothing else is interrupting, this read of the ISR will return a x'00 character.

## Multi-drop Mode (9-bit or Wake-Up)

The DUART is equipped with a wake up mode for multi-drop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while

MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the TxFIFO.

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In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RxFIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RxFIFO. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

### PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has 3 mode registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register "Miscellaneous Commands". Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Philips Semiconductors UART software.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

**Table 1. SC28L92 register addressing READ (RDN = 0), WRITE (WRN = 0)**

0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RxFIFOA)	Tx Holding Register A (TxFIFOA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Preset Register (CTPU)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Preset Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RxFIFOB)	Tx Holding Register B (TxFIFOB)
1	1	0	0	Interrupt vector (68K mode)	Interrupt vector (68K mode)
1	1	0	0	General purpose register (Intel mode)	General purpose register (Intel mode)
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command (SOPR)
1	1	1	1	Stop Counter Command	Reset output Port Bits Command (ROPR)

**NOTE:**

1. The three MR registers are accessed via the MR Pointer and Commands 0x1n and 0xBn (where n = represents receiver and transmitter enable bits)

The following named registers are the same for Channels A and B				
Mode	Register	MRnA	MRnB	R/W
Status	Register	SRA	SRB	R only
Clock	Select	CSRA	CSRB	W only
Command	Register	CRA	CRB	W only
Receiver	FIFO	RxFIFOA	RxFIFOB	R only
Transmitter	FIFO	TxFIFOA	TxFIFOB	W only

These are support functions for both Channels		
Register Name	Register	R/W
Input Port Change Register	IPCR	R
Auxiliary Control Register	ACR	W
Interrupt Status Register	ISR	R
Interrupt Mask Register	IMR	W
Counter Timer Upper Value	CTU	R
Counter Timer Lower Value	CTL	R
Counter Timer Preset Upper	CTPU	W
Counter Timer Preset Lower	CTPL	W
Input Port Register	IPR	R
Output Configuration Register	OPCR	W
Set Output Port	Bits	W
Reset Output Port	Bits	W

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**Table 2. Register bit formats**

**MR0 – MODE REGISTER 0**

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR0	WATCHDOG	RxINT BIT 2	TxINT (1:0)	FIFO SIZE	BAUD RATE EXTENDED II	TEST 2	BAUD RATE EXTENDED 1	

**MR1 – MODE REGISTER 1**

Bit 7	Bit 6	Bit 5	Bit 4:3	Bit 2	Bit 1:0
RxRTS Control	ISR Read Mode	Error Mode	Parity Mode	Parity Type	Bits per Character

**MR2 – MODE REGISTER 2**

Bits 7:6	Bit 5	Bit 4	Bit 3:2	Bit 1:0
Channel Mode	TxRTS Control	CTSN Enable Tx	RxINT	Stop Length

**CSR – CLOCK SELECT REGISTER**

Bits 7:4	Bits 43:0
Receiver Clock, Select Code	Transmitter Clock select code,

**CR –COMMAND REGISTER**

Bits 7:4	Bit 3	Bit 2	Bit 1	Bit 0
Channel Command codes	Disable Tx	Enable Tx	Enable Tx	Enable Rx

**SR – CHANNEL STATUS REGISTER**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Received Break	Framing Error	Parity Error	Overrun Error	TxE <sub>MT</sub>	TxRDY	RxFULL	RxRDY

**IMR – INTERRUPT MASK REGISTER (ENABLES INTERRUPTS)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change Input Port	Change Break B	RxRDY B	TxRDYB	Counter Ready	Change Break A	RxRDY A	TxRDY A

**ISR – INTERRUPT STATUS REGISTER**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change Input Port	Change Break B	RxRDY B	TxRDYB	Counter Ready	Change Break A	RxRDY A	TxRDY A

**CTPU – COUNTER TIMER PRESET REGISTERS, UPPER**

Bits 7:0
8 MSB of the BRG Timer divisor.

**CTPL – COUNTER TIMER PRESET REGISTER, LOWER**

Bits 7:0
8 LSB of the BRG Timer divisor.

**ACR – COUNTER TIMER PRESET REGISTER**

Bit 7	Bit 6:4	Bit 3	Bit 2	Bit 1	Bit 0
Baud Group	Counter Timer mode and clock select	Enable IP3	Enable IP2	Enable IP1	Enable IP0

**IPCR – INPUT PORT CHANGE REGISTER**

Bit 7	Bit 6:4	Bit 3	Bit 2	Bit 1	Bit 0
Baud Group	Counter Timer mode and clock select	Enable IP3	Enable IP2	Enable IP1	Enable IP0

**IPR – INPUT PORT REGISTER**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
State of IP	State of IP 6	State of IP 5	State of IP 4	State of IP 3	State of IP 2	State of IP 1	State of IP 0

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## REGISTER DESCRIPTIONS Mode Registers

### MR0a

MR0 Mode Register 0 MR0 is accessed by setting the MR pointer to 0 via the command register command B.

	Bit 7	BIT 6	BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>MR0A</b> <b>MR0B</b> MR0B[3:0] are reserved	<b>Rx WATCHDOG</b> 0 = Disable 1 = Enable	<b>RxINT BIT 2</b> See Tables in MR0 description	<b>TxINT (1:0)</b> See table #4	<b>FIFO SIZE</b> 0 = 8 byte FIFO 1 = 16 byte FIFO	<b>BAUD RATE EXTENDED II</b> 0 = Normal 1 = Extend II	<b>TEST 2</b> Set to 0	<b>BAUD RATE EXTENDED I</b> 0 = Normal 1 = Extend

**MR0[7]**—This bit controls the receiver watch dog timer. 0 = disable, 1 = enable. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the Rx FIFO that has not been read. This situation may occur when the byte count of the last part of a message is not large enough to generate an interrupt.

**MR0[6]**—Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the FIFO that generates the receiver interrupt.

**MR0[6] MR1[6]** Note that this control is split between MR0 and MR1. This is for backward compatibility to the SC2692 and SCN2681.

**Table 3. Receiver FIFO interrupt fill level (MR0(3) = 0)**

MR0[6] MR1[6]	Interrupt Condition
00	1 or more bytes in FIFO (Rx RDY)
01	3 or more bytes in FIFO
10	6 or more bytes in FIFO
11	8 bytes in FIFO (Rx FULL)

**Table 3a. Receiver FIFO interrupt fill level(MR0(3)=1)**

MR0[6] MR1[6]	Interrupt Condition
00	1 or more bytes in FIFO (Rx RDY)
01	8 or more bytes in FIFO
10	12 or more bytes in FIFO
11	16 bytes in FIFO (Rx FULL)

For the receiver these bits control the number of FIFO positions filled when the receiver will attempt to interrupt. After the reset the receiver FIFO is empty. The default setting of these bits cause the receiver to attempt to interrupt when it has one or more bytes in it.

**MR0[5:4]**—Tx interrupt fill level.

**Table 4. Transmitter FIFO interrupt fill level MR0(3) = 0**

MR0[5:4]	Interrupt Condition
00	8 bytes empty (Tx EMPTY)
01	4 or more bytes empty
10	6 or more bytes empty
11	1 or more bytes empty (Tx RDY)

**Table 4a. Transmitter FIFO interrupt fill level MR0(3) = 1**

MR0[5:4]	Interrupt Condition
00	16 bytes empty (Tx EMPTY)
01	8 or more bytes empty
10	12 or more bytes empty
11	1 or more bytes empty (Tx RDY)

For the transmitter these bits control the number of FIFO positions empty when the transmitter will attempt to interrupt. After the reset the transmit FIFO has 8 bytes empty. It will then attempt to interrupt as soon as the transmitter is enabled. The default setting of the MR0 bits (5:4) condition the transmitter to attempt to interrupt only when it is completely empty. As soon as one byte is loaded, it is no longer empty and hence will withdraw its interrupt request.

**MR0[3]**—Selects the FIFO depth at 8 or 16 bytes. See Tables 3 and 4

**MR0[2:0]**—These bits are used to select one of the six baud rate groups.

See Table 5 for the group organization.

- 000 Normal mode
- 001 Extended mode I
- 100 Extended mode II

Other combinations of MR2[2:0] should not be used

**Note:** MR0[3:0] are not used in channel B and should be set to 0.



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## MR1A

MR1 Mode Register 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Rx CONTROLS RTS	RxINT BIT 1	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHARACTER	
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multi-drop Mode		0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8	

**NOTE:**

In block error mode, block error conditions must be cleared by using the error reset command (command 4x) or a receiver reset.

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CR command 1. After reading or writing MR1A, the pointer will point to MR2A.

**MR1A[7]—Channel A Receiver Request-to-Send Control (Flow Control)**

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0].

MR1A[7] = 1 causes RTSAN to be negated (OP0 is driven to a '1' [V<sub>CC</sub>]) upon receipt of a valid start bit if the Channel A FIFO is full. This is the beginning of the reception of the ninth byte. If the FIFO is not read before the start of the tenth byte, an overrun condition will occur and the tenth byte will be lost. However, the bit in OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

**MR1[6]**—Bit 1 of the receiver interrupt control. See description under MR0[6].

**MR1A[5]—Channel A Error Mode Select**

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block'

mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

**MR1A[4:3]—Channel A Parity Mode Select**

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multi-drop mode described in the Operation section.

**MR1A[2]—Channel A Parity Type Select**

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multi-drop mode it selects the polarity of the A/D bit.

**MR1A[1:0]—Channel A Bits Per Character Select**

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

**MR2A—Channel A Mode Register 2**

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

## MR2 MODE REGISTER 2

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE		Tx CONTROLS RTS	CTS ENABLE Tx	STOP BIT LENGTH NOTE: Add 0.5 to binary codes 0–7 for 5 bit character lengths.			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop		0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

**NOTE:**

Add 0.5 to values shown for 0–7 if channel is programmed for 5 bits/char.

**MR2A[7:6]—Channel A Mode Select**

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently.

MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is relocked and retransmitted on the TxDA output.

2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.

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6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loop back mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loop back mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA out-put.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of auto echo or remote loop back modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in auto echo by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in auto echo mode until the entire stop has been re-transmitted.

**MR2A[5]—Channel A Transmitter Request-to-Send Control** This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the Tx FIFO, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled.

This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A Tx FIFO.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

**MR2A[4]—Channel A Clear-to-Send Control** If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

**MR2A[3:0]—Channel A Stop Bit Length Select** This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the stop bit position (one bit time after the last data bit, or after the parity bit if enabled is sampled).

If an external 1X clock is used for the transmitter,

MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

## MR0B—Channel B Mode Register 0

MR0B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR0 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR0B, the pointer will point to MR1B.

The bit definitions for this register are identical to MR0A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs. MR0B[3:0] are reserved.

## MR1B—Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## MR2B—Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

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## CSRA—Channel A Clock Select Register

### CSRA[7:4]—Channel A Receiver Clock Select

This field selects the baud rate clock for the Channel A receiver. The field definition is shown in Table 5.

### CSR CLOCK SELECT REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSRA	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
CSRB	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	See Text and table 5				See Text and table 5			

**Table 5. Baud rate (base on a 3.6864MHz crystal clock)**

CSRA[7:4]	MR0[0] = 0 (Normal Mode)		MR0[0] = 1 (Extended Mode I)		MR0[2] = 1 (Extended Mode II)	
	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	300	450	4,800	7,200
0001	110	110	110	110	880	880
0010	134.5	134.5	134.5	134.5	1,076	1,076
0011	200	150	1200	900	19.2K	14.4K
0100	300	300	1800	1800	28.8K	28.8K
0101	600	600	3600	3600	57.6K	57.6K
0110	1,200	1,200	7200	7,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1001	4,800	4,800	28.8K	28.8K	4,800	4,800
1010	7,200	1,800	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	57.6K	57.6K	9,600	9,600
1100	38.4K	19.2K	230.4K	115.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer	Timer	Timer
1110	IP4–16X	IP4–16X	IP4–16X	IP4–16X	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X	IP4–1X	IP4–1X	IP4–1X	IP4–1X

**NOTE:**

The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.



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**Table 6. Bit rate generator characteristics**

Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (KHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

**NOTE:**

Duty cycle of 16X clock is 50% ± 1%

**CSRA[3:0]—Channel A Transmitter Clock Select**

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 5, except as follows:

CSRA[3:0]	
1110	1111
IP3–16X	IP3–1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

**CSRB—Channel B Clock Select Register**

**CSRB[7:4]—Channel B Receiver Clock Select**

This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 5, except as follows:

CSRB[7:4]	
1110	1111
IP6–1X	IP6–16X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

**CSRB[3:0]—Channel B Transmitter Clock Select**

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 5, except as follows:

CSRB[3:0]	
1110	1111
IP5–1X	IP5–16X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

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## CRA—Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

### CR COMMAND REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB	MISCELLANEOUS COMMANDS				Disable Tx	Enable Tx	Disable Rx	Enable Rx
	See Text of Channel Command Register				1 = Yes 0 = No	1 = Yes 0 = No	1 = Yes 0 = No	1 = Yes 0 = No

#### NOTES:

Access to the miscellaneous commands should be separated by 3 X1 clock edges. A disabled transmitter cannot be loaded.

#### CRA[7:4]—Miscellaneous Commands

Execution of the commands in the upper four bits of this register must be separated by 3 X1 clock edges. Other reads or writes (including writes to the lower four bits) may be inserted to achieve this separation.

#### CRA[7:4]—Commands

0000	No command.	1010	Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset. (See also Watchdog timer description in the receiver section.)
0001	Reset MR pointer. Causes the Channel A MR pointer to point to MR1.	1011	Set MR pointer to '0'
0010	Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.	1100	Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued to force a reset of the ISR(3) bit
0011	Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.	1101	Not used.
0100	Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.	1110	Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.
0101	Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero	1111	Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only. For maximum power reduction input pins should be at V <sub>SS</sub> or V <sub>DD</sub> .
0110	Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the Tx FIFO, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.		
0111	Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.		
1000	Assert RTSN. Causes the RTSN output to be asserted (Low).		
1001	Negate RTSN. Causes the RTSN output to be negated (High)		

#### CRA[3]—Disable Channel A Transmitter

This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the Tx FIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

#### CRA[2]—Enable Channel A Transmitter

Enables operation of the Channel A transmitter. The TxRDY and TxEMT status bits will be asserted if the transmitter is idle.

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**CRA[1]—Disable Channel A Receiver**

This command terminates operation of the receiver immediately—a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multi-drop mode is programmed, the receiver operates even if it is disabled. See Operation section.

**CRA[0]—Enable Channel A Receiver**

Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

**CRB—Channel B Command Register**

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of commands "Ex" and "Fx" which are used for power down mode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

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## SRA—Channel A Status Register SR STATUS REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>SRA SRB</b>	<b>RECEIVED BREAK*</b>	<b>FRAMING ERROR*</b>	<b>PARITY ERROR*</b>	<b>OVERRUN ERROR</b>	<b>TxE<sub>MT</sub></b>	<b>TxRDY</b>	<b>FFULL</b>	<b>RxRDY</b>
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

\*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a “reset error status” command. In character mode they are discarded when the corresponding data character is read from the FIFO. In block error mode, the error-reset command (command 4x or receiver reset) must be used to clear block error conditions

**SRA[7]—Channel A Received Break** This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time two successive edges of the internal or external 1X clock. **This will usually require a high time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock.**

When this bit is set, the Channel A ‘change in break’ bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

This bit is reset by command 4 (0100) written to the command register or by receiver reset.

### SRA[6]—Channel A Framing Error

This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

### SRA[5]—Channel A Parity Error

This bit is set when the ‘with parity’ or ‘force parity’ mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multi-drop mode the parity error bit stores the receive A/D (Address/Data) bit.

### SRA[4]—Channel A Overrun Error

This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a ‘reset error status’ command.

### SRA[3]—Channel A Transmitter Empty (TxEMTA)

This bit will be set when the transmitter under runs, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the under run condition.

### SRA[2]—Channel A Transmitter Ready (TxRDYA)

This bit, when set, indicates that the transmit FIFO is not full and ready to be loaded with another character. This bit is cleared when the transmit FIFO is loaded by the CPU and there are (after this load) no more empty locations in the FIFO. It is set when a character is transferred to the transmit shift register. TxRDYA is reset when the transmitter is disabled and is set when the

transmitter is first enabled. Characters loaded to the Tx FIFO while this bit is 0 will be lost. This bit has different meaning from ISR[0].

### SRA[1]—Channel A FIFO Full (FFULLA)

This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the receive FIFO. If a character is waiting in the receive shift register because the FIFO is full, FFULLA will not be reset when the CPU reads the receive FIFO. This bit has different meaning from ISR1 when MR1 6 is programmed to a ‘1’.

### SRA[0]—Channel A Receiver Ready (RxRDYA)

This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receive FIFO, only if (after this read) there are no more characters in the FIFO.

## SRB—Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

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## OPCR—Output Port Configuration Register OPCR OUTPUT PORT CONFIGURATION REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0 = OPR[7] 1 = TxRDY B	0 = OPR[6] 1 = TxRDY A	0 = OPR[5] 1 = RxRDY/FFULL B	0 = OPR[4] 1 = RxRDY/FFULL A	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)		00 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)	

### OPCR[7]—OP7 Output Select

This bit programs the OP7 output to provide one of the following:

- 0 The complement of OPR[7].
- 1 The Channel B transmitter interrupt output which is the complement of ISR[4]. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[6]—OP6 Output Select

This bit programs the OP6 output to provide one of the following:

- 0 The complement of OPR[6].
- 1 The Channel A transmitter interrupt output which is the complement of ISR[0]. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[5]—OP5 Output Select

This bit programs the OP5 output to provide one of the following:

- 0 The complement of OPR[5].
- 1 The Channel B receiver interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[4]—OP4 Output Select

This field programs the OP4 output to provide one of the following:

- 0 The complement of OPR[4].
- 1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

### OPCR[3:2]—OP3 Output Select

This bit programs the OP3 output to provide one of the following:

- 00 The complement of OPR[3].
- 01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- 10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- 11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

### OPCR[1:0]—OP2 Output Select

This field programs the OP2 output to provide one of the following:

- 00 The complement of OPR[2].
- 01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- 10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- 11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

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## SOPR—Set the Output Port Bits (OPR)

SOPR[7:0]—Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect. This allows software to set individual bits with our keeping a copy of the OPR bit configuration.

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0
<b>Set OPR Bits</b>	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change	1=set bit 0 = no change

## ROPR—Reset Output Port Bits (OPR)

ROPR[7:0]—Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect. This allows software to reset individual bits with our keeping a copy of the OPR bit configuration.

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0
<b>Reset OPR Bits</b>	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change	1=reset bit 0 = no change

## OPR Output Port Register

The output pins (OP pins) drive the compliment of the data written to this register.

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0
<b>OPR</b>	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low

## ACR Auxiliary Control Register

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	<b>BRG SET Select</b>	<b>Counter Timer Mode Mode and clock sour select</b>			<b>Delta IP3 int enable</b>	<b>Delta IP3 int enable</b>	<b>Delta IP3 int enable</b>	<b>Delta IP3 int enable</b>
<b>ACR</b>	0 = set 1 1 = set 2	See table 7			0 = off 1 = enabled	0 = off 1 = enabled	0 = off 1 = enabled	0 = off 1 = enabled

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## ACR—Auxiliary Control Register

### ACR[7]—Baud Rate Generator Set Select

This bit selects one of two sets of baud rates to be generated by the BRG (see Table 5).

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB.

Baud rate generator characteristics are given in Table 6.

### ACR[6:4]—Counter/Timer Mode And Clock Source Select

This field selects the operating mode of the counter/timer and its clock source as shown in Table 7

### ACR [3:0]—IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable

This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR [7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR [7], which results in the generation of an interrupt output if IMR [7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR [7].

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**Table 7. ACR 6:4 field definition**

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA - 1X clock of Channel A transmitter
010	Counter	TxCB - 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

**NOTE:**

The timer mode generates a square wave

**IPCR INPUT PORT CONFIGURATION REGISTER**

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>IPCR</b>	<b>Delta IP3</b>	<b>Delta IP3</b>	<b>Delta IP3</b>	<b>Delta IP3</b>	<b>IP 3</b>	<b>IP 2</b>	<b>IP 1</b>	<b>IP 0</b>
	0 = no change 1 = change	0 = no change 1 = change	0 = no change 1 = change	0 = no change 1 = change	0 = low 1 = High	0 = low 1 = High	0 = low 1 = High	0 = low 1 = High

**IPCR [7:4]—IP3, IP2, IP1, IP0 Change-of-State**

These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR [7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

**IPCR [3:0]—IP3, IP2, IP1, IP0 Change-of-State**

These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.



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## ISR—Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR - the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to H'00' when the DUART is reset.

### ISR INTERRUPT STATUS REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR	INPPUT PORT CHANGE	DELTA Break B	RxRDY/ FFULL B	TxRDY B	Counter Ready	Delta Break A	RxRDY/ FFULL A	TxRDY A
	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled

#### ISR[7]—Input Port Change Status

This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

#### ISR[6]—Channel B Change In Break

This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

#### ISR[5]—RxB Interrupt

This bit indicates that the channel B receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

#### ISR[4]—TxB Interrupt

This bit indicates that the channel B transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

#### ISR[3]—Counter Ready.

In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

#### ISR[2]—Channel A Change in Break

This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

#### ISR[1]—RxA Interrupt

This bit indicates that the channel A receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

#### ISR[0]—TxA Interrupt

This bit indicates that the channel A transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

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## IMR—Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

### IMR INTERRUPT MASK REGISTER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR	INPPUT PORT CHANGE	Delta Break B	RxRDY/ FFULL B	TxRDY B	Counter Ready	Delta Break A	RxRDY/ FFULL A	TxRDY A
INTERRUPT	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled	0 = not enabled 1 = enabled

## CTPU and CTPL – Counter/Timer Registers

### CTPU COUNTER TIMER PRESET UPPER

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTPU	The lower eight (8) bits for the 16 bit counter timer preset register							

### CTPL COUNTER -TIMER PRESET LOW

	Bit 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTPL	The Upper eight (8) bits for the 16 bit counter timer preset register							

The CTPU and CTPL hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTPU/CTPL registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer mode, the C/T generates a square wave whose period is twice the value (in C/T clock periods) of the CTPU and CTPL. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTPU and CTPL for a particular 1X data clock is shown below.

$$n = (\text{C/T Clock Frequency}) \text{ divided by } (2 \times 16 \times \text{Baud rate desired})$$

$$n = (\text{C/T Clock Frequency}) / (2 \times 16 \times \text{Baud rate desired})$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

If the value in CTPU and CTPL is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTPU and CTPL.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output. In the counter mode, the value C/T loaded into CTPU and CTPL by the CPU is counted down to 0.. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set.

The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTPU and CTPL at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTPU and CTPL.

When the C/T clock divided by 16 is selected, the maximum divisor becomes 1,048,575.

## Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register (except the 2681 and 68681) The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V ss).

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Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one ( $V_{DD}$ ).

### The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB. RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the ninth character is sensed. Transmission then stops with nine valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter. MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be.

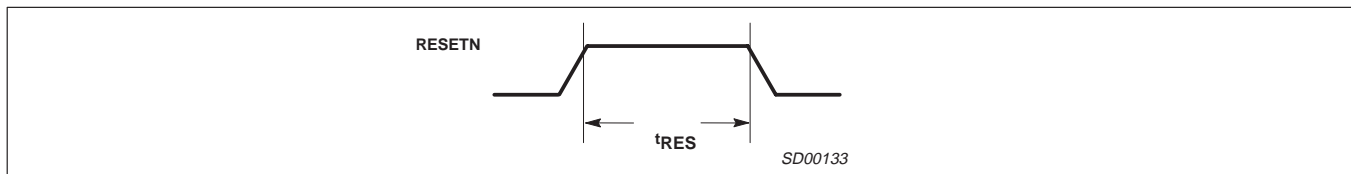


Figure 2. Reset Timing (80XXX mode)

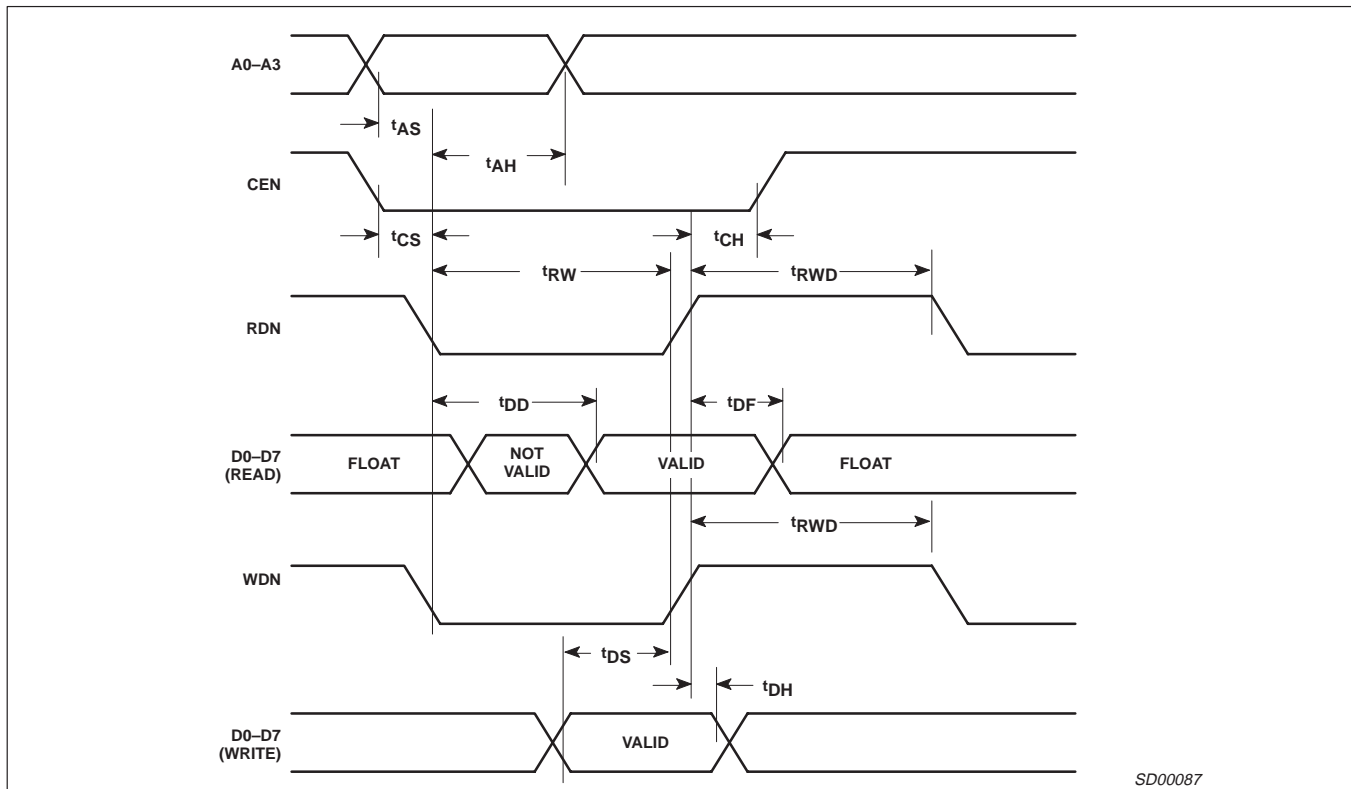


Figure 3. Bus Timing (80XXX mode)

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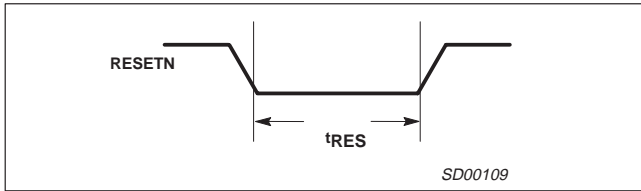
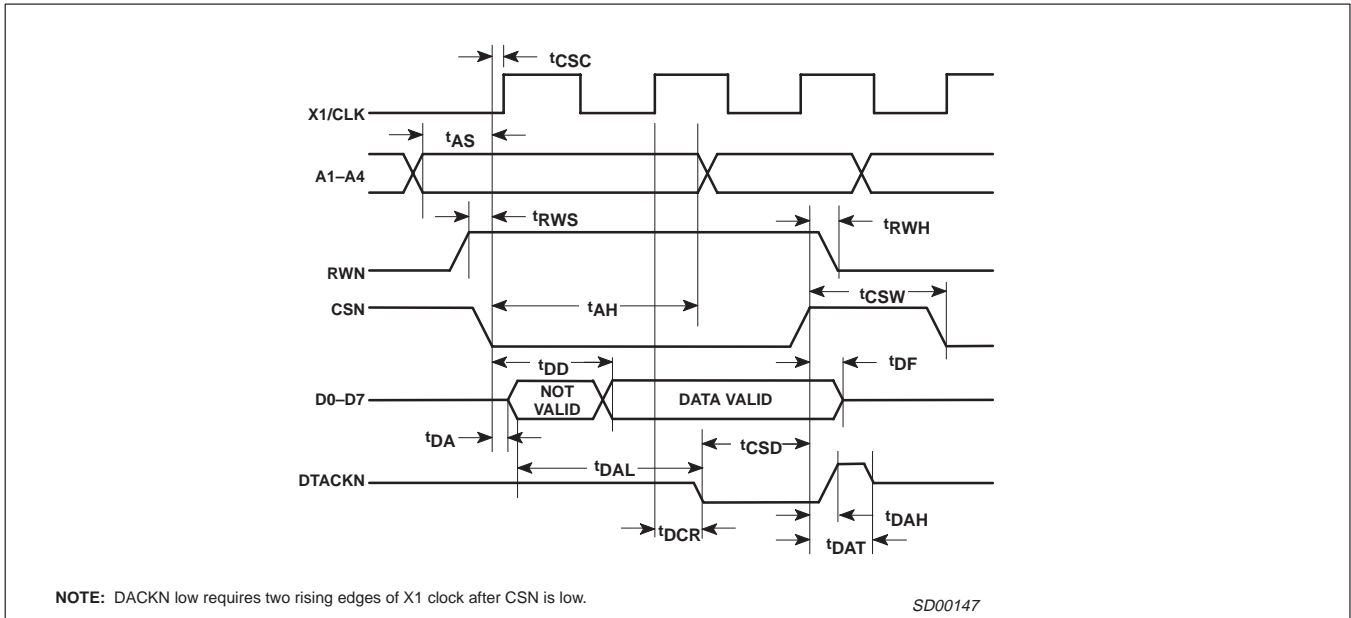


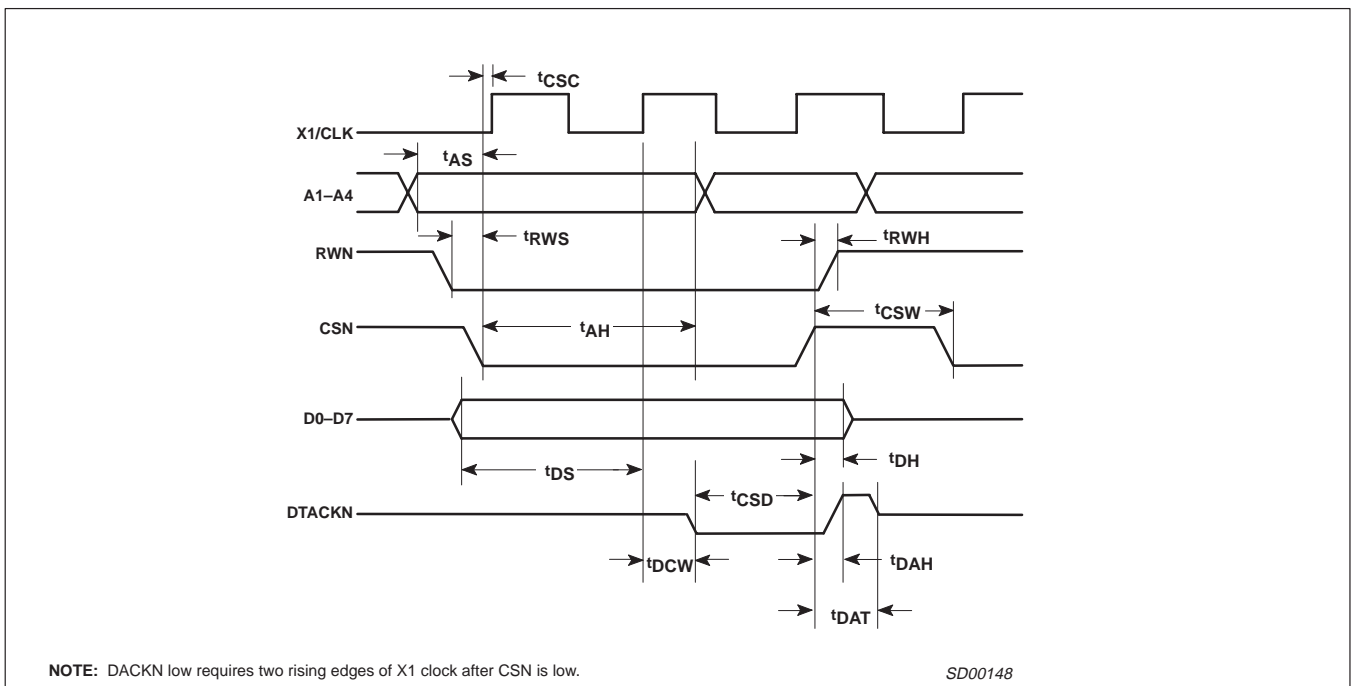
Figure 4. Reset Timing (68XXX mode)



NOTE: DACKN low requires two rising edges of X1 clock after CSN is low.

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Figure 5. Bus Timing (Read Cycle) (68XXX mode)



NOTE: DACKN low requires two rising edges of X1 clock after CSN is low.

SD00148

Figure 6. Bus Timing (Write Cycle) (68XXX mode)

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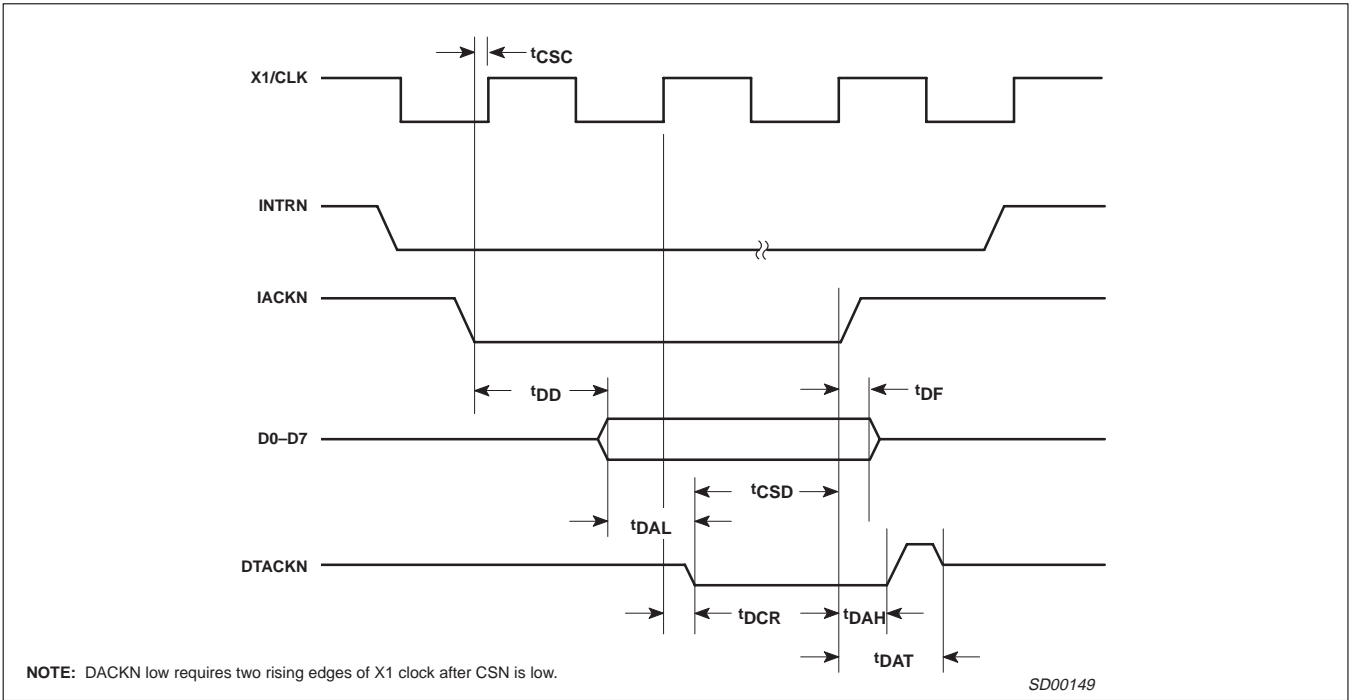


Figure 7. Interrupt Cycle Timing (68XXX mode)

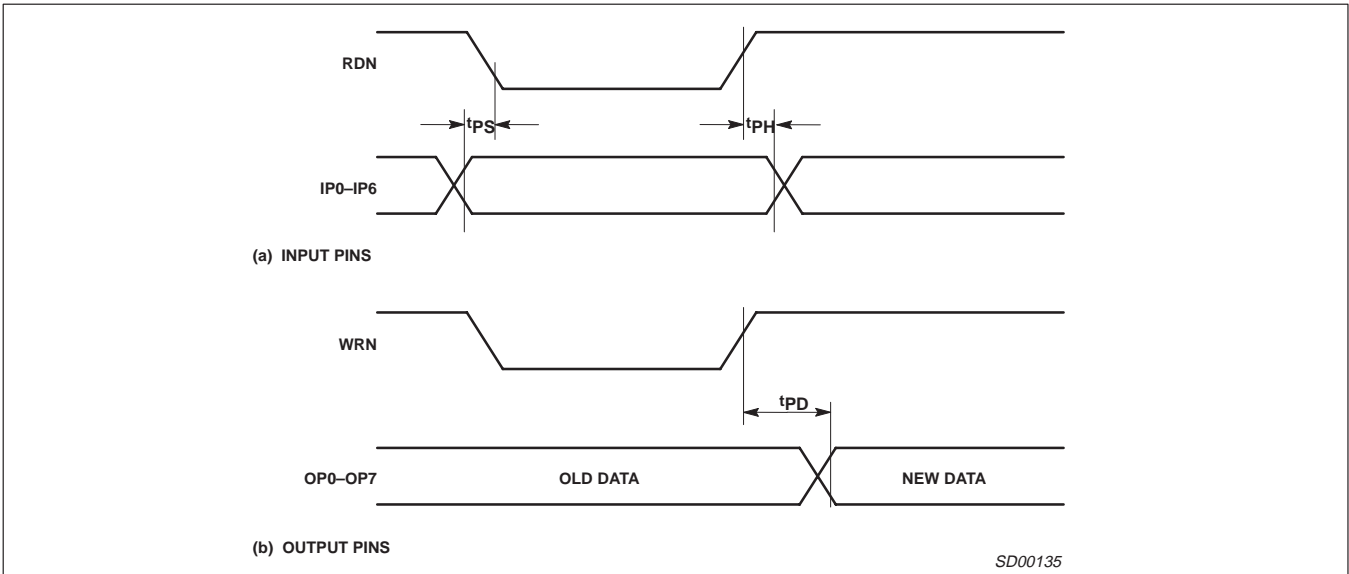


Figure 8. Port Timing

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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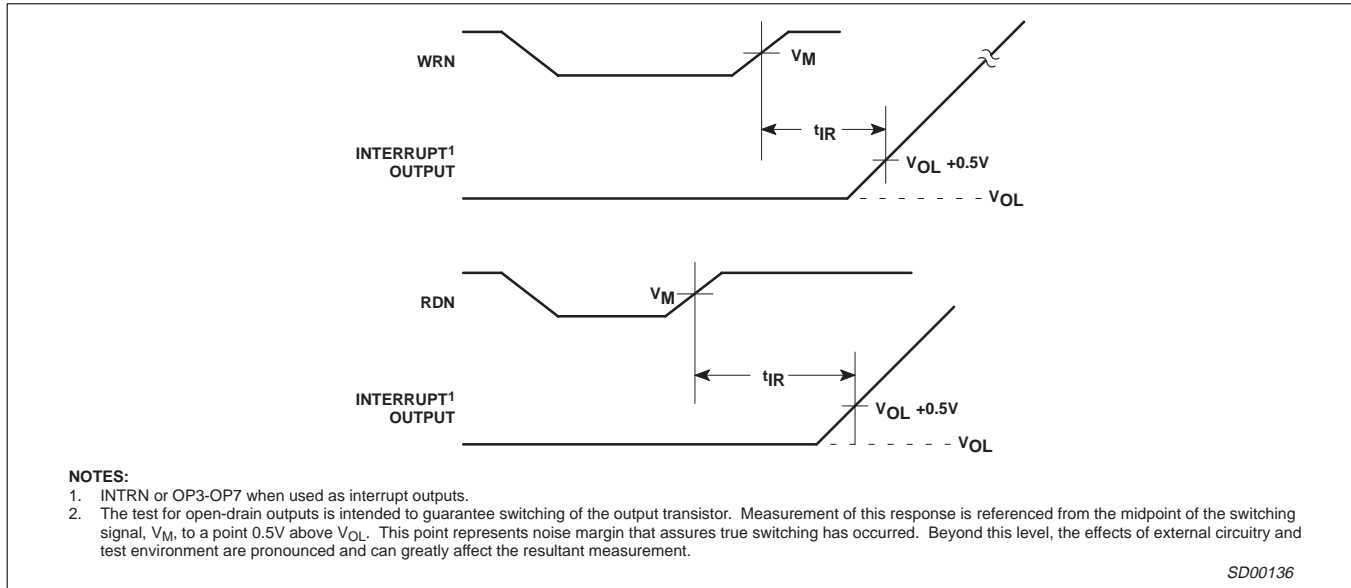


Figure 9. Interrupt Timing (80xxx mode)

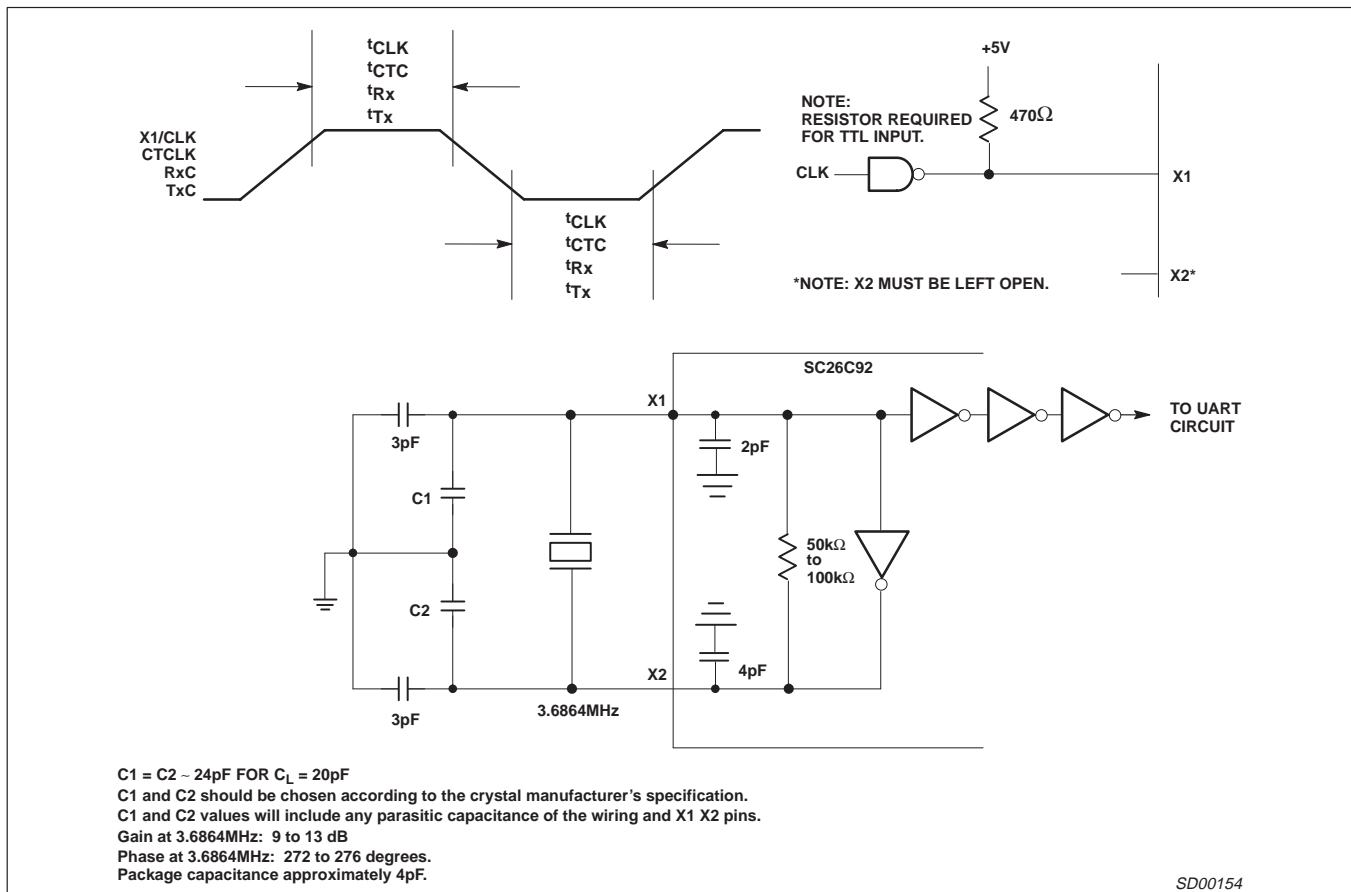


Figure 10. Clock Timing

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

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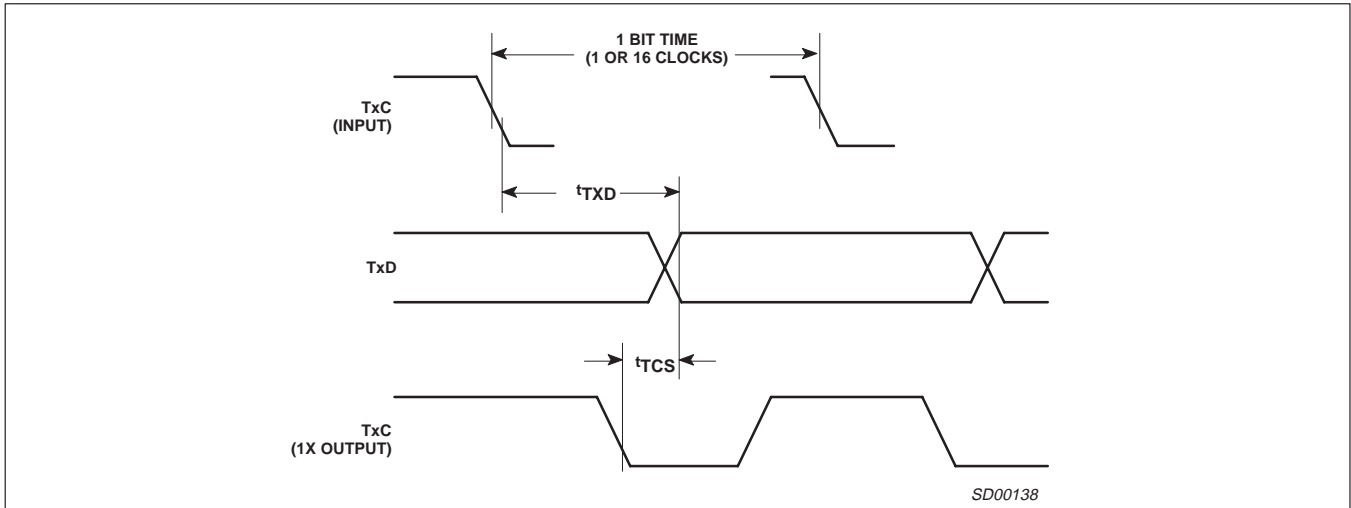


Figure 11. Transmitter External Clocks

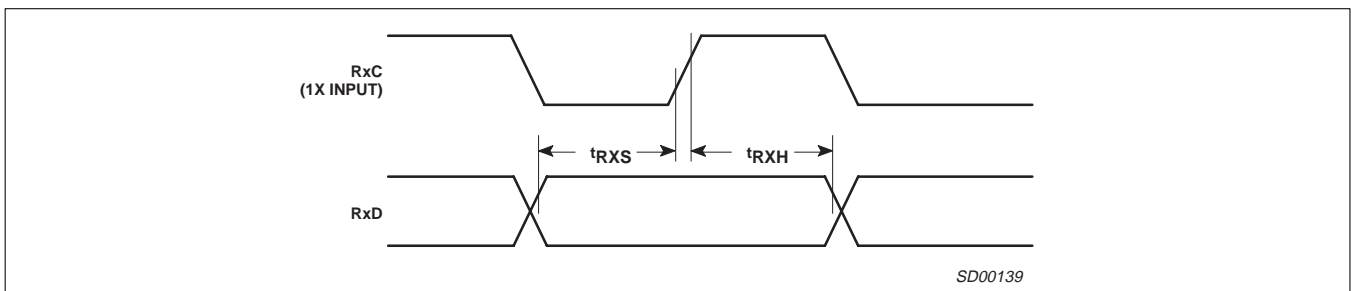
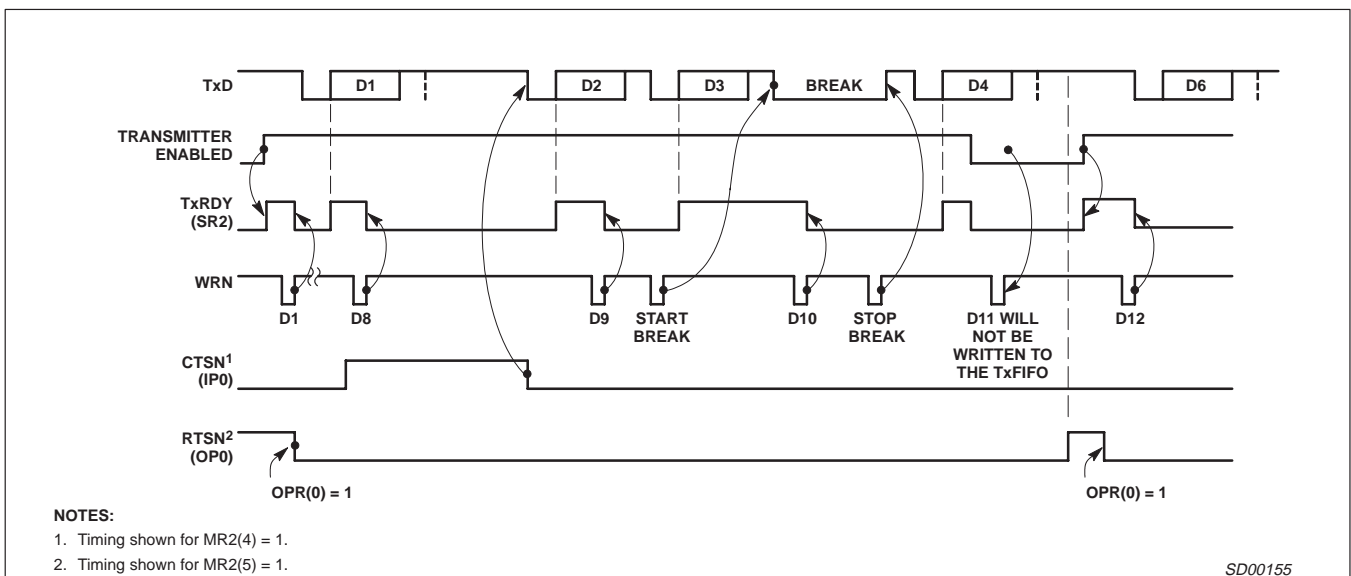


Figure 12. Receiver External Clock



- NOTES:
1. Timing shown for MR2(4) = 1.
  2. Timing shown for MR2(5) = 1.

Figure 13. Transmitter Timing

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# Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

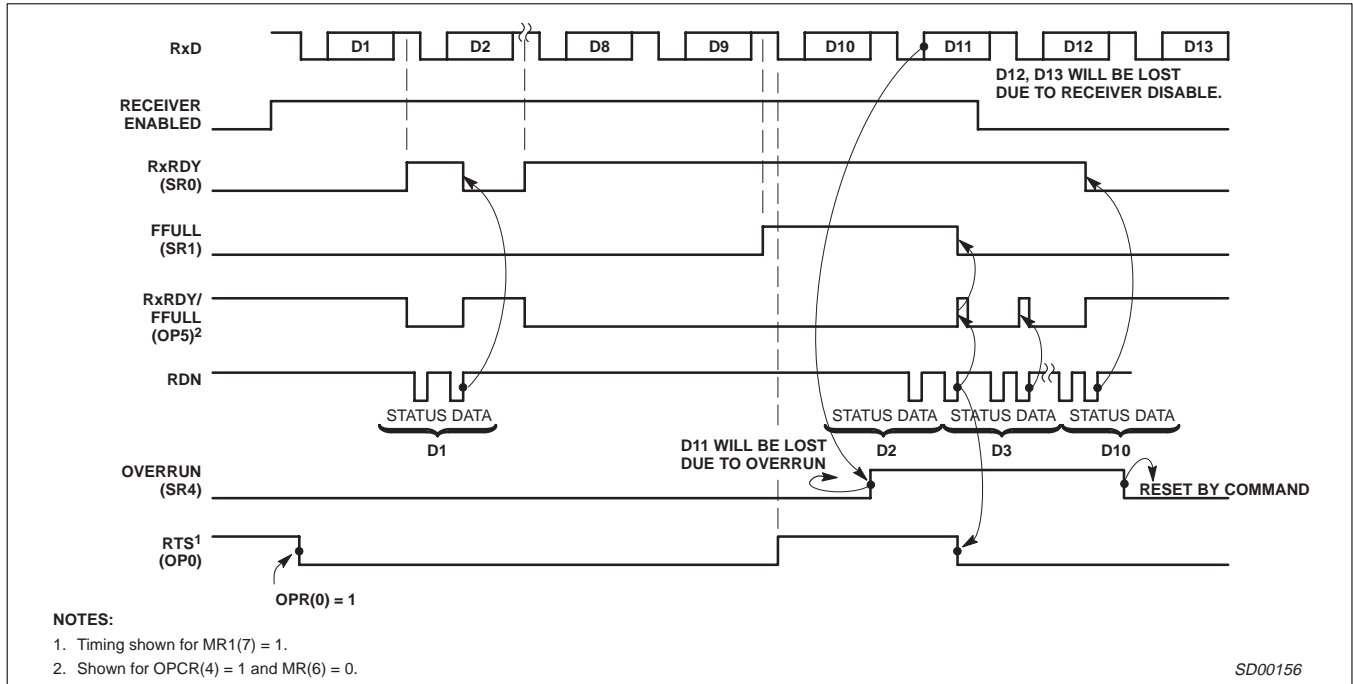


Figure 14. Receiver Timing

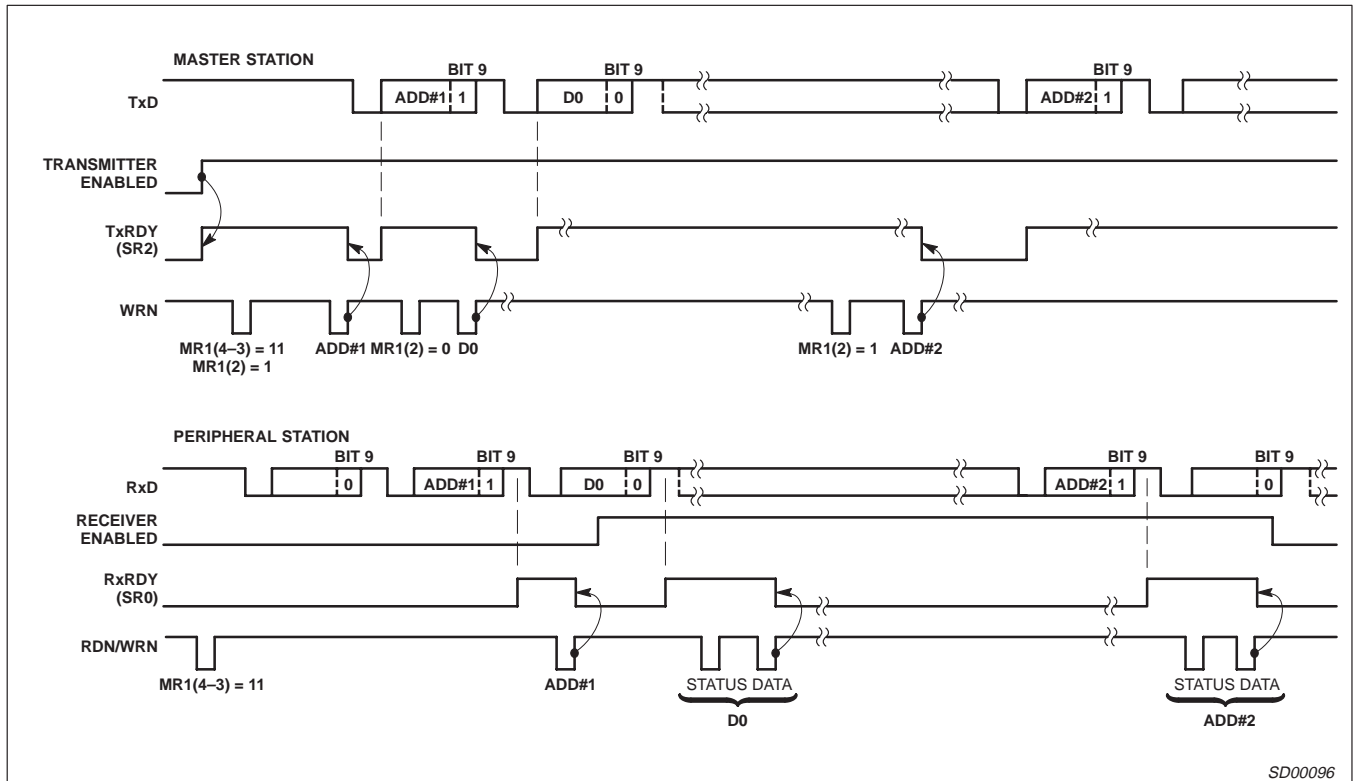


Figure 15. Wake-Up Mode



# Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

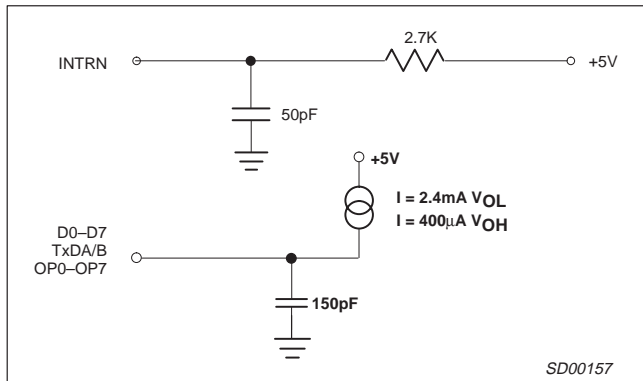


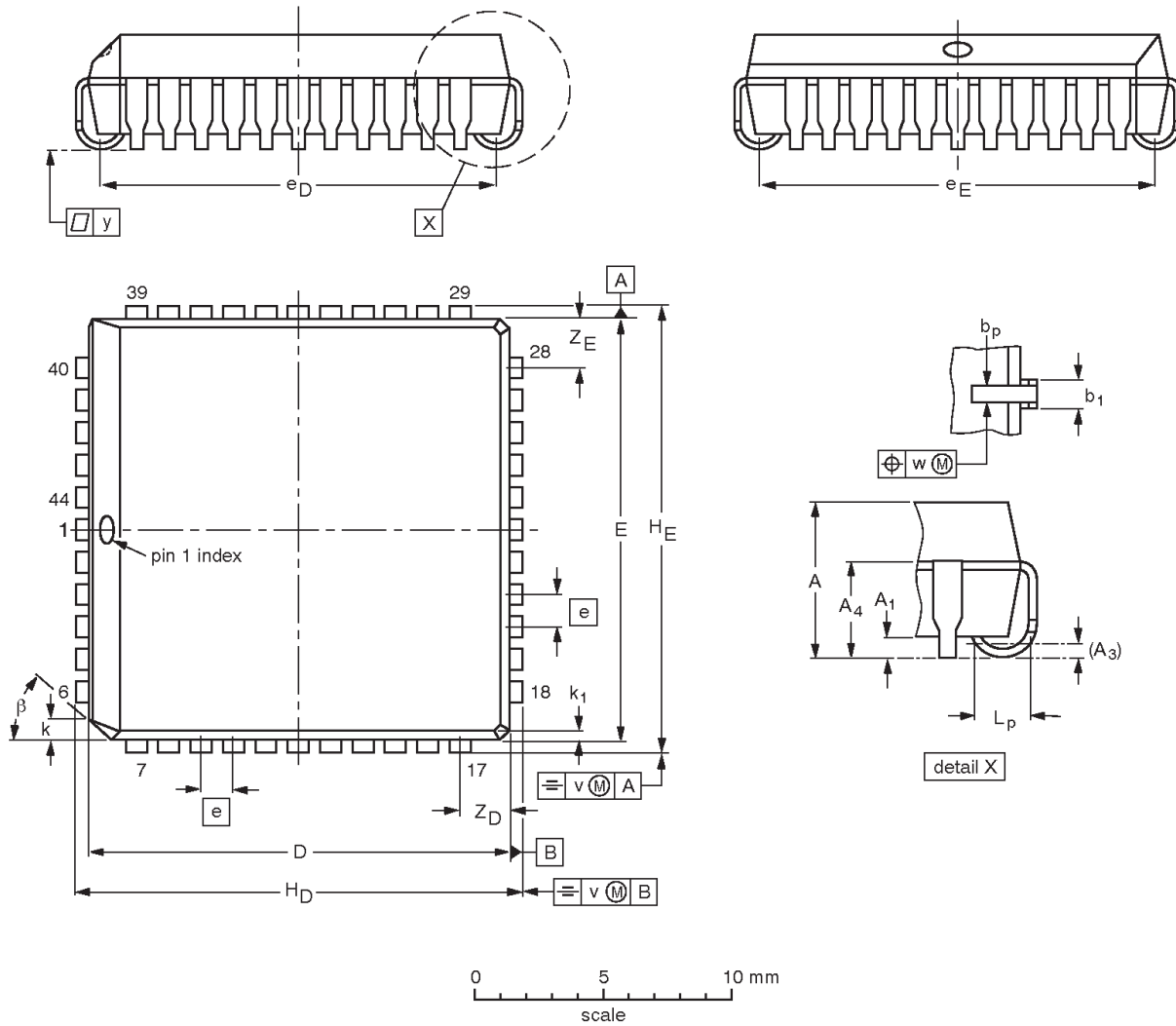
Figure 16. Test Conditions on Outputs

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

## SC28L92

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

UNIT	A	A <sub>1</sub> min.	A <sub>3</sub>	A <sub>4</sub> max.	b <sub>p</sub>	b <sub>1</sub>	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>D</sub>	e <sub>E</sub>	H <sub>D</sub>	H <sub>E</sub>	k	k <sub>1</sub> max.	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup> max.	Z <sub>E</sub> <sup>(1)</sup> max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

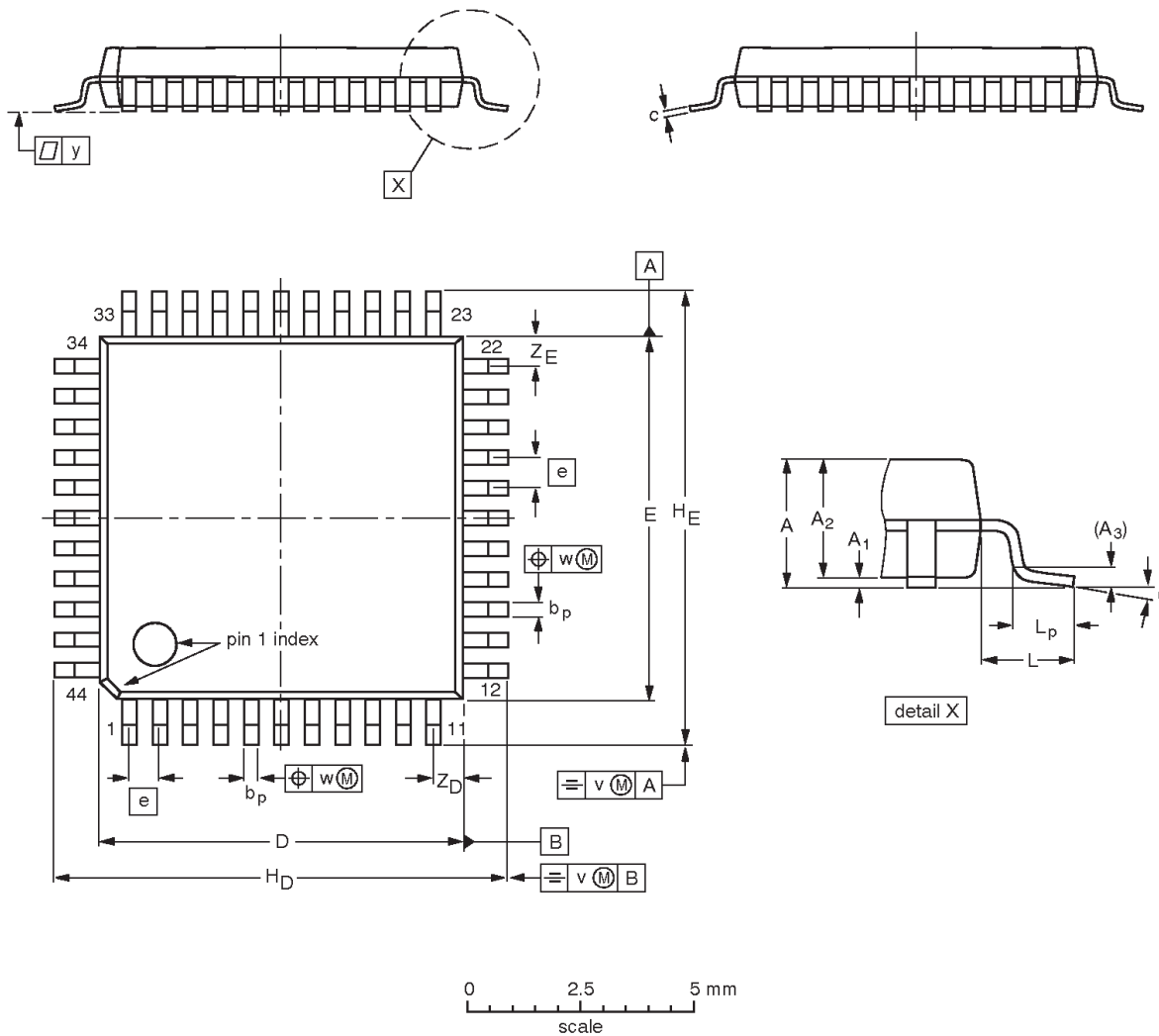
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				95-02-25 97-12-16

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

## SC28L92

**QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm**

**SOT307-2**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						95-02-04 97-08-01

# Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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Date of release: 10-98

Document order number:

9397 750 04465

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