

# DATA SHEET

## **TDA8772; TDA8772A** Triple 8-bit video digital-to-analog converter

Product specification  
Supersedes data of May 1994  
File under Integrated Circuits, IC02

1995 Mar 09

**Philips Semiconductors**



**PHILIPS**

## Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### FEATURES

- 8-bit resolution
- Sampling rate up to  
35 MHz for TDA8772H/3, TDA8772AH/3  
85 MHz for TDA8772H/8, TDA8772AH/8
- Internal reference voltage regulator
- No deglitching circuit required
- $\overline{\text{SYNC}}$ ,  $\overline{\text{BLANK}}$  control inputs
- 3 independent clock inputs (one per DAC)
- 1 V output voltage range
- 75  $\Omega$  output load
- TDA8772A has  $\overline{\text{BLANK}}$  control input on the GREEN channel only while TDA8772 has it on the 3 channels
- Single 5 V power supply
- 44-pin QFP package.

### APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8772H/3	44	QFP44	plastic	SOT307B	35 MHz
TDA8772AH/3	44	QFP44	plastic	SOT307B	35 MHz
TDA8772H/8	44	QFP44	plastic	SOT307B	85 MHz
TDA8772AH/8	44	QFP44	plastic	SOT307B	85 MHz

### GENERAL DESCRIPTION

The TDA8772, TDA8772A are triple 8-bit video digital-to-analog converters (DACs). They convert the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772H/3, TDA8772AH/3) and 85 MHz (TDA8772H/8, TDA8772AH/8).

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DDA</sub>	analog supply voltage		4.5	5.0	5.5	V
V <sub>DDD</sub>	digital supply voltage		4.5	5.0	5.5	V
I <sub>DDA</sub>	analog supply current	R <sub>L</sub> = 75 Ω; note 1	40	65	100	mA
I <sub>DDD</sub>	digital supply current TDA8772H/3, TDA8772AH/3 TDA8772H/8, TDA8772AH/8		–	7	16	mA
			–	16	27	mA
INL	integral non-linearity <sup>2</sup>	f <sub>clk</sub> = 35 MHz; ramp input	–	±0.5	±1	LSB
		f <sub>clk</sub> = 85 MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	f <sub>clk</sub> = 35 MHz; ramp input	–	±0.25	±0.5	LSB
		f <sub>clk</sub> = 85 MHz; ramp input	–	±0.5	±0.75	LSB
f <sub>clk(max)</sub>	maximum clock frequency TDA8772H/3, TDA8772AH/3 TDA8772H/8, TDA8772AH/8		35	–	–	MHz
			85	–	–	MHz
P <sub>tot</sub>	total power dissipation TDA8772H/3, TDA8772AH/3 TDA8772H/8, TDA8772AH/8	note 1				
		R <sub>L</sub> = 75 Ω; f <sub>clk</sub> = 35 MHz	180	360	640	mW
	R <sub>L</sub> = 75 Ω; f <sub>clk</sub> = 85 MHz	180	405	700	mW	

### Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### BLOCK DIAGRAMS

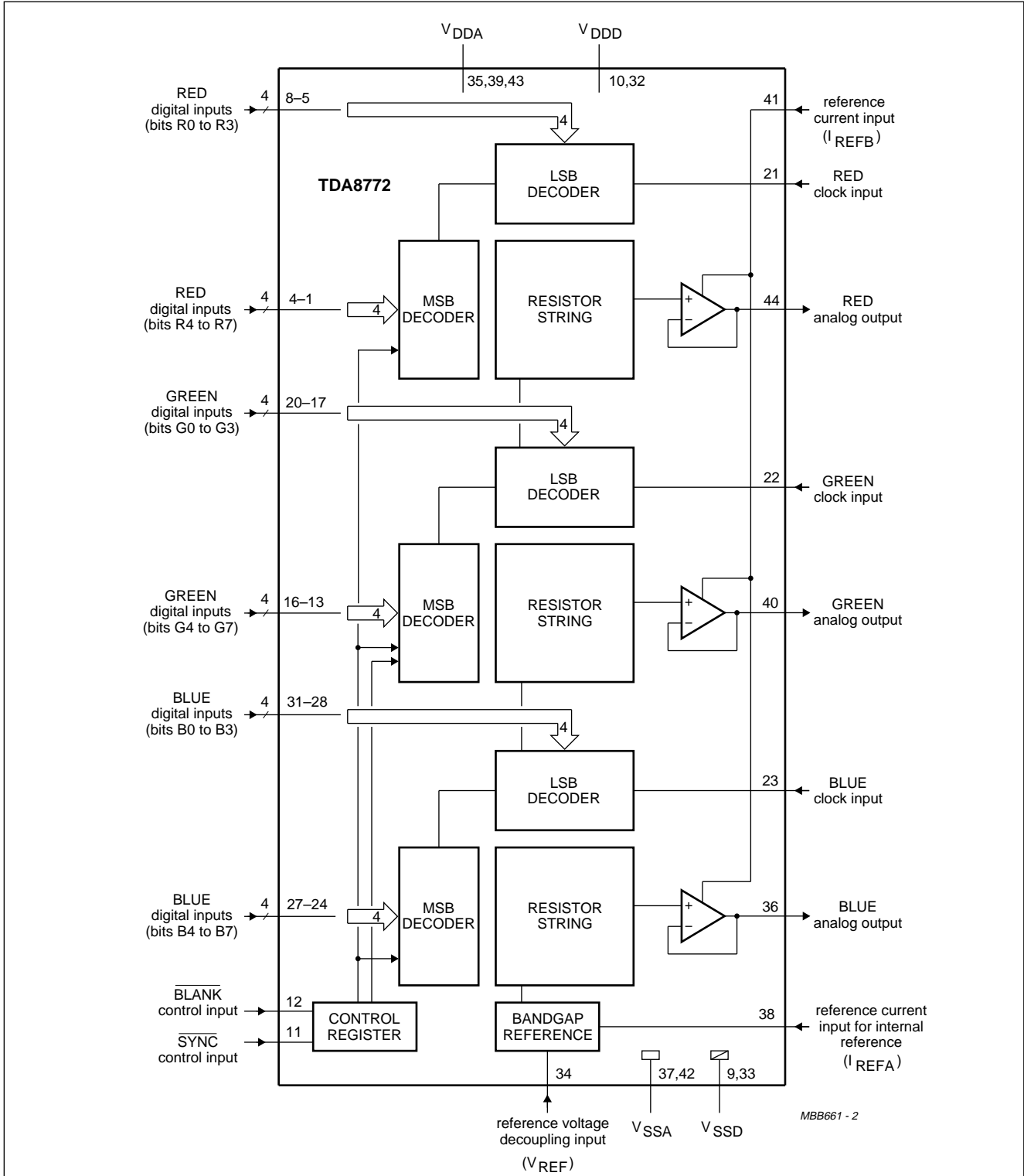


Fig.1 Block diagram for TDA8772.

# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

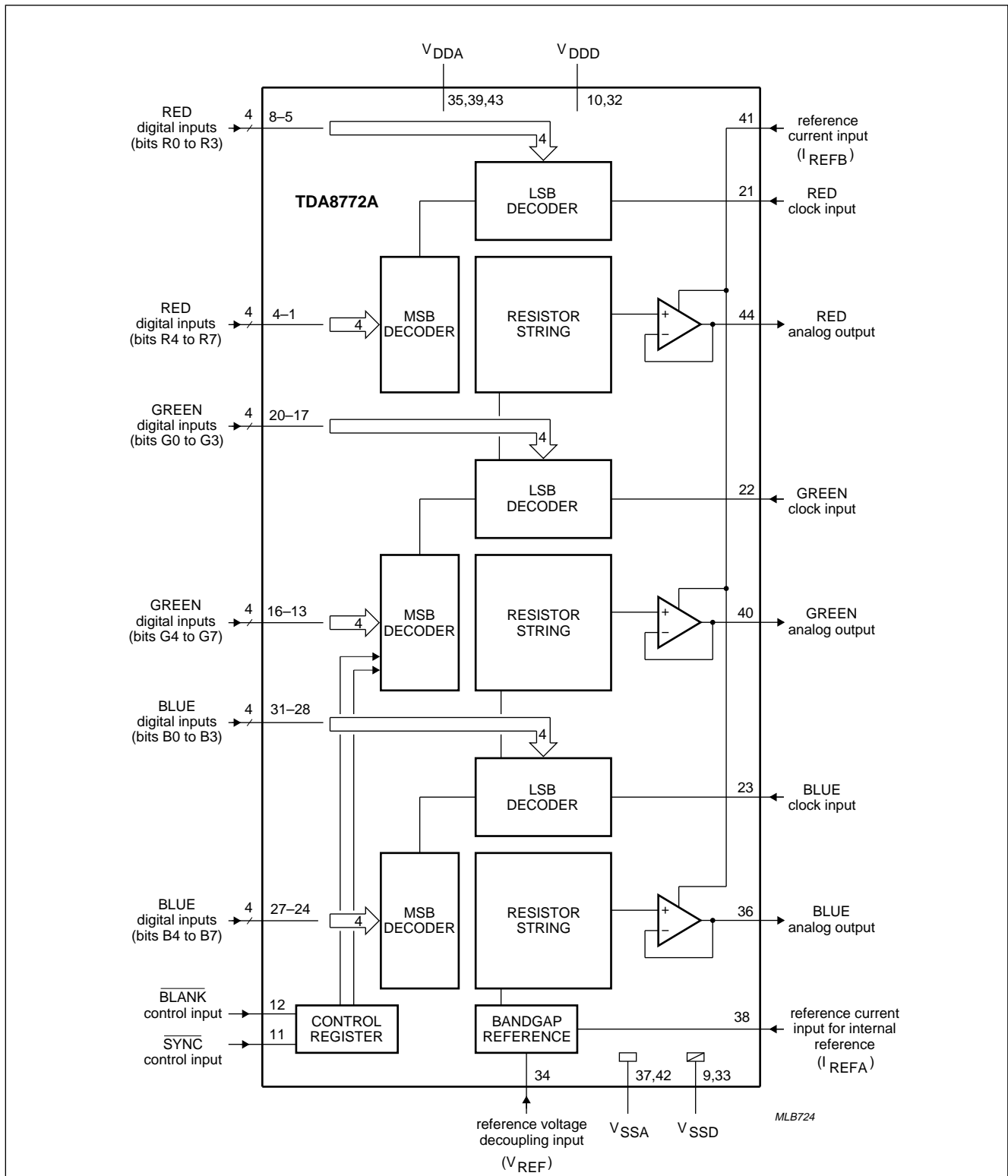


Fig.2 Block diagram for TDA8772A.

# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### PINNING

SYMBOL	PIN	DESCRIPTION
R7	1	RED digital input data; bit 7 (MSB)
R6	2	RED digital input data; bit 6
R5	3	RED digital input data; bit 5
R4	4	RED digital input data; bit 4
R3	5	RED digital input data; bit 3
R2	6	RED digital input data; bit 2
R1	7	RED digital input data; bit 1
R0	8	RED digital input data; bit 0 (LSB)
V <sub>SSD1</sub>	9	digital supply ground 1
V <sub>DD1</sub>	10	digital supply voltage 1
$\overline{\text{SYNC}}$	11	composite sync control input; for GREEN channel only (active LOW)
$\overline{\text{BLANK}}$	12	composite blank control input (active LOW)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
CLKR	21	RED clock input
CLKG	22	GREEN clock input
CLKB	23	BLUE clock input
B7	24	BLUE digital input data; bit 7 (MSB)
B6	25	BLUE digital input data; bit 6
B5	26	BLUE digital input data; bit 5
B4	27	BLUE digital input data; bit 4
B3	28	BLUE digital input data; bit 3
B2	29	BLUE digital input data; bit 2
B1	30	BLUE digital input data; bit 1
B0	31	BLUE digital input data; bit 0 (LSB)
V <sub>DD2</sub>	32	digital supply voltage 2
V <sub>SS2</sub>	33	digital supply ground 2
V <sub>REF</sub>	34	decoupling input for reference voltage
V <sub>DDA1</sub>	35	analog supply voltage 1
OUTB	36	BLUE analog output
V <sub>SSA1</sub>	37	analog supply ground 1
I <sub>REFA</sub>	38	reference current input for internal reference
V <sub>DDA2</sub>	39	analog supply voltage 2
OUTG	40	GREEN analog output

Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

SYMBOL	PIN	DESCRIPTION
I <sub>REFB</sub>	41	reference current input for output buffers
V <sub>SSA2</sub>	42	analog supply ground 2
V <sub>DDA3</sub>	43	analog supply voltage 3
OUTR	44	RED analog output

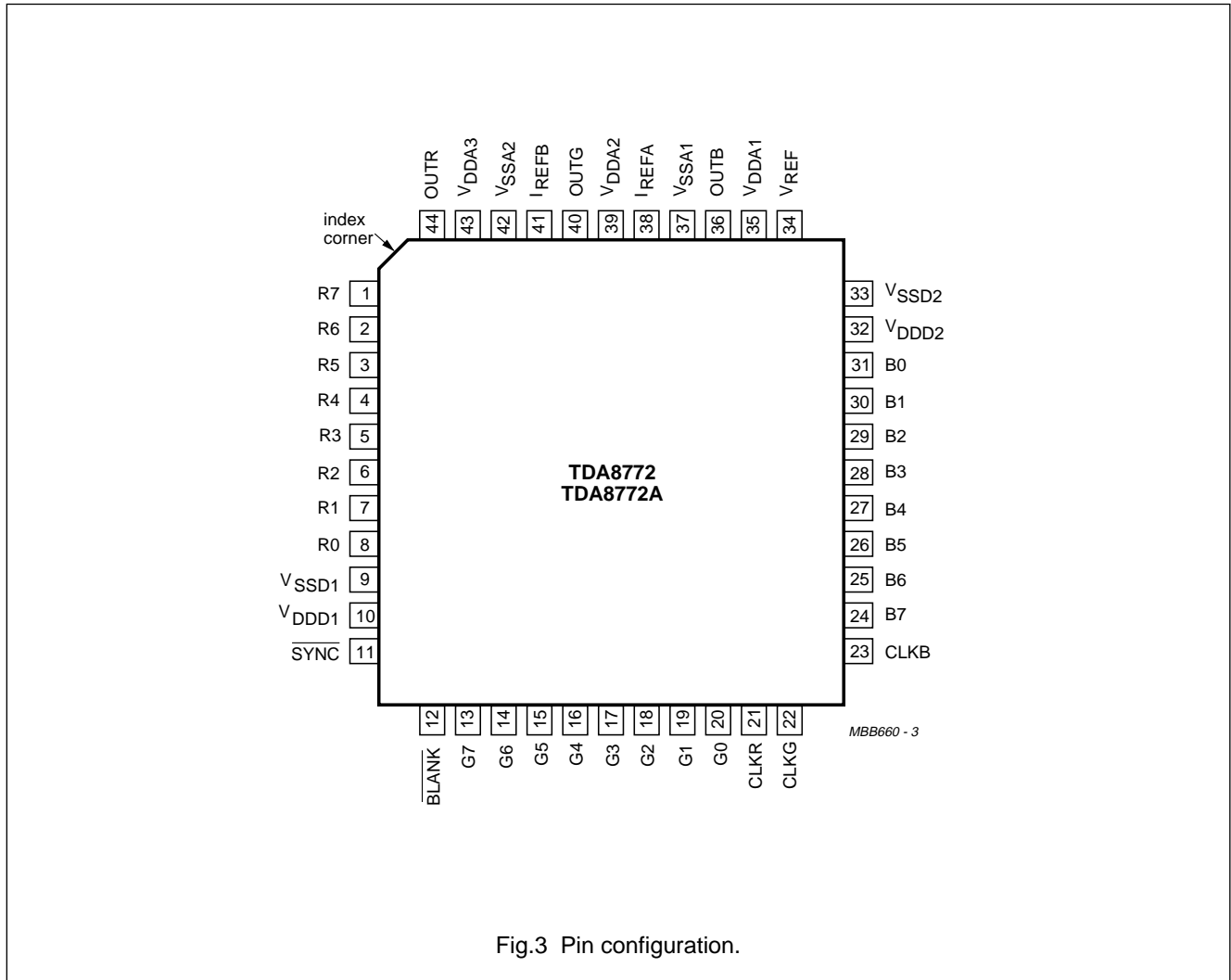


Fig.3 Pin configuration.

## Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DDA}$	analog supply voltage	-0.5	+6.5	V
$V_{DDD}$	digital supply voltage	-0.5	+6.5	V
$\Delta V_{DD}$	supply voltage difference between $V_{DDA}$ and $V_{DDD}$	-1.0	+1.0	V
$T_{stg}$	storage temperature	-55	+150	°C
$T_{amb}$	operating ambient temperature	0	+70	°C
$T_j$	junction temperature	-	+125	°C

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

### HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.



# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### CHARACTERISTICS

TDA8772H/3, TDA8772AH/3 operating at 35 MHz and TDA8772H/8, TDA8772AH/8 operating at 85 MHz unless otherwise specified.

$V_{DDA} = V_{DDD} = 4.5 \text{ V to } 5.5 \text{ V}$ ;  $V_{SSA}$  and  $V_{SSD}$  shorted together;  $V_{DDA} - V_{DDD} = -0.5 \text{ V to } +0.5 \text{ V}$ ;  $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$ ; typical values measured at  $V_{DDA} = V_{DDD} = 5 \text{ V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{DDA}$	analog supply voltage		4.5	5.0	5.5	V
$V_{DDD}$	digital supply voltage		4.5	5.0	5.5	V
$I_{DDA}$	analog supply current	$R_L = 75 \text{ } \Omega$ ; note 1	40	65	100	mA
$I_{DDD}$	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
<b>Inputs</b>						
CLOCK INPUTS (PINS 21, 22 AND 23)						
$V_{IL}$	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
BLANK, SYNC INPUTS (PINS 12 AND 11; ACTIVE LOW)						
$V_{IL}$	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
R, G, B DIGITAL INPUTS (PINS 1 TO 8, 13 TO 20 AND 24 TO 31)						
$V_{IL}$	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
$I_{REFA}$ INTERNAL REFERENCE SUPPLY CURRENT (PIN 38)						
$I_I$	input current		–	0.17	0.25	mA
$I_{REFB}$ OUTPUT BUFFER SUPPLY CURRENT (PIN 41)						
$I_I$	input current		–	0.5	0.7	mA
<b>Timing (<math>C_L = 25 \text{ pF}</math>; <math>R_L = 75 \text{ } \Omega</math>); see Fig.4</b>						
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
$t_{CPH}$	clock pulse width HIGH		5	–	–	ns
$t_{CPL}$	clock pulse width LOW		5	–	–	ns
$t_r$	clock rise time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
$t_f$	clock fall time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns

Triple 8-bit video digital-to-analog  
converter

TDA8772; TDA8772A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Voltage reference (pin 34, referenced to V<sub>SSA</sub>)</b>						
V <sub>REF</sub>	output reference voltage		1.180	1.242	1.305	V
<b>Outputs</b>						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 36, 44 AND 40, REFERENCED TO V <sub>SSA</sub> ) FOR 75 Ω LOAD; see Tables 1 and 2						
FSR	full-scale output voltage range		0.9	1.0	1.1	V
V <sub>os</sub>	offset of analog voltage output		0.75	0.83	0.95	V
V <sub>OUTmax</sub>	maximum output voltage	data inputs = logic 1; note 2	1.65	1.83	2.05	V
V <sub>OUTmin</sub>	minimum output voltage	data inputs = logic 0; note 2	0.75	0.83	0.95	V
THD	total harmonic distortion	f <sub>i</sub> = 4.43 MHz; f <sub>clk</sub> = 35 MHz	–	–45	–	dB
		f <sub>i</sub> = 4.43 MHz; f <sub>clk</sub> = 85 MHz	–	–43	–	dB
Z <sub>L</sub>	output load impedance		60	75	90	Ω
<b>Transfer function</b>						
INL	integral non-linearity	f <sub>clk</sub> = 35 MHz; ramp input	–	±0.5	±1	LSB
		f <sub>clk</sub> = 85 MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	f <sub>clk</sub> = 35 MHz; ramp input	–	±0.25	±0.5	LSB
		f <sub>clk</sub> = 85 MHz; ramp input	–	±0.5	±0.75	LSB
α <sub>CT</sub>	crosstalk DAC to DAC		–45	–	–	dB
	DAC to DAC matching		–	1.0	2.0	%
<b>Switching characteristics (for 75 Ω output load); see Fig.5</b>						
t <sub>d</sub>	input to 50% output delay time	full-scale change	–	10	–	ns
t <sub>s1</sub>	settling time	10% to 90% full-scale change	–	6	–	ns
t <sub>s2</sub>	settling time	to ±1 LSB	–	30	–	ns
<b>Output transients (glitches)</b>						
V <sub>g</sub>	area for 1 LSB change		–	1	–	LSB.ns

**Notes**

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.
2. V<sub>OUT</sub> is directly proportional to V<sub>REF</sub>.

# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

**Table 1** Input coding and DAC output voltages (typical values)

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG $R_L = 75 \Omega$
0000 0000	0	0.830
0000 0001	1	0.834
.... ....	.	.
1000 0000	128	1.330
.... ....	.	.
1111 1110	254	1.826
1111 1111	255	1.830

**Table 2** Input coding and DAC output voltages (typical values)

BINARY INPUT DATA	$\overline{\text{SYNC}}$ (PIN 11)	$\overline{\text{BLANK}}$ (PIN 12)	DAC OUTPUT VOLTAGES (V)		
			OUTG (PIN 40)	OUTR/B (PINS 44, 46) TDA8772	OUTR/B (PINS 44, 46) TDA8772A
.... ....	x	1	see Table 1	see Table 1	see Table 1
.... ....	1	0	0.830	0.830	
.... ....	0	0	0.440		

Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

TIMING

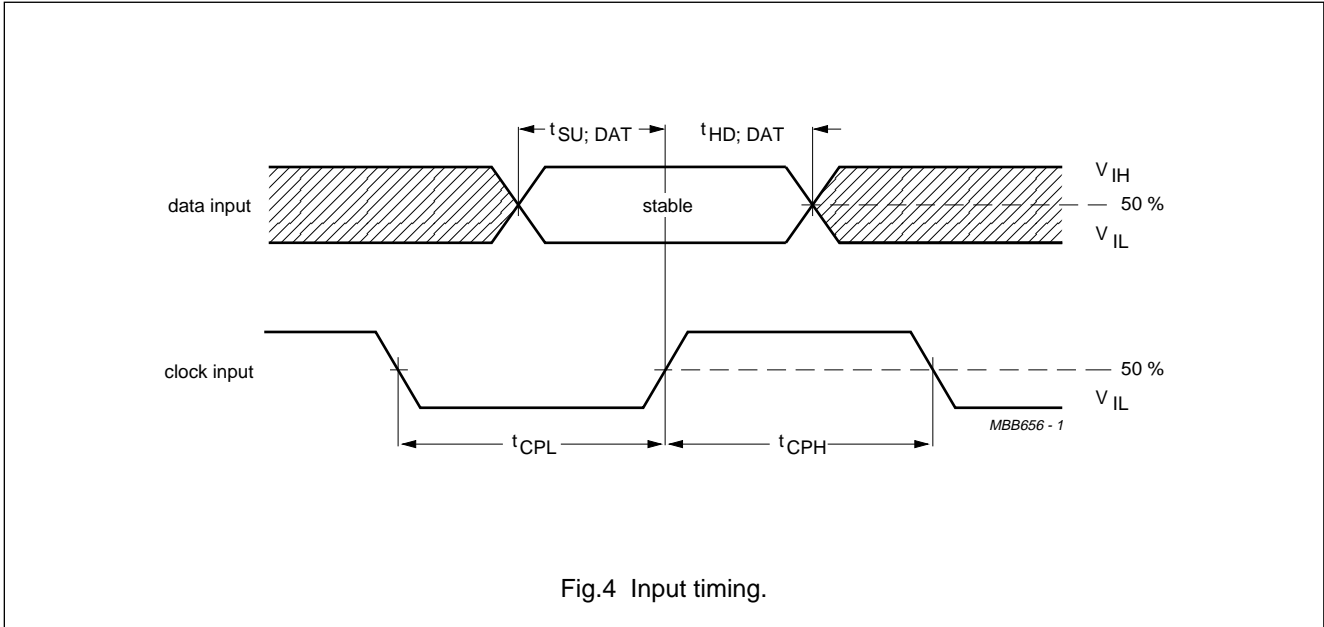


Fig.4 Input timing.

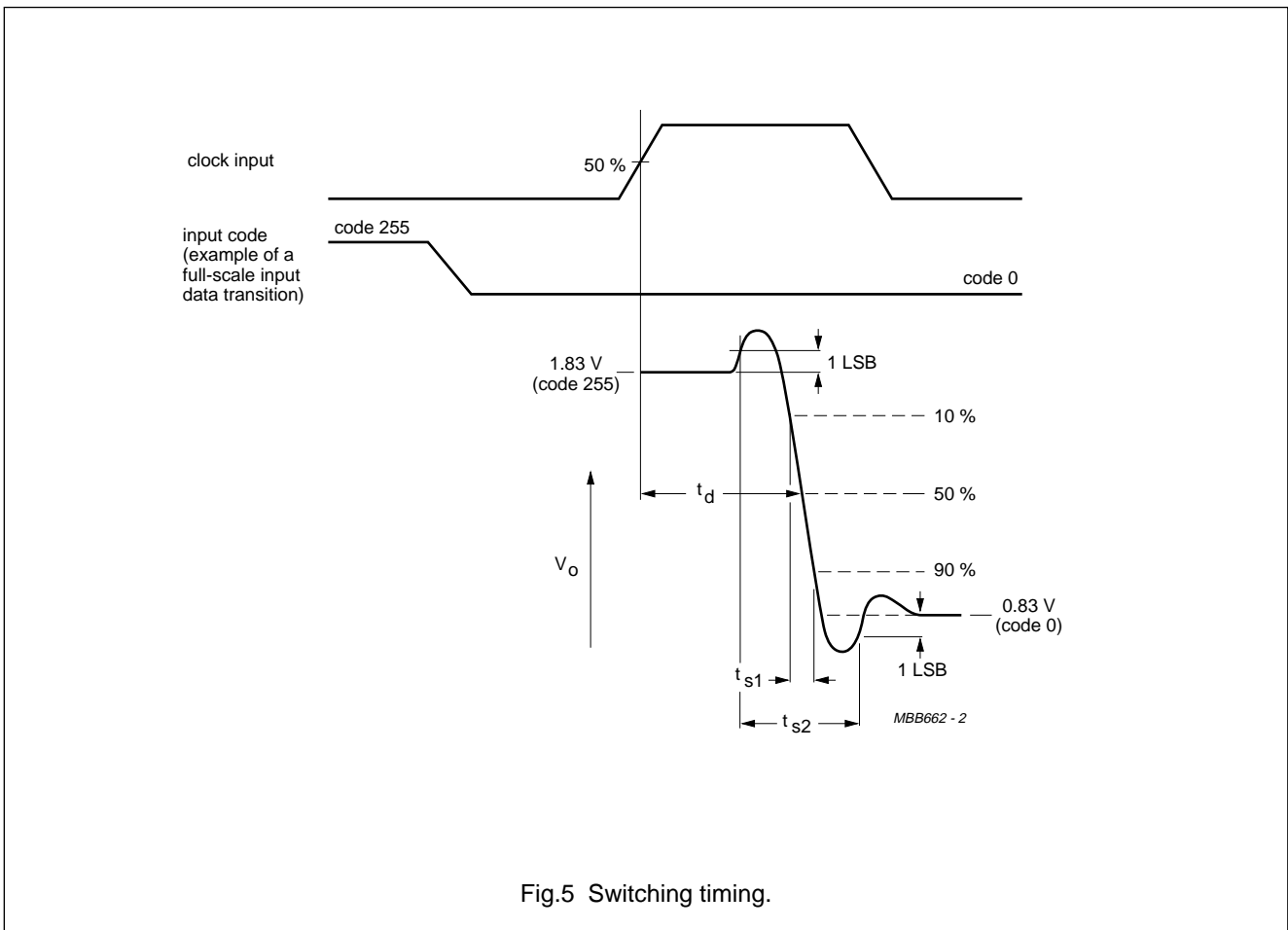
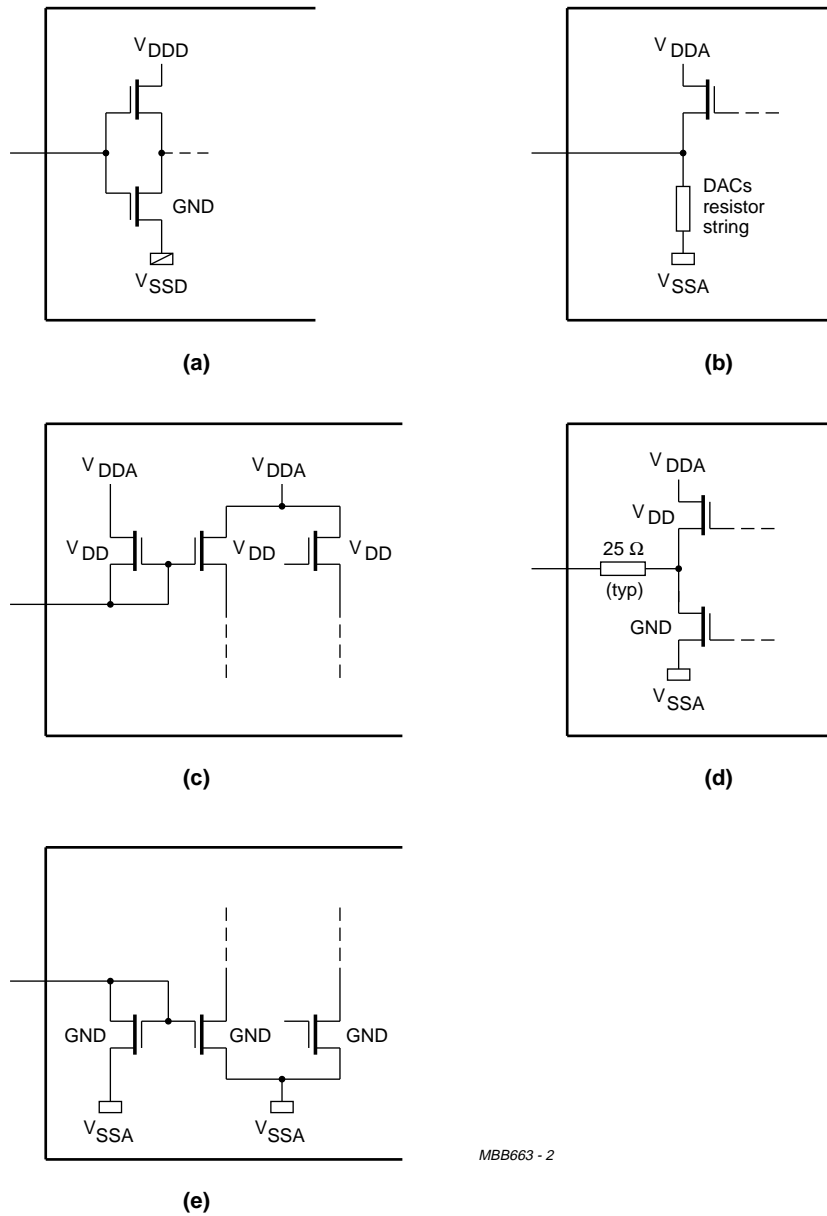


Fig.5 Switching timing.

Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

INTERNAL CIRCUITRY



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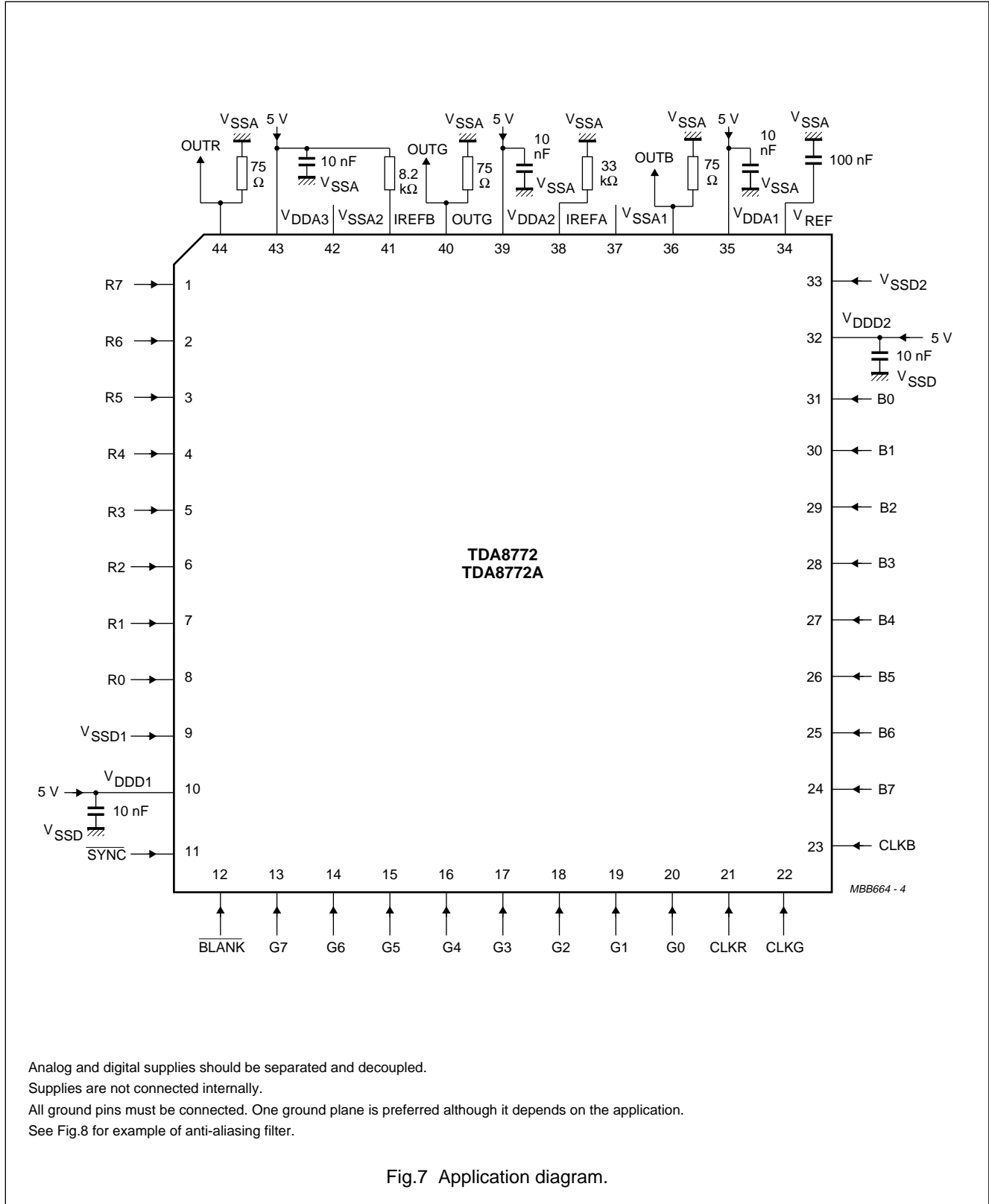
- (a) Digital inputs; pins 1 to 8 and 11 to 31.
- (b) VREF; pin 34.
- (c) IREFA; pin 38.
- (d) OUTR, G, B; pins 44, 40 and 36.
- (e) IREFB; pin 41.

Fig.6 Internal circuitry.

Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

APPLICATION INFORMATION



Analogue and digital supplies should be separated and decoupled.  
 Supplies are not connected internally.  
 All ground pins must be connected. One ground plane is preferred although it depends on the application.  
 See Fig.8 for example of anti-aliasing filter.

Fig.7 Application diagram.

# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

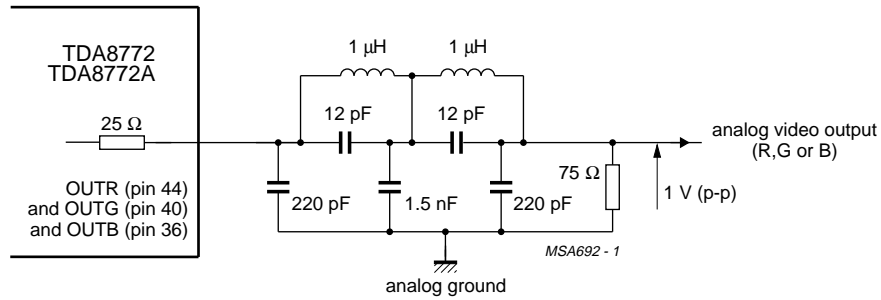


Fig.8 Example of anti-aliasing filter for 1 V output swing.

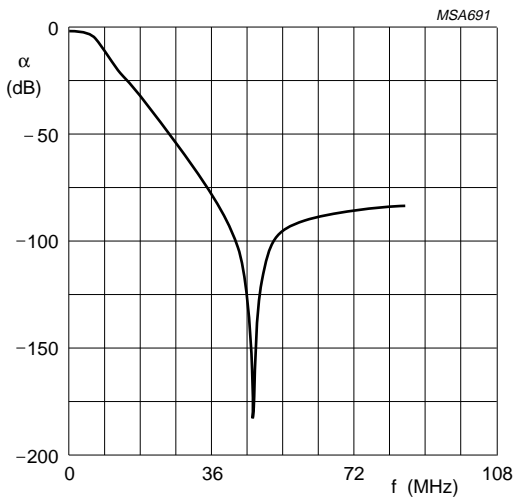


Fig.9 Frequency response for filter shown in Fig.8.

### Characteristics of Fig.9

- Order 5; adapted CHEBYSHEV
- Ripple  $\rho \geq 0.6$  dB
- $f$  at  $-3$  dB = 6.5 MHz
- $f_{\text{NOTCH}} = 46$  MHz.

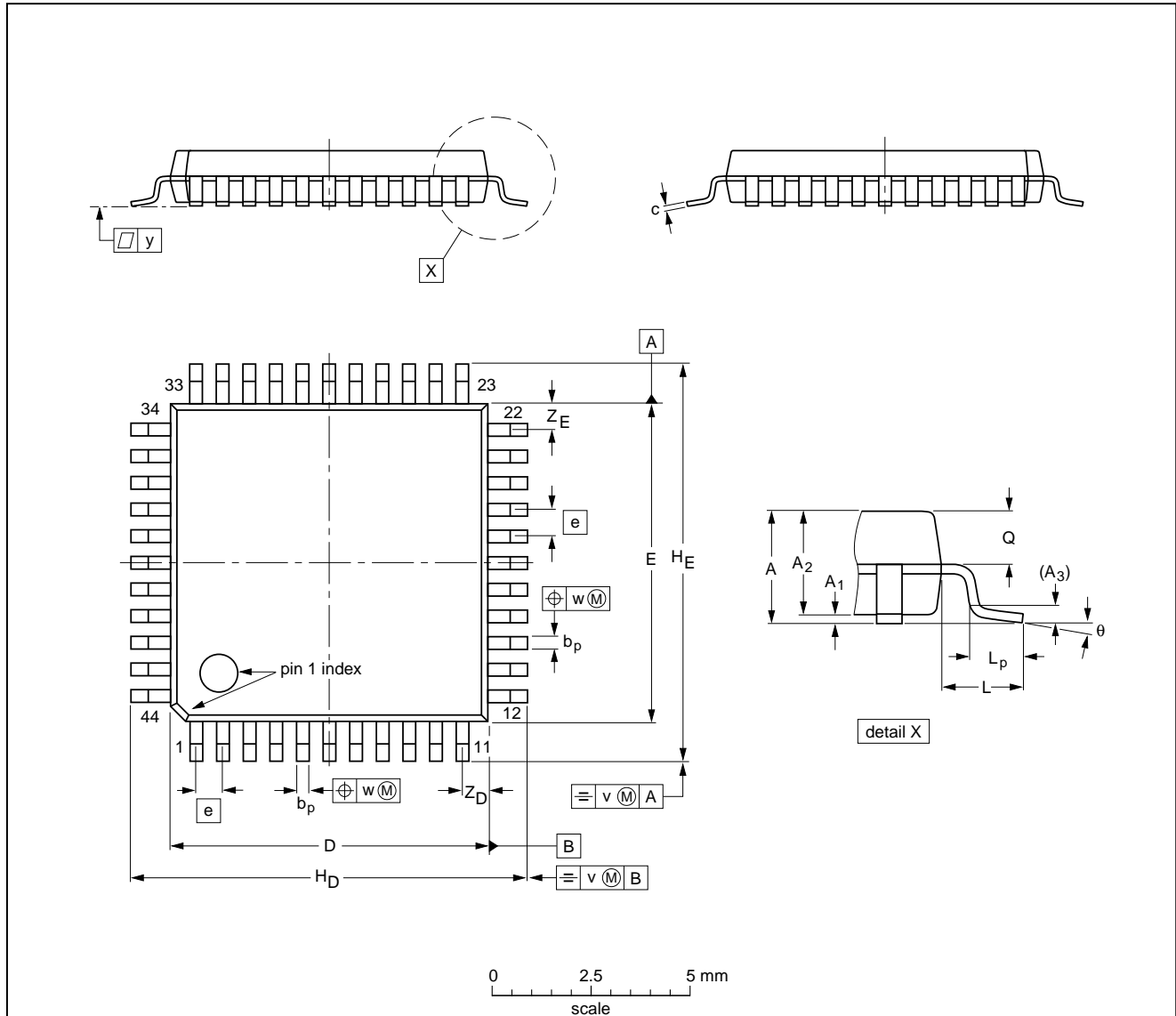
# Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### PACKAGE OUTLINE

**QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm**

**SOT307-2**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						92-11-17 95-02-04



## Triple 8-bit video digital-to-analog converter

## TDA8772; TDA8772A

### SOLDERING

#### Plastic quad flat packages

##### BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

##### BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

##### REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

### DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Triple 8-bit video digital-to-analog  
converter

TDA8772; TDA8772A

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**NOTES**

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Triple 8-bit video digital-to-analog  
converter

TDA8772; TDA8772A

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**NOTES**

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