

## 20-bit input bitstream conversion DAC for digital audio systems

### SAA7350

#### FEATURES

- Up to 20-bit input
- Variety of interface formats (Japanese and I<sup>2</sup>S)
- Choice of two system clock frequencies
- Sampling frequency from 16 kHz to 53 kHz
- Third order noise shaping to increase signal-to-noise ratio
- Bitstream conversion, using switched capacitor one-bit DAC
- Differential mode output configuration
- Single power supply operation (+5 V)
- -10 to +70 °C operating temperature range
- Output interface for TDA1547

#### GENERAL DESCRIPTION

The SAA7350 is a CMOS digital-to-analog converter using Philips bitstream conversion technique. The device is designed for mid/high performance digital audio systems (particularly compact disc). The device also can be used with the TDA1547 device for top performance digital audio systems.



#### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	supply voltage range	4.5	5.0	5.5	V
f <sub>XTAL</sub>	crystal frequency (256 f <sub>s</sub> )	-	11.2896	-	MHz
f <sub>XTAL</sub>	crystal frequency (384 f <sub>s</sub> )	-	16.9344	-	MHz
DR	dynamic range	93	98	-	dB
THD	total harmonic distortion	-	-96	-93	dB
	digital silence	-	-103	-100	dB

#### ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7350GP	44	QPF	plastic	SOT205AG

## 20-bit input bitstream conversion DAC for digital audio systems

SAA7350

## PINNING

SYMBOL	PIN	DESCRIPTION
XSEL	1	crystal frequency select; this pin is used to select the master crystal frequency as follows: XSEL HIGH = 384 $f_s$ , XSEL LOW = 256 $f_s$ ; if unconnected the pin will default HIGH
DOEN	2	one-bit digital output enable; when LOW, the one-bit code outputs are made available for TDA1547; if unconnected the pin will default HIGH
IDF3, IDF2, IDF1	3, 4, 5	input data format; these three pins determine the input format the device is to operate in (see functional description); if unconnected these pins will default HIGH (i.e. burst clock mode)
TEST4	6	test 4; this pin should be left open-circuit
SDI2	7	serial data input; used in simultaneous mode only (for the right channel signal); when not used, this pin will be internally pulled HIGH
SDI1	8	serial data input; this should be a 16, 18 or 20-bit linear 2's complement PCM signal; in simultaneous mode this pin is used for the left channel signal
WSI	9	serial input word select signal; signifies whether data word is for the left or right channel; can be either $f_s$ , 2 $f_s$ , 4 $f_s$ or 8 $f_s$ , where $f_s$ is the system sampling frequency; $f_s$ can be between 16 kHz and 53 kHz
SCKI	10	bit clock input for the serial input interface
TEST1	11	test 1; this pin should be left open-circuit
V <sub>DD</sub>	12	+5 V power supply for the digital section
V <sub>SS</sub>	13	ground connection for the digital section
XIN	14	crystal oscillator input
XOUT	15	crystal oscillator output
XSYS1	16	buffered oscillator output
TEST5	17	test 5; in normal operation this pin should be tied LOW
V <sub>DDAR</sub>	18	analog 5 V supply for right channel
INTR+	19	output from the right positive switched-capacitor integrator; input to differential operational amplifier
FBR+	20	feedback connection for the right positive switched-capacitor integrator
V <sub>SSAR</sub>	21	0 V supply for right channel
FBR-	22	feedback connection for the right negative switched-capacitor integrator
INTR-	23	output from the right negative switched-capacitor integrator; input to differential operational amplifier
V <sub>RCR</sub>	24	high impedance voltage reference for right channel inputs; typically V <sub>DDAR</sub> /2
V <sub>DACR</sub>	25	reference voltage supply for right channel DAC's; normally this will be connected to V <sub>SS</sub>
V <sub>ROR</sub>	26	right channel voltage reference output; typically V <sub>DDAR</sub> /2
V <sub>DDATR</sub>	27	5 V supply for right channel analog timing
V <sub>SSAT</sub>	28	0 V supply for left and right channel analog timing
V <sub>DDATL</sub>	29	5 V supply for left channel analog timing
IRR	30	24 k $\Omega$ bias resistor connection for the reference current generator circuit



---

**20-bit input bitstream conversion  
DAC for digital audio systems**


---

**SAA7350****PINNING**

SYMBOL	PIN	DESCRIPTION
V <sub>ROL</sub>	31	left channel voltage reference output; typically V <sub>DDAL</sub> /2
V <sub>DAFL</sub>	32	reference voltage supply for left channel DAC; normally this will be connected to V <sub>SS</sub>
V <sub>RCL</sub>	33	high impedance voltage reference for left channel inputs and for bias current generator; typically V <sub>DDAL</sub> /2
INTL-	34	output from the left negative switched-capacitor integrator; input to differential operational-amplifier
FBL-	35	feedback connection for the left negative switched-capacitor integrator
V <sub>SSAL</sub>	36	0 V supply for left channel
FBL+	37	feedback connection for the left positive switched-capacitor integrator
INTL+	38	output from the left positive switched-capacitor integrator; input to differential operational-amplifier
V <sub>DDAL</sub>	39	analog 5 V supply for left channel
TEST2	40	test 2; this pin should be left open-circuit
TEST3	41	test 3; this pin should be left open-circuit
DOL	42	digital output left; left channel one-bit code for TDA1547; when disabled this pin will be driven LOW
XSYS2	43	output clock at a frequency of half the master clock frequency
DOR	44	digital output right; right channel one-bit code for TDA1547; when disabled this pin will be driven LOW

20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

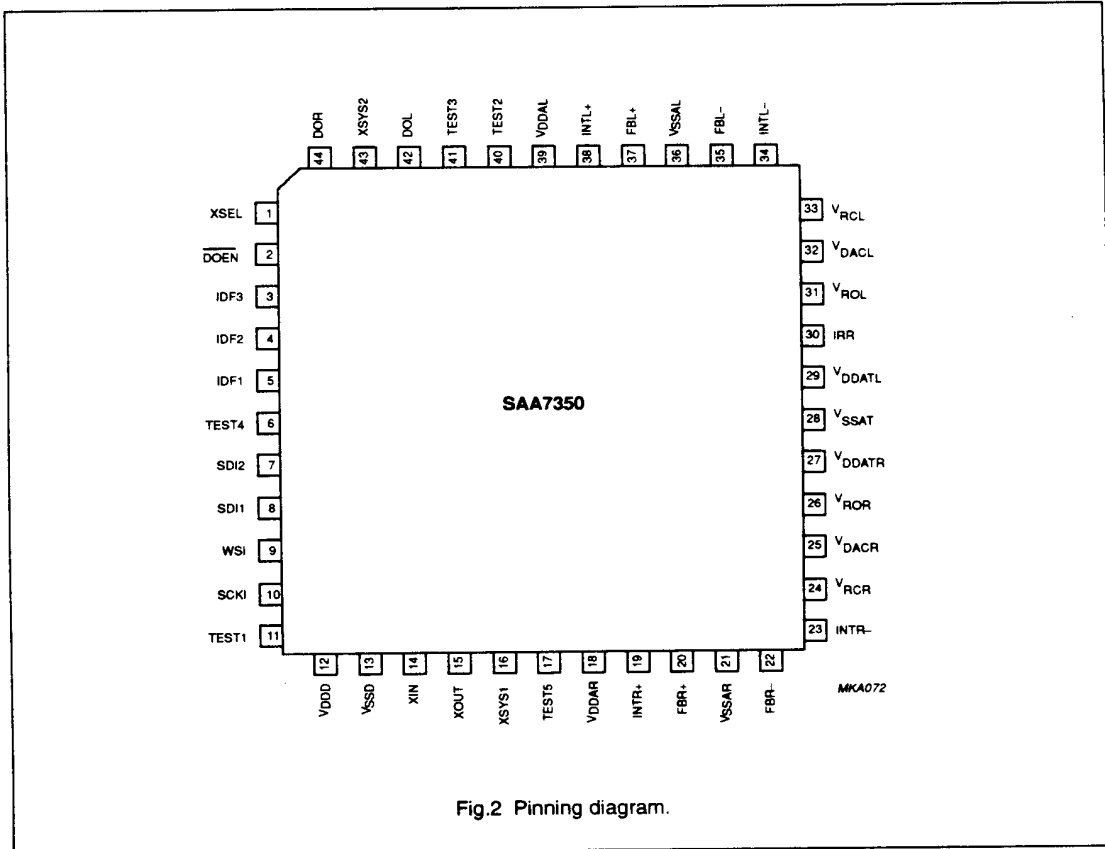


Fig.2 Pinning diagram.

## 20-bit input bitstream conversion DAC for digital audio systems

SAA7350

### FUNCTIONAL DESCRIPTION

#### General

The SAA7350 bitstream conversion CMOS DAC contains a flexible interface supporting a variety of formats. This enables it to be used with a number of available digital filters with wordlengths of up to 20 bits and upsampling up to 8  $f_s$ . The system sampling frequency ( $f_s$ ) can be between 16 kHz and 53 kHz.

The analog section contains four one-bit DACs operated in differential mode to achieve high performance signal-to-noise ratio, channel separation and total harmonic distortion.

#### Input interface

The SAA7350 supports the following modes:

- I<sup>2</sup>S with dataword rates of  $f_s$ , 2  $f_s$  or 4  $f_s$  with wordlengths of up to 20 bits (see Fig. 3). A minimum of 16 bit-clock cycles per word is required.
- Sony serial format for dataword rate of  $f_s$ , 2  $f_s$  or 4  $f_s$  with wordlengths of 16, 18 or 20 bits (see Fig. 4). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of  $f_s$ , 2  $f_s$ , 4  $f_s$  or 8  $f_s$  with wordlengths of up to 20 bits idling on the least significant bit (see Fig. 5). A minimum of 16 bit-clock cycles per word is required.
- Simultaneous mode for dataword rates of  $f_s$ , 2  $f_s$ , 4  $f_s$  and 8  $f_s$  with wordlengths of 18 or 20 bits idling on the MSB (see Fig. 6). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of  $f_s$ , 2  $f_s$ , 4  $f_s$  or 8  $f_s$  with wordlengths of up to 20 bits using burst clocks (see Fig. 7). A minimum of 16 bit-clock cycles is required. This mode is restricted to having the bit clock at less than or equal to half the master clock frequency supplied to the SAA7350.

The choice of these formats is given by the pins IDF1 to IDF3 as shown below.

#### Input data formats

IDF3	IDF2	IDF1	format
0	0	0	I <sup>2</sup> S format up to 20 bits
0	0	1	Sony serial format 16 bits
0	1	0	Sony serial format 18 bits
0	1	1	Sony serial format 20 bits
1	0	0	simultaneous format idling on LSB up to 20 bits
1	0	1	simultaneous format idling on MSB 18 bits
1	1	0	simultaneous format idling on MSB 20 bits
1	1	1	simultaneous format burst clock up to 20 bits

The transfer on the serial input has to be synchronous to the master clock.

## 20-bit input bitstream conversion DAC for digital audio systems

SAA7350

### Clock frequency

The device can run at an input clock frequency of either  $384 f_s$  or  $256 f_s$  (pin XSEL) outputting a system clock at the same frequency on XSYS1 and half input clock frequency on XSYS2.  $f_s$  can be between 16 kHz and 53 kHz.

### Noise shaping

Third order noise shaping is implemented on the SAA7350 to give an improved signal-to-noise ratio. DC offset and out-of-band dither is added to prevent idle patterns in the audio band.

### Bitstream conversion DAC

The digital-to-analogue conversion in the SAA7350 is performed using the Philips bitstream conversion technique. The input from the digital filter is oversampled to  $8 f_s$  by means of a digital sample and hold and converted to a 1-bit pulse density modulated (PDM) signal. A switched capacitor technique is used for the bitstream conversion to convert the PDM signal to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of an integrator. As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure.

In order to increase the output signal-to-noise ratio and THD performance, internal operational-amplifiers are provided so that the device is operated in differential mode. With this technique, any common mode signals cancel thus improving the signal-to-noise ratio and total harmonic distortion.

### TDA1547 interface

The SAA7350 can also be used to provide oversampling and noise shaping for the TDA1547. One-bit codes and clock outputs are supplied for inputs to the TDA1547.

### LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DDA}$	analog supply voltage; note 1	-0.5	+6.5	V
$V_i$	DC input voltage	-0.5	+6.5	V
$I_{iK}$	DC input diode current	-	$\pm 20$	mA
$V_o$	DC output voltage	-0.5	+6.5	V
$I_o$	DC output source or sink current	-	$\pm 20$	mA
$I_{DD}$ or $I_{SS}$	DC $V_{DD}$ or $V_{SS}$ current (total)	-	$\pm 0.5$	A
$T_{stg}$	storage temperature range	-65	+150	°C
$T_{amb}$	operating ambient temperature range	-10	+70	°C
$V_{es}$	electrostatic handling; note 2	-1000	+1000	V

#### Notes to the limiting values

- All  $V_{DD}$  and  $V_{SS}$  pins must be connected externally to the same power supply unit.
- Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  series resistor with a rise time of 15 ns.

## 20-bit input bitstream conversion DAC for digital audio systems

SAA7350

**CHARACTERISTICS**
 $V_{DD} = 5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $f_{XTAL} = 384\text{ f}_0$ ;  $f_s = 44.1\text{ kHz}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DDA}$	supply voltage (analog)		4.5	5.0	5.5	V
$I_{DDA}$	supply current (analog)		-	45	70	mA
$V_{DD0}$	supply voltage (digital)		4.5	5.0	5.5	V
$I_{DD0}$	supply current (digital)		-	30	50	mA
<b>Digital part:</b>						
<b>Inputs: SCKI, WSI, SDI1</b>						
$V_L$	LOW level input voltage	note 1	-0.5	-	+0.8	V
$V_H$	HIGH level input voltage	note 1	2.0	-	$V_{DD} + 0.5$	V
$I_{LI}$	input leakage current	note 2	-10	0	+10	$\mu\text{A}$
$C_i$	input capacitance		-	-	10	pF
<b>Inputs: XSEL, SD12, DOEN, IDF1, IDF2, IDF3</b>						
		note 3				
$V_L$	LOW level input voltage	note 1	-0.5	-	+0.8	V
$V_H$	HIGH level input voltage	note 1	2.0	-	$V_{DD} + 0.5$	V
$Z_i$	pull-up impedance		-	50	-	k $\Omega$
$C_i$	input capacitance		-	-	10	pF
<b>Crystal oscillator input: XIN</b>						
$V_L$	LOW level input voltage	note 1	-0.5	-	+1.5	V
$V_H$	HIGH level input voltage	note 1	3.5	-	$V_{DD} + 0.5$	V
$I_{LI}$	input leakage current	note 2	-10	0	+10	$\mu\text{A}$
$C_i$	input capacitance		-	-	10	pF
<b>Outputs: XSYS1</b>						
$V_{OL}$	LOW level output voltage	note 1	-0.5	-	+0.4	V
$V_{OH}$	HIGH level output voltage	note 1	2.4	-	$V_{DD} + 0.5$	V
$C_L$	load capacitance		-	-	35	pF
<b>Outputs: XSYS2, DOL, DOR</b>						
$V_{OL}$	LOW level output voltage		-	-	0.5	V
$V_{OH}$	HIGH level output voltage		$V_{DD} - 0.5$	-	-	V
$C_L$	load capacitance		-	-	20	pF
<b>Crystal oscillator: input XIN/output XOUT</b>						
$f_{XTAL}$	operating frequency XTAL	note 4	4.096	256 $f_0$ or 384 $f_0$	20.35	MHz
$G_m$	mutual conductance	100 kHz	1.5	-	-	mA/V
$G_v$	small signal voltage gain	$G_v = G_m \times R_o$	3.5	-	-	V/V
$C_i$	input capacitance		-	-	10	pF



20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Crystal oscillator: input XIN/output XOUT</b>						
$C_{FB}$	feedback capacitance		-	-	5	pF
$C_O$	output capacitance		-	-	10	pF
$I_{LI}$	input leakage current	note 2	-10	-	+10	$\mu$ A
<b>Timing</b>						
<b>External clock input: XIN</b>						
$f_c$	input frequency		4.096	256 $f_s$ or 384 $f_s$	20.35	MHz
$t_r$	input rise time	note 5	-	-	10	ns
$t_f$	input fall time	note 5	-	-	10	ns
$t_{HIGH}$	input HIGH time (relative to clock period)	at 1.5 V	30	-	70	%
<b>System clock output: XSYS1</b>						
		note 6				
$t_r$	output rise time	note 5	-	-	10	ns
$t_f$	output fall time	note 5	-	-	10	ns
$t_{HIGH}$	output HIGH time (relative to clock period)	note 7	-	50	-	%
<b>Data outputs: DOL, DOR</b>						
		see Fig. 8; note 8				
$t_r$	data output rise time		-	10	15	ns
$t_f$	data output fall time		-	10	15	ns
$t_{SU}$	data output set-up time		0	-	-	ns
$t_{HD}$	data output hold time		25	-	-	ns
<b>Data clock output: XSYS2</b>						
		see Fig. 8; note 8				
$t_r$	clock output rise time		-	5	10	ns
$t_f$	clock output fall time		-	5	10	ns
$t_{HIGH}$	clock output HIGH time	note 9	40	-	-	ns
$t_{LOW}$	clock output LOW time	note 9	40	-	-	ns
<b>Input timing</b>						
		see Fig. 9				
<b>Clock input: SCKI</b>						
$f_c$	input clock frequency		0.256	-	20.35	MHz
mSR	mark space ratio		40:60	-	60:40	
<b>Word select input: WSI</b>						
$f_i$	input frequency		14.4	-	424	kHz
<b>Data inputs: SDI1, SDI2/word select input: WSI</b>						
$t_{SU-DAT}$	input set-up time		-	20	-	ns
$t_{HD-DAT}$	input hold time (relative to SCKI)		0	-	-	ns

**20-bit input bitstream conversion  
DAC for digital audio systems**

SAA7350

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Analog part</b>						
<b>Reference voltage source: VRC</b>						
$V_{ref}$	high-impedance reference voltage level		-	2.5	-	V
<b>Outputs: INTL+, INTL-, INTR+, INTR-</b>		notes 10 and 11				
$V_{AO(RMS)}$	output level at 0 dB (RMS value)	note 12	-	0.9	-	V
$V_{DIFF(RMS)}$	application output level at 0 dB (RMS value)	note 13	1.62	1.80	1.98	V
<b>DAC performance</b>		note 12				
DR	dynamic range		93	98	-	dB
THD + N	total harmonic distortion	at 0 dB/1 kHz	-	-96	-93	dB
	digital silence		-	-103	-100	dB
a	channel separation	1 kHz	-	100	-	dB
RR	power supply rejection ratio to $V_{DD}$		-	60	-	dB
	channel matching	note 14	-	-	$\pm 0.25$	dB
le	linearity	0 to -100 dB	-	$\pm 1$	-	dB

**Notes to the characteristics**

- Minimum  $V_{IL}$ ,  $V_{OL}$  and maximum  $V_{IH}$ ,  $V_{OH}$  are peak values to allow for transients.
- $I_{L(MIN)}$  and  $I_{L(MIN)}$  measured at  $V_I = 0$  V;  $I_{L(MAX)}$  and  $I_{L(MAX)}$  measured at  $V_I = V_{DD}$ .
- Pins XSEL and SDI2 are internally pulled high when not connected. XSEL HIGH indicates a crystal frequency of  $384 f_s$ .
- $f_{XTAL}$  is a multiple of the system sampling frequency  $f_s$ .  $f_s$  can be between 16 and 53 kHz.
- Reference levels = 0.8 V and 2.0 V.
- Output times are measured with a capacitive load of 35 pF. XSYS2 is half the master clock frequency. See Fig.10 for relative clock timings.
- $t_{HIGH}$  valid only when used with XTAL, with 50% input mark space ratio. XSYS1  $t_{HIGH}$  is measured at  $V_{DD}/2$ .
- Output times are measured with a capacitive load of 20 pF. XSYS2 is half the master clock frequency. Data output hold time is relative to XSYS2.
- XSYS2 output HIGH/LOW times are for 20.35 MHz. Minimum value for 16.934 MHz is 49 ns.
- Device measured in differential mode with external components shown in recommended application diagram (see Figs 13 and 14). It should be noted that for 1.80 mV output, feedback resistors R16a, R17a, R16b, R17b should be 31.6 k $\Omega$ . Application diagram shows preferred type range values of 30 k $\Omega$  which give  $1.80 \times 30/31.6 = 1.70$  mV.
- Maximum load (excluding feedback) is 10 k $\Omega$ , 100 pF to VRO ( $V_{ref}$ ). Dynamic output impedance is typically 150  $\Omega$ .
- Output level tracks linearly with sampling frequency ( $f_s$ ). DAC performance quoted for 18-bit, 4  $f_s$  input.
- Application output level measured at output from first operational-amplifier stage in Figs 13 and 14.
- With matched external components.

20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

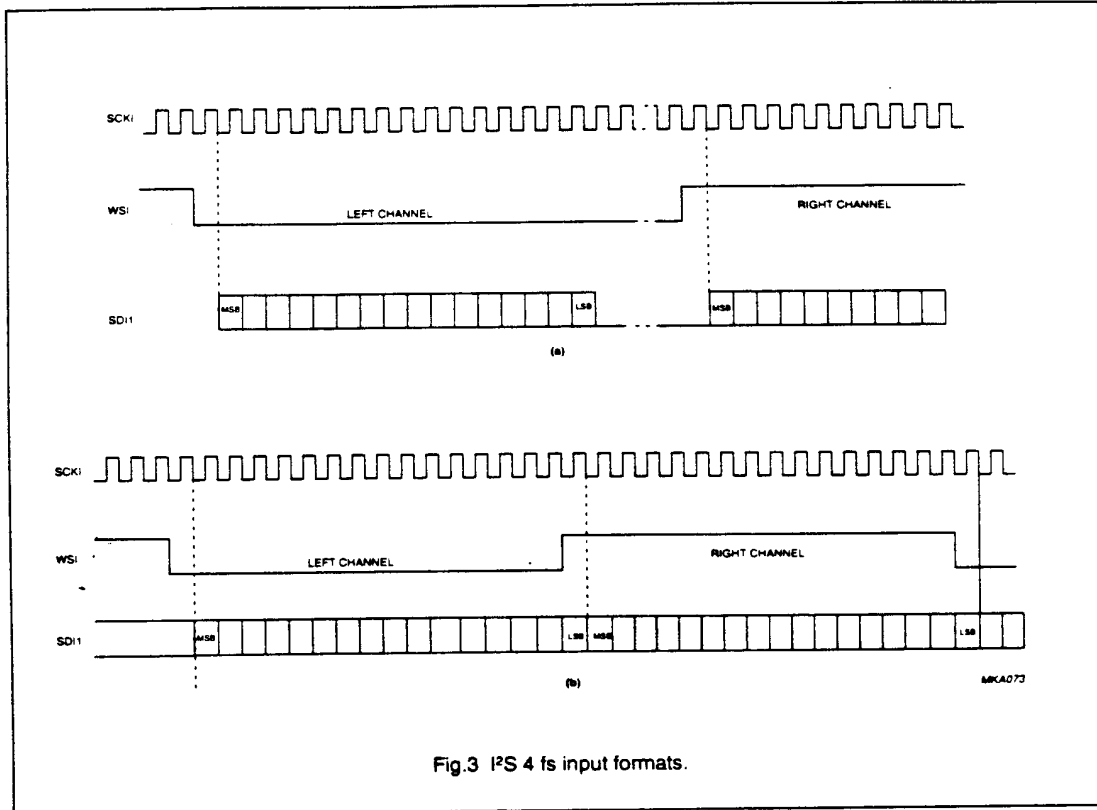


Fig.3 I<sup>2</sup>S 4 fs input formats.

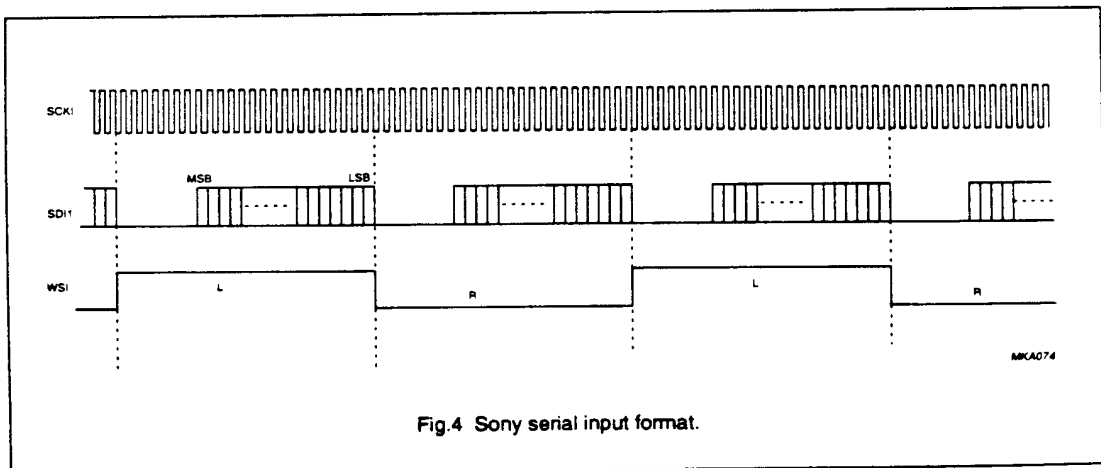


Fig.4 Sony serial input format.

20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

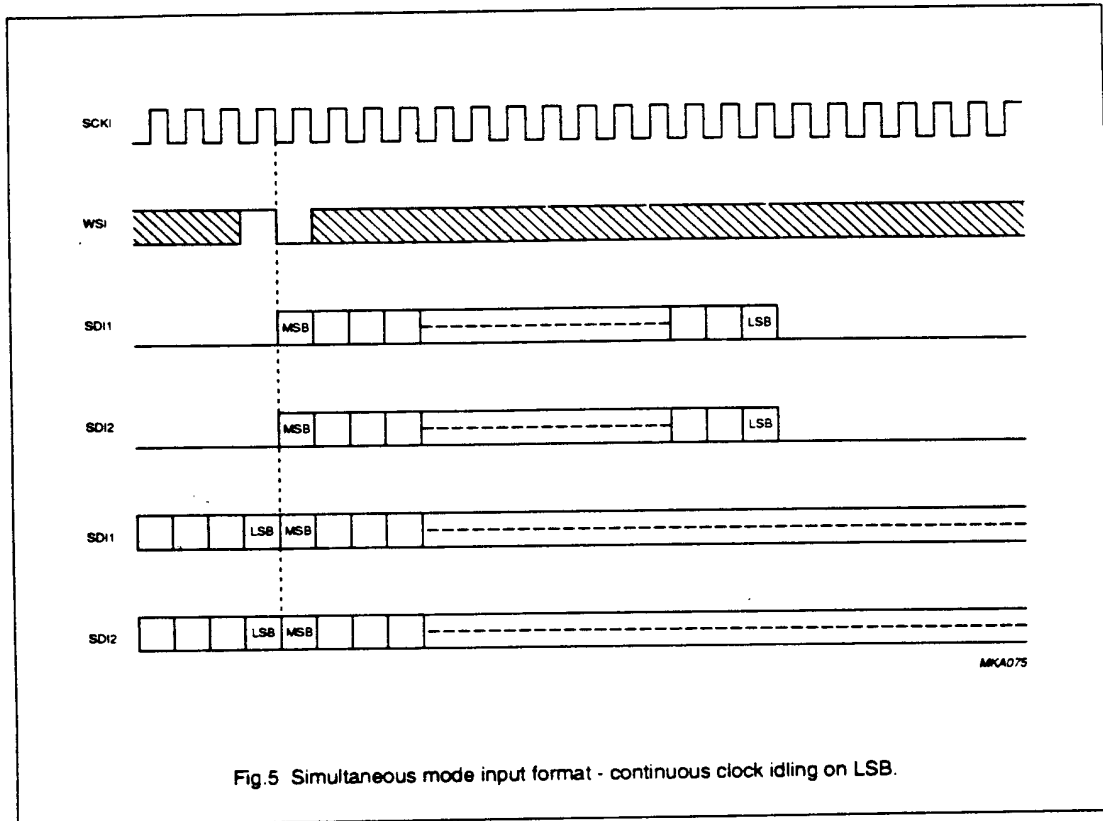


Fig.5 Simultaneous mode input format - continuous clock idling on LSB.

20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

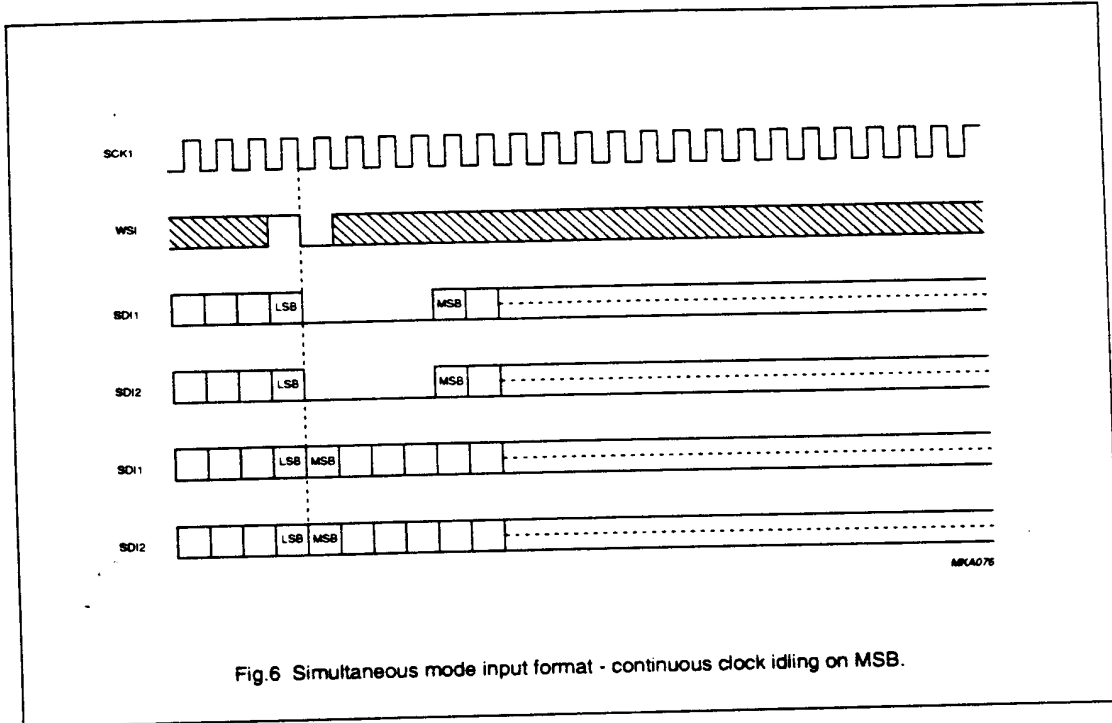


Fig.6 Simultaneous mode input format - continuous clock idling on MSB.

20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

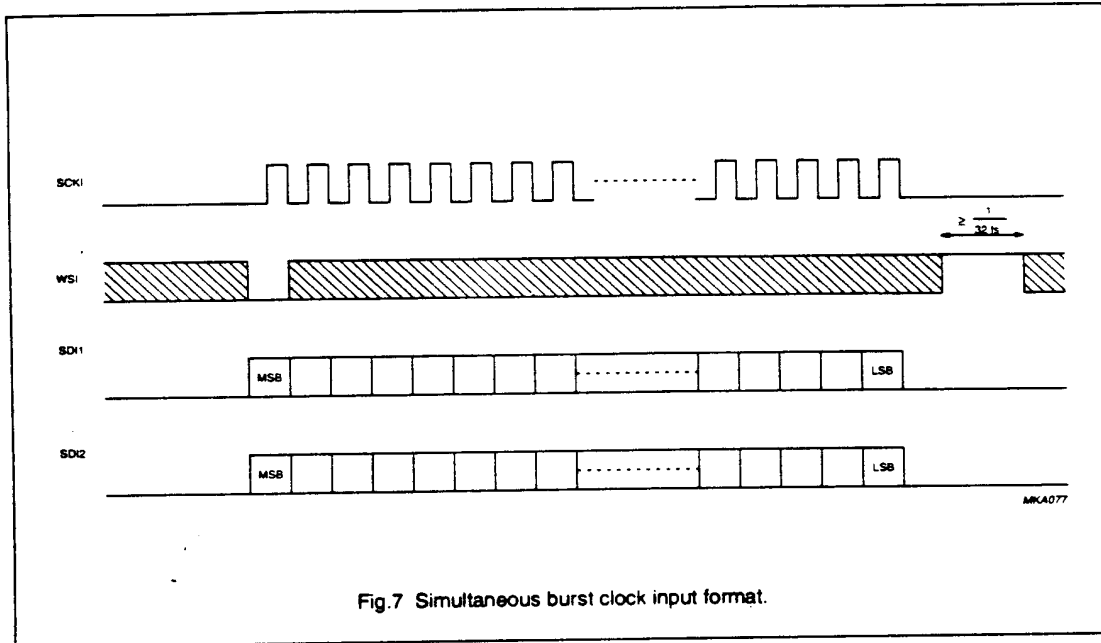


Fig.7 Simultaneous burst clock input format.

20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

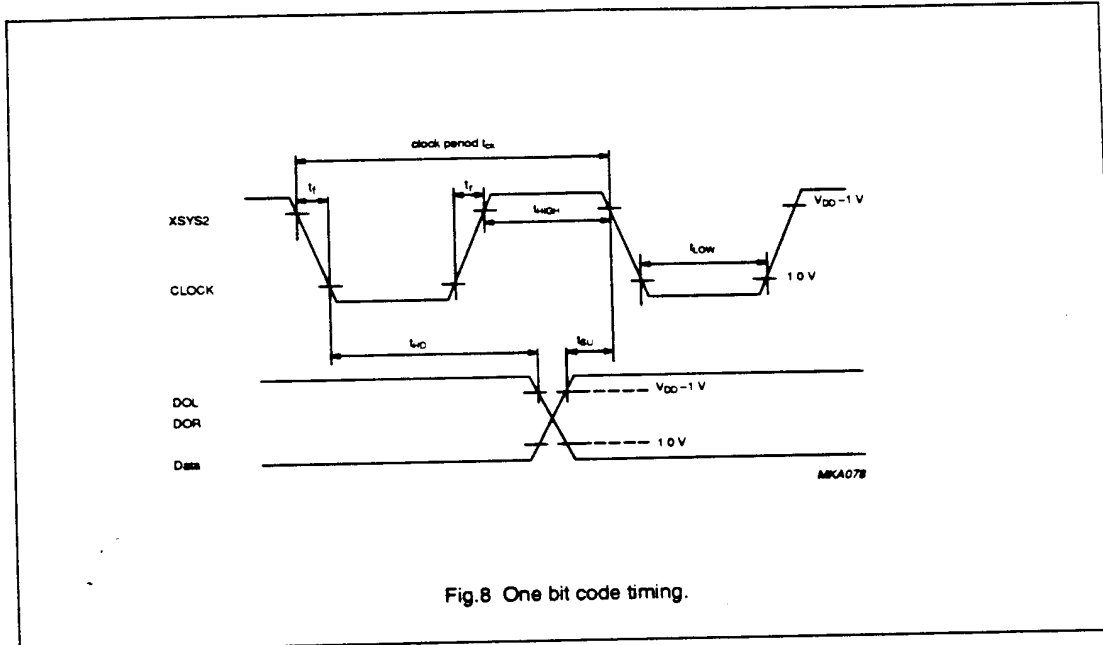


Fig.8 One bit code timing.

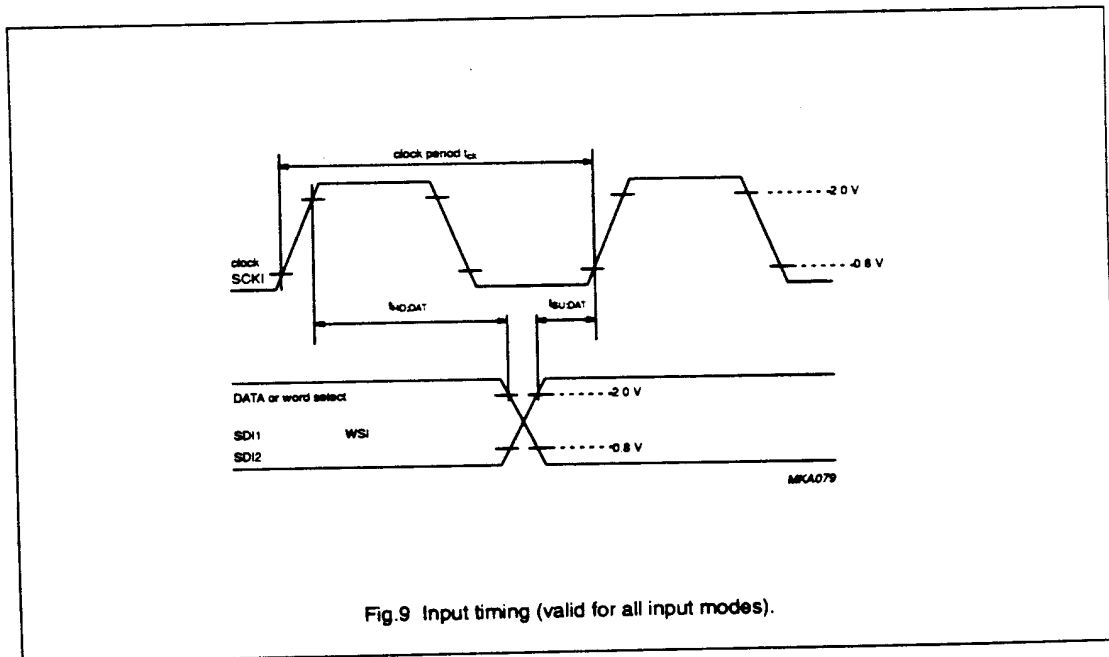
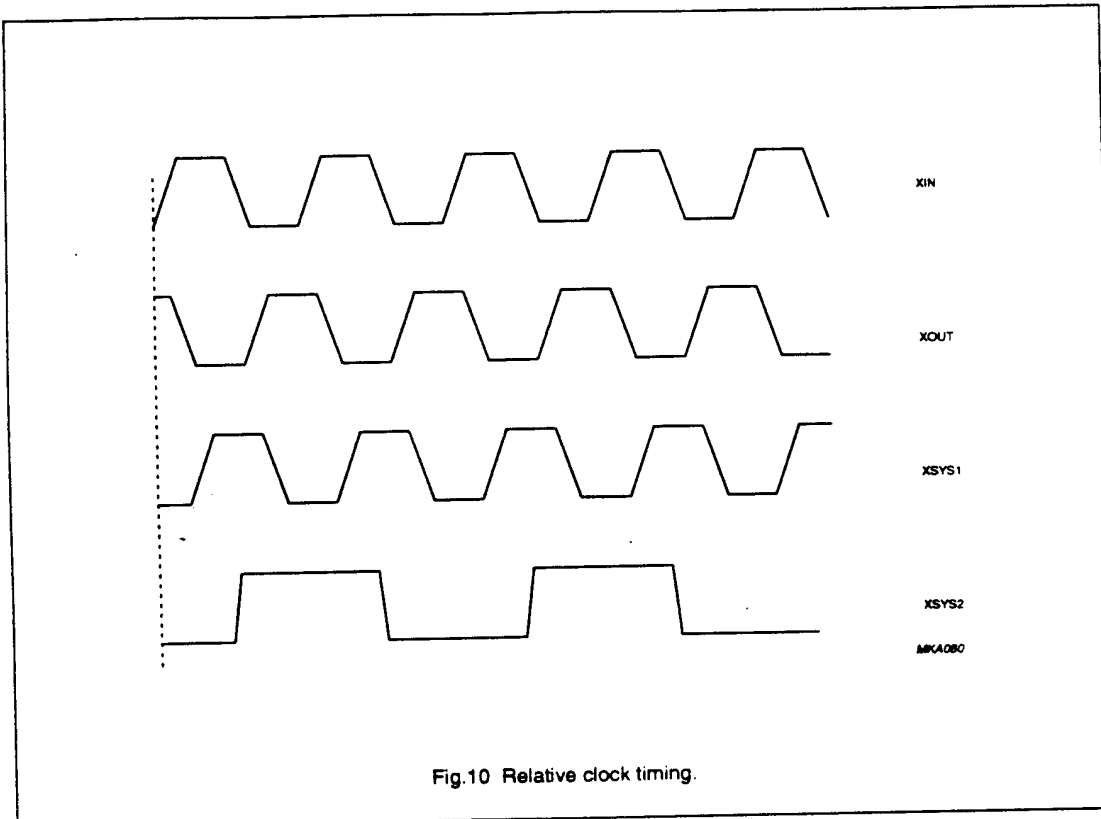


Fig.9 Input timing (valid for all input modes).

20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350





20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

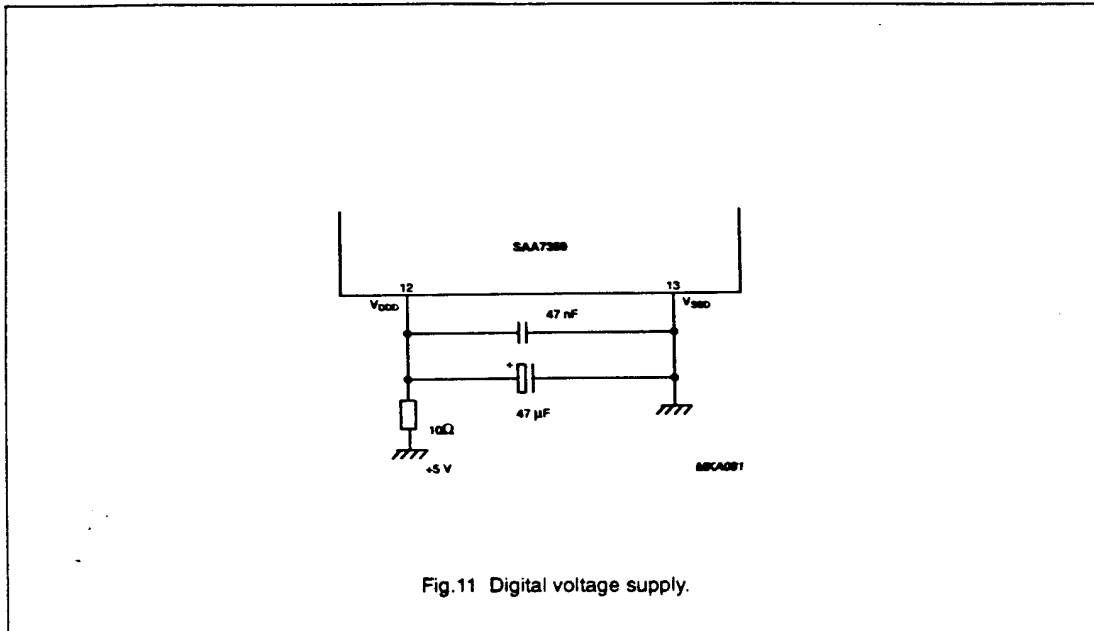


Fig.11 Digital voltage supply.

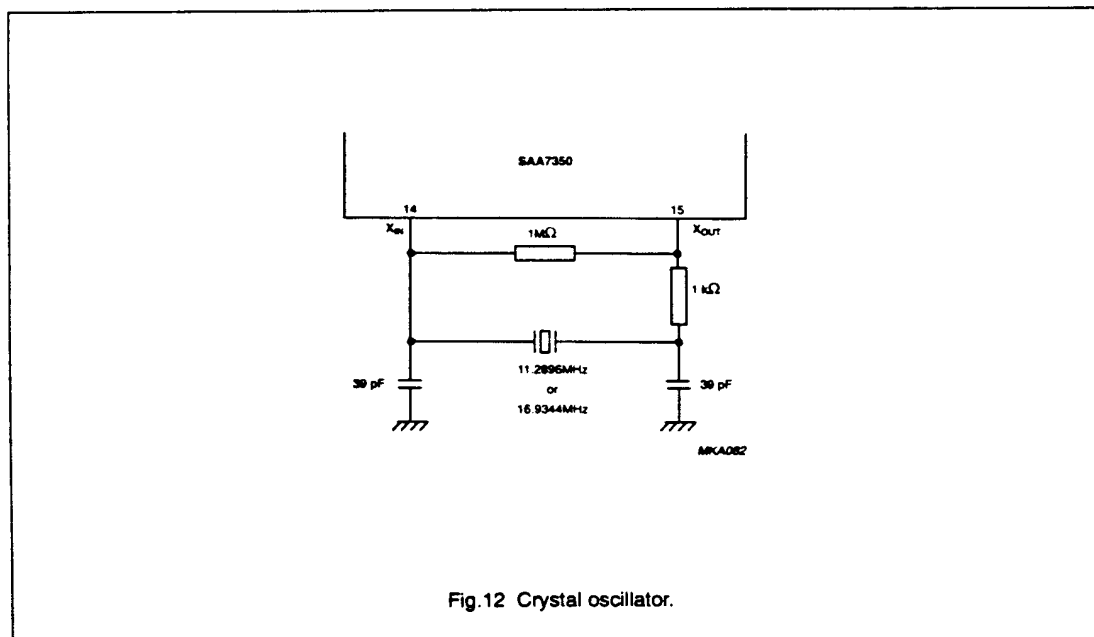


Fig.12 Crystal oscillator.



20-bit input bitstream conversion  
DAC for digital audio systems

SAA7350

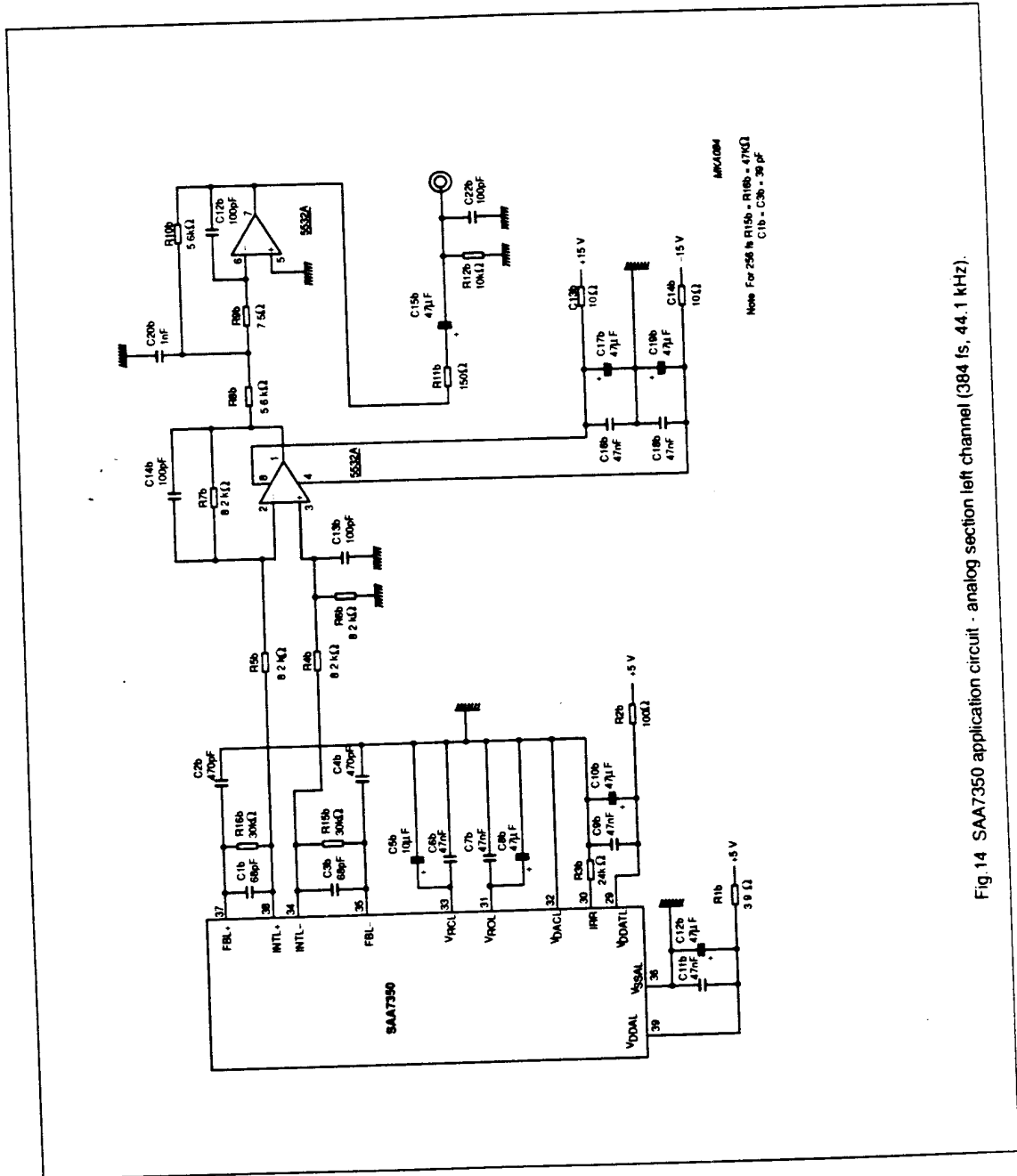


Fig. 14 SAA7350 application circuit - analog section left channel (384 fs, 44.1 kHz).