Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA9820

Multistandard / dual channel TV FM intercarrier sound demodulator

FEATURES

- Multistandard application for sound standards M, B/G, I, D/K
- Two alignment-free PLL FM demodulators
- Four-input source selector for one of the two FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components

GENERAL DESCRIPTION

The TDA9820 is a monolithic, integrated, multistandard TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase-Locked Loop (PLL) reference frequency generation. The circuit has a minimum number of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	peak output current (pin 8 and pin 7)		–	–	± 1.5	mA
P_{tot}	power consumption	V_P = 5 V	–	–	150	mW
(S+N)/N	signal-to-noise ratio (pin 8 and pin 7)	CCIR 468-3	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection (pin 7 and pin 8)	V_{RR} < 200 mV f = 70 Hz	–	20	–	dB
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9820	16	DIL	plastic	SOT38

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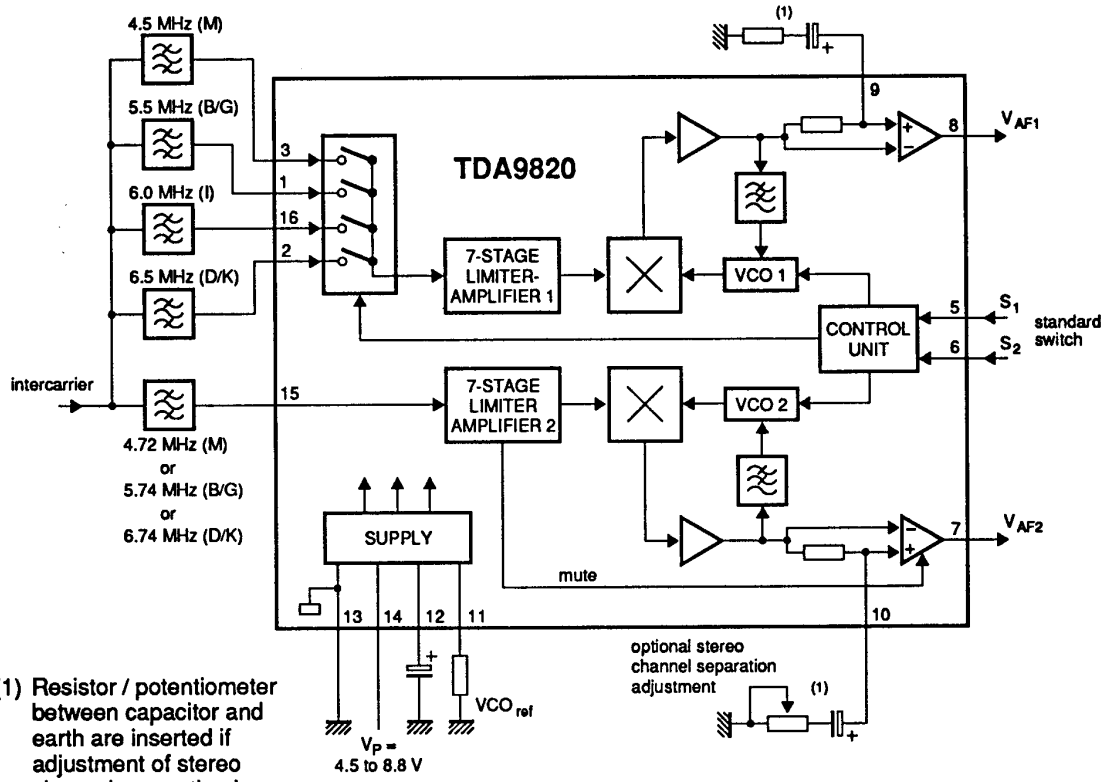

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	first intercarrier input at 5.5 MHz
$IN_{1(D/K)}$	2	first intercarrier input at 6.5 MHz
$IN_{1(M)}$	3	first intercarrier input at 4.5 MHz
n.c.	4	not connected
S_1	5	standard switch bit 1
S_2	6	standard switch bit 2
V_{AF2}	7	second audio output voltage
V_{AF1}	8	first audio output voltage
C_1	9	decoupling capacitor
C_2	10	decoupling capacitor
VCO_{REF}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
IN_2	15	second intercarrier input
$IN_{1(I)}$	16	first intercarrier input at 6.0 MHz

PIN CONFIGURATION

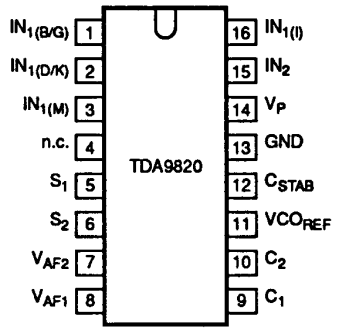

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels , each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is as follows (see Fig.1):

Source selector

The intercarrier signal is fed through external ceramic bandpass filters which are tuned to the sound carrier frequencies.
One of the four filtered sound carriers from pins 1, 2, 3 or 16 is fed to limiter-amplifier 1 via the appropriate electronic switch in the source selector. The electronic switch of the sound carrier is selected by the control unit (see Logic Table).
The second sound carrier of the intercarrier signal is directly fed from pin 15 to limiter-amplifier 2.

FM demodulators

Each limiter amplifier is AC-coupled into an FM demodulator. The FM demodulator PLLs ensures that the demodulators are alignment-free. The FM demodulator outputs are amplified to 500 mV_{rms}. High amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC de-coupling at pin 9 and pin 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as followes:
a) V_{AF1} by a resistor in series with the DC de-coupling capacitor at pin 9
b) V_{AF2} by a variable resistor in series with the DC de-coupling capacitor on pin 10 to the same voltage as V_{AF1} .

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV_{rms}. This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV_{rms} mute is switched off.

Control unit

The control unit selects the required sound standard according to the voltages on pin 5 and pin 6. The control unit performs the following:
(a) selects the free-running frequencies of VCO1 and VCO2
(b) switches the source selector (the four possible combinations are shown in the Logic Table).

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Logic Table

Standard	S1 (pin 5)	S2 (pin 6)	frequency VCO1	frequency VCO2	source selector connection
B/G	1	1	5.5 MHz	5.74 MHz	pin 1
M	1	0	4.5 MHz	4.72 MHz	pin 3
I	0	1	6.0 MHz	off	pin 16
D/K	0	0	6.5 MHz	6.74 MHz	pin 2

Note to Logic Table

In columns S1 and S2:
0 stands for LOW and
1 stands for HIGH.

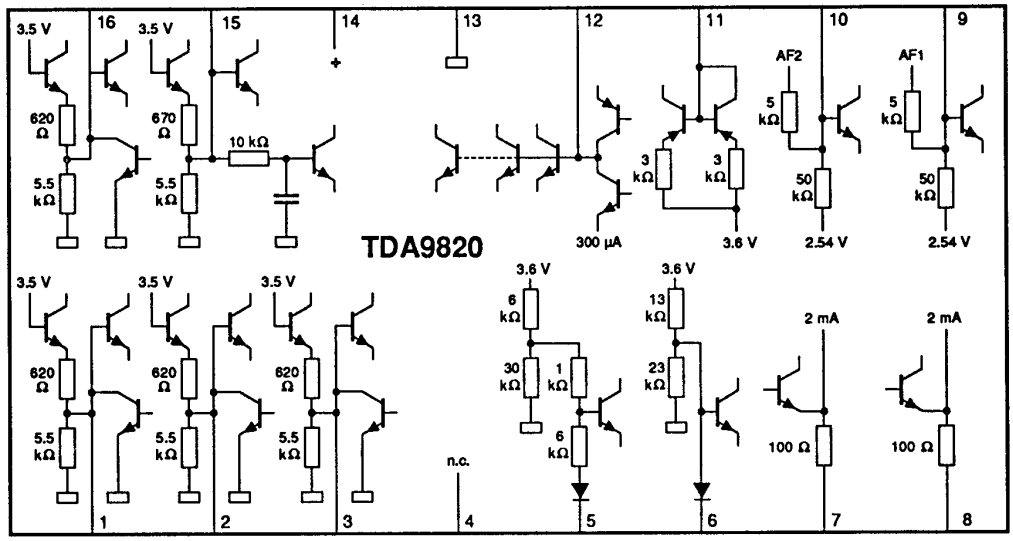


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 14)	–	8.8	V
V_i	input signal (pins 1, 2, 3, 15 and 16)	–0.5	5.0	V
V_{adj}	adjusting voltage (pin 9 and pin 10)	–0.5	V_P + 0.5	V
T_{stg}	storage temperature range	–25	+ 125	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	150	mW

CHARACTERISTICS

All voltages are measured to GND (pin 13); V_P = 5.0 V; Δf_i = ± 50 kHz; f_{mod} = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
Source selector and limiter-amplifier 1 (pins 1, 2, 3 and 16)						
V_i	DC input voltage	input activated	–	2.55	–	V
		input not activated	–	–	0.1	V
R_i	input resistance	input activated	480	600	720	Ω
		input not activated	–	–	100	Ω
$V_{i(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB	–	100	250	μV
	allowed input signal (RMS value)		200	–	–	mV
α_i	crosstalk attenuation	not activated input to activated input	–	50	–	dB
Limiter-amplifier 2						
V_{15}	DC input voltage		–	2.55	–	V
$V_{15(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB (note 1)	–	150	250	μV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
R_{15}	input resistance		480	600	720	Ω
	hysteresis of level detector		–	12	–	dB
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequencies	R11 = 27 kΩ see Logic Table	– – – –	4.5 5.5 6.0 6.5	– – – –	MHz MHz MHz MHz
f_{VCO2}	free-running frequencies	R11 = 27 kΩ see Logic Table	– – –	4.72 5.74 6.74	– – –	MHz MHz MHz
$\Delta f_{VCO1/2}$	free-running frequency spread		–	–	± 10	%
	drift of free-running frequencies	0 to 70 °C	–	500	–	kHz
	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
	adjustment range of free-running frequencies	resistance at pin 11	± 1	–	–	MHz
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	22	29	kΩ
S	steepness of free-running frequency adjustment	resistance at pin 11	–	–200	–	kHz/kΩ
Δf1	catching range of PLLs		± 1.4	± 1.9	–	MHz
Δf2	holding range of PLLs		± 2.0	± 3.0	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output amplifiers AF1 (pin 8) and AF2 (pin 7)						
V_o	DC output voltage (pin 8 and pin7)		–	2.15	–	V
$V_{o(rms)}$	output signal (pin 8 and pin7) (RMS value)		–	0.5	–	V
		clipping level	1.2	–	–	V
I_M	AC output peak current (pin 8 and pin7)		–	–	± 1.5	mA
I_o	DC output current (pin 8 and pin7)		–	–	–2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	0 to 70 °C	–	0.7	–	dB
$\Delta V_o/\Delta V_o$	relative drift of AF output signals	0 to 70 °C	–	0.2	–	dB
$V_{AF(1-2)}$	difference between output signals (pin 8 and pin7)	with 50 µs de-emphasis	–	± 0.3	± 1.0	dB
R_o	output resistance (pin 8 and pin7)		–	100	–	Ω
R_s	series resistor for optional crosstalk adjustment (pin 9 and pin 10)	$V_{AF(1-2)}$ = ± 1.5 dB	–	1.1	–	kΩ
THD	distortion (pin 8 and pin7)	with 50 µs de-emphasis	–	0.1	0.3	%
α_{AM}	AM suppression of AF1/2 (pin 8 and pin7)	with 50 µs de-emphasis; m = 0.3; Δfi = ± 50 kHz; f_{AM} = 1 kHz	46	66	–	dB
(S+N)/N	signal-to-noise ratio (pin 8 and pin7)	with 50 µs de-emphasis; CCIR 468-3	64	68	–	dB
AF_{resp}	AF frequency response (pin 8 and pin 7)	$\Delta V_{AF1/2}$ = –3 dB	0.02	–	200	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value) (pins 8, 7)		–	50	–	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
Control unit (see Logic Table)						
$V_{5,6}$	voltage for 'low'		0	–	0.8	V
$I_{5,6}$	input current	$0 < V_{5,6} < 0.8$	–	–180	–250	µA
$R_{5,6}$	allowed resistance to ground	$0 < V_{5,6} < 0.8$ ('low')	–	–	3.0	kΩ
V_5	voltage for HIGH (note 2)		2.2	–	V_P	V
V_6	voltage for HIGH (note 2)		1.8	–	V_P	V
$I_{5,6}$	input current	$V_{5,6} = V_P$	–	–	10	µA

Notes to the characteristics

1. The input signal at pin 15 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. Under this condition the input impedance is 490 Ω.
2. An open pin (n.c.) is interpreted as HIGH.

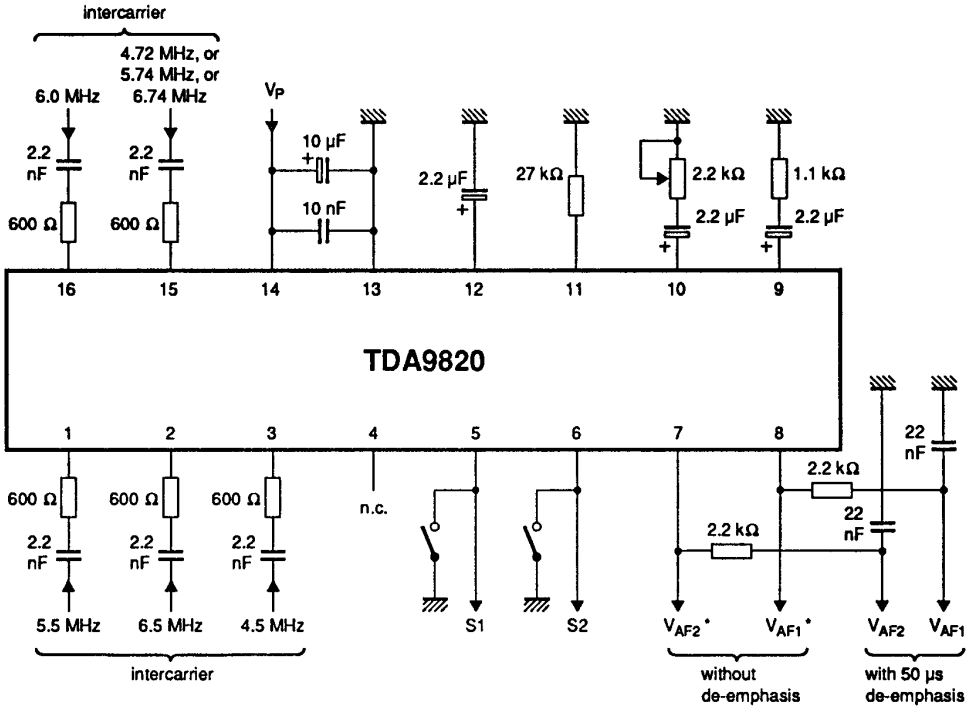


Fig.4 Test circuit.

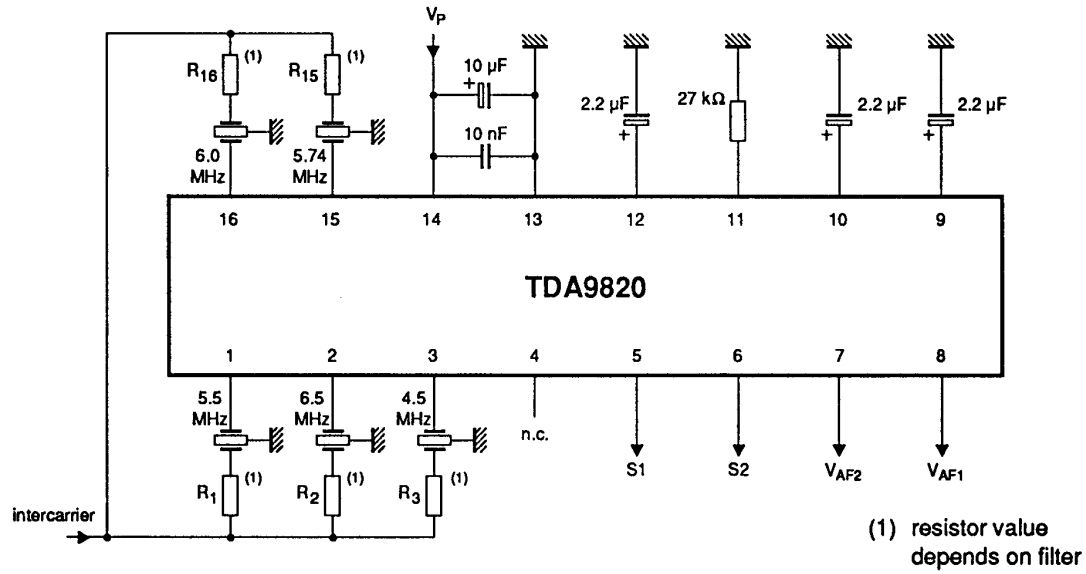
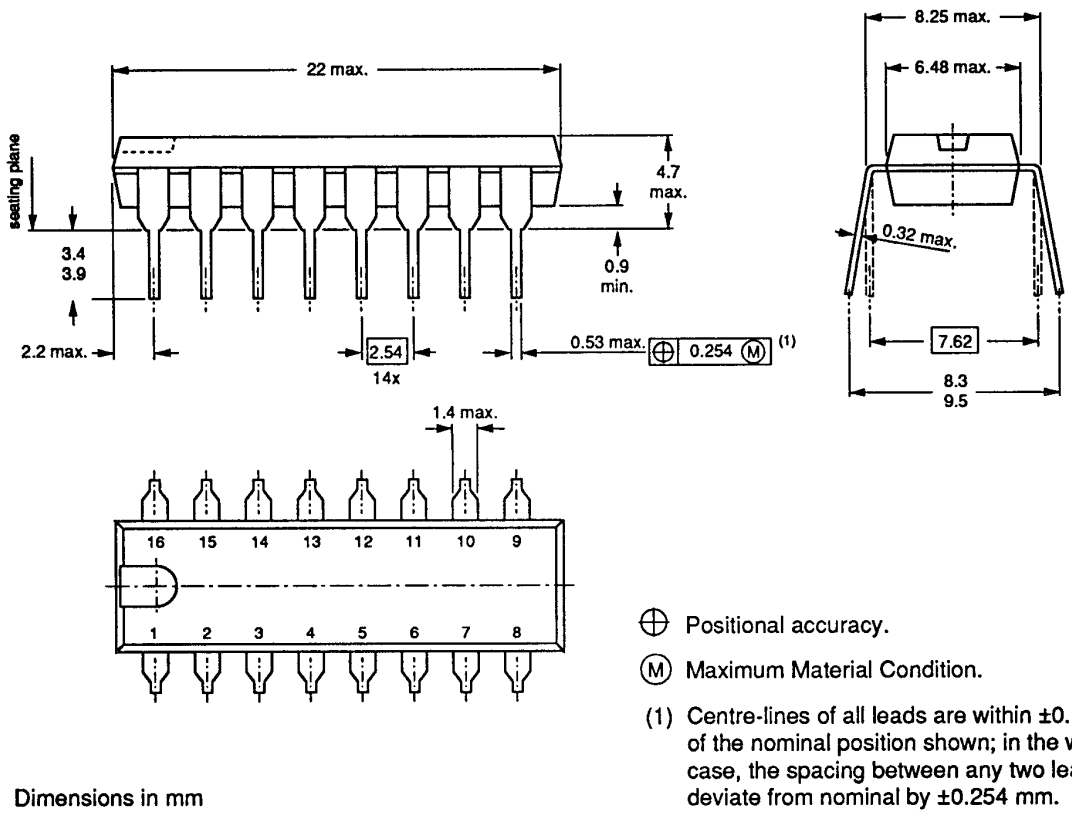


Fig.5 Application circuit.

PACKAGE OUTLINE



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

Dimensions in mm

Fig.5 16-lead DIL-package; plastic (SOT38).

SOLDERING

Plastic dual in-line packages

BY HAND

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering, to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

The same precautions and limits apply as described in 'soldering by hand'.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	

Printed in The Netherlands 9397 288 60011