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DATA RATE ADAPTER

GENERAL DESCRIPTION

The PCB2320 is a CMOS integrated circuit for ISDN applications which has been developed to adapt synchronous and asynchronous user data rates on the CCITT-R interface to a 64 kbit/s Terminal Highway channel (THW).

Features

- Synchronous data rate adaption to 64 kbit/s according to both CCITT X.30 and V.110 specification
- Synchronous data rates supported from 600 to 64000 bits/s
- Asynchronous data rates supported using multisampling method up to 19200 bit/s with additional transition coding based on CCITT recommendation R.111. These rates are of use for 50, 75, 110, 134.5, 150, 200, 3600, 7200, 12000, 14400 and 19200 bits/s
- Automatic speed recognition in receiver with the aid of a microcontroller (for synchronous speeds up to 19200 bits/s)
- 2 Mbit highway interface (long synchronization)
- Serial interface for the DTE
- Microcontroller interface with multiplexed address/data bus
- Interchange circuits mapped into X and S bits
- Forcing and looping of interchange circuits
- Setting of test loops
- DRA monitoring possibilities for in or out of synchronization indication, activity check and readout of the logic states in the interchange circuits
- Single 5 V power supply
- TTL compatible input levels

9397 290 60011

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117)

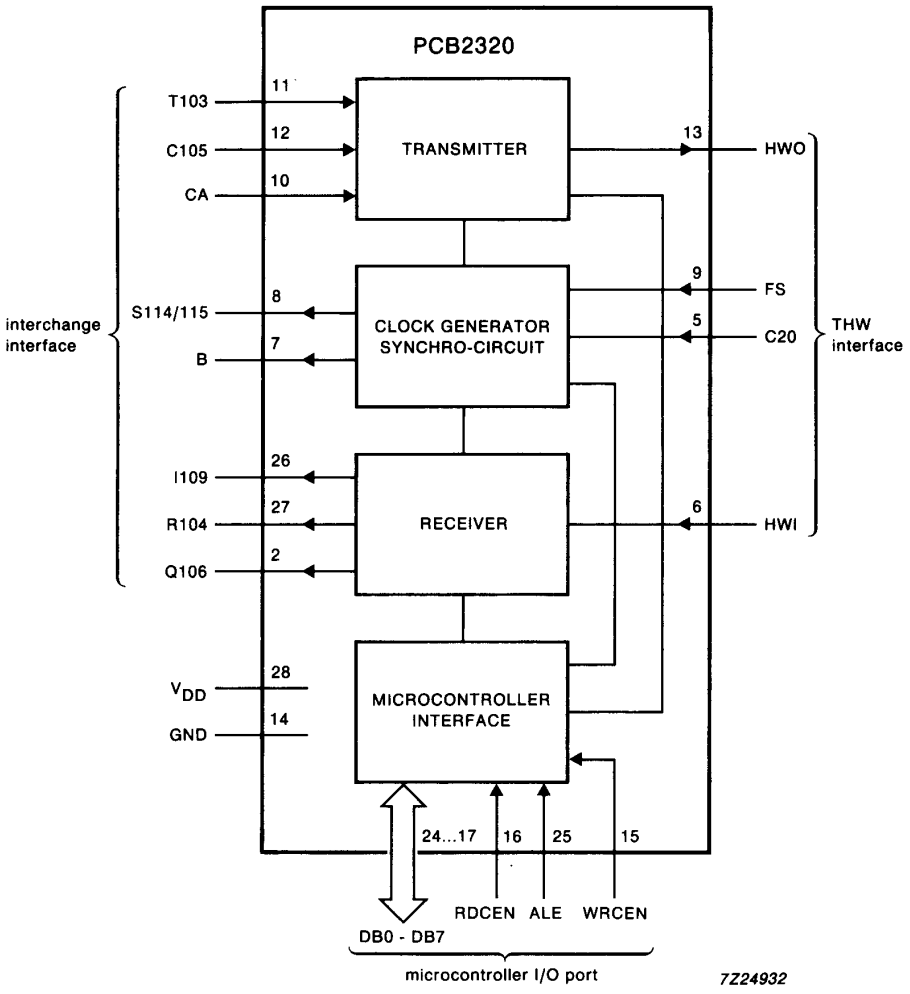

Fig.1 Block diagram.

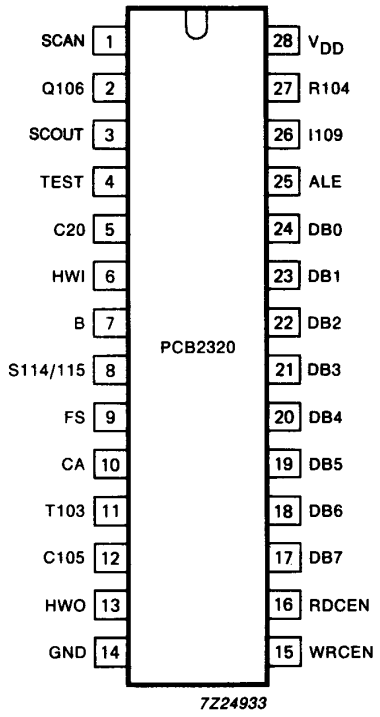

Fig.2 Pinning diagram.

DEVELOPMENT DATA

PIN	SYMBOL	DESCRIPTION
1	SCAN	Scantest-mode select. For normal use of the DRA, SCAN should be connected to ground.
2	Q106	Q106 performs as a circuit 106, a CCITT V-series defined interchange circuit. The μC is able to control this circuit (see section 2.4).
3	SCOUT	Scanline output. This output is only used in the scantest mode. For normal use this pin should not be connected.
4	TEST	Test-mode setting. For normal use TEST should be always connected to ground.
5	C20	Clock input (2.048 MHz). C20 is the clock input for the device.
6	HWI	Highway input. Input for the 2 Mbit/s highway time slot (8-bits) timed by C20 (pin 5) and controlled by FS (pin 9).
7	B	Byte timing output (X series). Signal B is a CCITT-X series defined control signal. This circuit provides the byte timing signal for the DTE. The output at pin 7 indicates the last bit of a data byte, it is HIGH during one period of S114/115 (pin 8) and LOW during the byte period. Output B can be controlled by the microcontroller.
8	S114/115	Signal element timing output. S114/115 (circuit 114/115 for V, S for X series) provides signal element timing. In synchronous mode S114/115 generates the data clock for circuit T103 and R104. In asynchronous mode S114/115 generates 48 kHz which is half of the sampling clock frequency of the asynchronous coder. S114/115 can be controlled by the microcontroller.

PIN	SYMBOL	DESCRIPTION
9	FS	Frame select input. Highway frame alignment signal. Every 125 μs FS aligns the 8 highway bits for the DRA on the highway input (pin 6) and highway output (pin 13).
10	CA	Second control input. CA is a signalling channel to the remote subscribers circuit IA. It is sampled every 40 bit frame and transmitted in the X-bit. Output IA can be read by the microcontroller or coupled to Q106. CA can be controlled by the microcontroller.
11	T103	Transmit input. T103 has to be connected to the transmit output (T for X, circuit 103 for V series) of the DTE equipment. For synchronous speeds T103 will be sampled by the DRA on every leading edge of S114/115. T103 can be controlled by the microcontroller.
12	C105	C105 is a signalling channel which corresponds to I109 of the remote subscriber. For the V series, C105 performs as circuit 105 and for the X series as circuit C. C105 is sampled on the trailing edge of the byte-time output pulse. C105 is sampled three times per 40-bit frame and six times per 80-bit multiframe and then placed in the S-bits. C105 can be controlled by the microcontroller.
13	HWO	Highway output. This is the output for the 2 Mbit/s time slot which are produced by the DRA during control of the frame select input. The HWO will be 3-state when FS is LOW. The HWO can be controlled by the microcontroller.
14	GND	System ground.
15	WRCEN	Write chip enable (active LOW). The microcontroller writes data to the DRA when WRCEN is LOW.
16	RDCEN	Read chip enable (active LOW). Data is transferred to the bus by the DRA after the negative edge of RDCEN.
17	DB7	Data/address bus
18	DB6	
19	DB5	
20	DB4	
21	DB3	
22	DB2	
23	DB1	
24	DB0	
25	ALE	Address latch enable input. When ALE is HIGH the data/address bus contains an address.
26	I109	Data channel received line signal detector/indication. Output which indicates the state of the remote subscribers C105 circuit. I109 is inverted on the trailing edge of S114/115. I109 can be made byte-timing synchronous by the microcontroller.
27	R104	R104 provides circuit 104 for the V series and R for the X series of interfaces. Circuit R104 will be shifted out on every trailing edge of S114/115. R104 can be made byte-timing synchronous by the microcontroller.
28	V_{DD}	Power supply +5 V.

FUNCTIONAL DESCRIPTION

The DRA adapts synchronous user data rates on the 'R' interface in accordance with the CCITT X.30/V.110 and ECMA 102 specification (September 1984) to a 64-kbit/s THW channel (ISDN B-channel) and vice-versa. Asynchronous data on the 'R' interface, up to 19200-bits/s, is supported using the multisampling method with additional transition coding based on the CCITT R.111 recommendation.
The translation between user data rates and the 64-kbit/s data rate is performed in the transmitter and receiver part as illustrated in Fig.1. The block diagram illustrates three interfaces;

The interchange interface — A set of 'V' type interchange circuits, 103 to106, 109, 114 and 115 or 'X' type data interface interchange circuits, T, R, C, I, S and B can be connected to the DRA via level converters.

The terminal highway — The THW is a PCM highway with a transmission rate of 2.048 Mbits/s which consists of 32 x 64 kbits/s channels. The interface consists of two unidirectional data lines (HWI and HWO), a THW clock line (C20) and a THW alignment signal line (FS). The internal timing for the DRA is derived from the THW clock and the THW alignment signal from the clock generator and synchronization circuit respectively), i.e. no crystal or external oscillator is required.

The 8-bit microcontroller — The microcontroller I/O port is PCB80C51 compatible microcontroller interface. The data and address lines are multiplexed. The I/O port provides the interface for the control stages of the DRA. The microcontroller is used to load the DRA with information about speed, test loops, SET or RESET of interchange circuits while information from the DRA about speed setting of the remote subscriber, state of the interchange circuits and synchronization on the THW can be read out.

DEVELOPMENT DATA

Modes of operation

For synchronous data rates of 600, 1200, 2400, 4800, 9600, 19200 and 38400-bits/s an X.30/V.110 defined multiframe of 80-bits is used (see Table A1) which consists of 2 x 40-bit frames using subrates of 8, 16 and 32 kbits/s. An incoming data rate is transposed to the next highest data rate (the intermediate rate) which is expressed by $2^{\wedge}$ x 8 kbits/s (where $^{\wedge}$ = 0, 1, 2 or 3, see Table 1).

Table 1 First step in data rate adaption

data rate (bit/s)	frame speed (Hz)
600, 1200, 2400, 4800	8000
9600	16000
19200	32000
38400	64000

The data rate conversion is completed after being multiplied to 64 kbits/s. The multiframe consists of 10 bytes which in turn contains 8 x 6 data bits, 8 x 'S' bits (used for a line signalling channel), 7 bits to indicate the selected speed and 17 bits for frame synchronization. For a data rate of 48000 bits/s a 32-bit frame is used (see Table A2). The frame consists of 4 bytes which in turn contain 4 x 6 data bits, 3 x 'S' bits, 1 x 'X' bit and 4 frame synchronization bits. For a data rate of 56000 bits/s a 32-bit frame is used (see Table A3). The frame consists of 4 x 7 data bits and 4-bits for a line signalling channel. For a data rate of 64000 bits/s no data rate adaption is required. The DRA is transparent at this date rate (see Table A4).
For asynchronous data between 0 and 19200 bits/s a transparent transmission method is used. The data is sampled at 96 kHz and placed in a 48 kbit/s bit-stream. A 32-bit frame is used which consists of 4 x 6 bits for coded data, 3 x 'S' bits, 1 x 'X' bit and 4 frame synchronization bits.

FUNCTIONAL DESCRIPTION (continued)

A coding/sampling method is used which is based on the technique of multiple sampling with additional transition coding, as recommended in CCITT R.111 (see Fig.A1). This method does not recognise character length or start/stop bits but samples the incoming data at 96 kHz and codes the transition in two bits. The resultant 48-kbits/s data stream is inserted in the 32-bit frame in accordance with X.30/V.110. In the 48-kbits/s data stream there are always at least 2 bits per 19.2 kbits/s signal element. One 'T' bit (transition) is used to indicate the polarity after a transition and a second bit 'C' (coding) is used to define in which half, A or B, of the 48 kHz clock period the transition has occured.
Because one bit can discriminate two phases, the sampling frequency must be 96 kHz.
In the lower data rates more than two 48-kbit data bits will fall between two signal element transitions. In this situation the resultant 48-kbit data bits 'P' (polarity) will repeat the polarity and are, therefore, equal to the previous transition bit 'T'.
The phase shift varies for the different bit rates from 20% for 19200 bits/s up to 2.5% for 2400 bits/s (lower for slow data).

Interchange interface

The interchange interface connects the DRA, via level converters, to the DATA Terminal Equipment (DTE) (see Fig.3).
The relationship between the signals on the interchange circuits and the signals at the DRA are given in Table 2. The interchange interface consists of the following circuits:

T103	circuit 103 (V series), transmitted data; T (X series), transmit
R104	circuit 104 (V series), received data; R (X series), receive
C105	circuit 105 (V series), request to send; C (X series), control
Q106	circuit 106 (V series), ready for sending
I109	circuit 109 (V series), data channel received line signal detector; I (X series), indication
S114/115	circuit 114 (V series), transmitter signal element timing circuit 115 (V series), receiver signal element timing; S (X series), signal element timing
B	B (X series), byte timing
CA	second control input

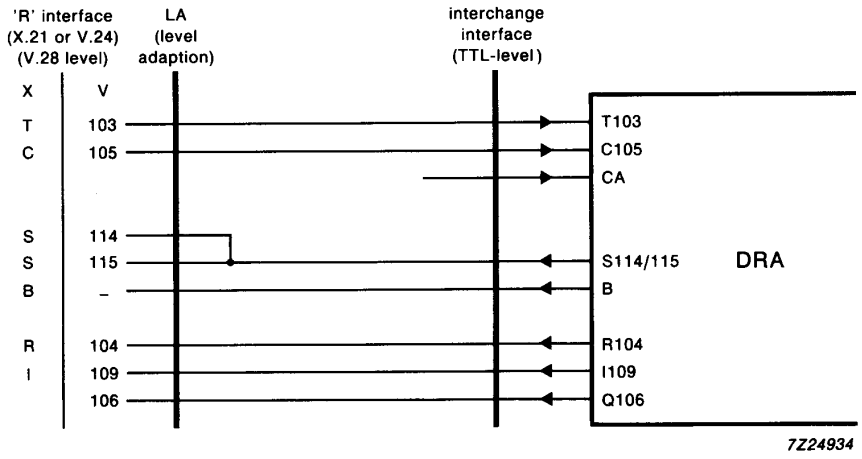

Fig.3 Interchange interface.

Table 2 Relationship between the signals on the interchange circuits and the signals on the DRA.

interchange circuit	state of the int. circuit	pin name of DRA	state on pin of DRA
103 or T 104 or R	0/1 0/1	T103 R104	0/1 0/1
114/115 or S B 105 or C 106 109 or I	ON/OFF ON/OFF ON/OFF ON/OFF ON/OFF	S114/115 B C105 Q106 I109	0/1 0/1 0/1 0/1 0/1
	OFF, 1 : $V \leqslant -3$ V ON, 0 : $V \geqslant 3$ V		0: V = 0 V 1: V = 5 V

Note to Table 2

On the highway frame ON = 1 and OFF = 0 in accordance with ECMA 102 (September 1984). This is contrary to ECMA 102 (December 1984 where ON = 0 and OFF = 1).

The frequency of the element timing signal (S114/115 pin 8) is dependent on the data rate setting of the DRA. This can be initiated by bits V1 to V4 in register W1. The relationship between the frequency of S114/115 and the data rate of the DRA is given in Table 5.

The 'B' signal (pin 7) provides the DTE with the byte timing signal. The signal will be HIGH during one period of S114/115 and indicates the last bit of a data byte (LOW during the byte period). The DTE must initiate the first bit of the byte on circuit T103 at the HIGH-to-LOW transition of S114/115 which follows the HIGH-to-LOW transition of signal 'B'.
For synchronous speeds T103 (pin 11) is sampled at every leading edge of S114/115 whilst signal changes on R104 (pin 27) occur on every trailing edge (see Fig.4).

DEVELOPMENT DATA

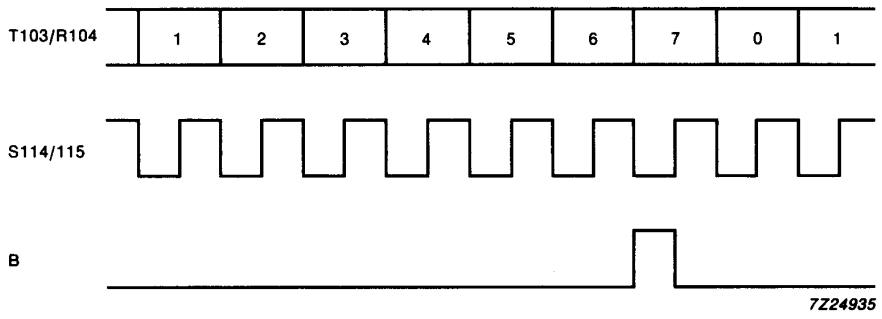

Fig.4 Timing on the interchange interface.

FUNCTIONAL DESCRIPTION (continued)

C105 (pin 12) is sampled on every trailing edge of signal 'B'. It is sampled three times per 40-bit frame and placed in the 'S'-bits of the frame. I109 (pin 26) indicates the state of the remote subscriber circuit C105 and is inverted on the trailing edge of S114/115. I109 can be made byte-timing synchronous under control from the microcontroller.
I109 is delayed to enable an inversion at the first HIGH-to-LOW transition of S114/115 subsequent to the HIGH to LOW transition of circuit 'B' or vice versa. At the same time the 8th data bit is clocked out from R104. I109 is 1-bit earlier as defined in CCITT X.30.
CA is a signalling channel to the remote subscribers circuit IA. The signal is sampled every 40-bit frame and transmitted in the X-bit. Output IA can be read via the microcontroller or coupled to Q106. Signal changes in Q106 occur as soon as the new X-bit is received which is on the falling edge of S114/115.
The sampling moments of the interchange circuits are illustrated in Appendix B.

Terminal highway interface

The terminal highway (THW) is a 2 Mbits/s four-wire fully duplex PCM highway for 64 kbits/s circuit switched channels.
The THW consists of:

HWI	terminal highway input
HWO	terminal highway output
C20	terminal highway 2048 kHz clock input
FS	terminal highway slot assignment input

The THW incorporates 32 channels. One channel, on the HWO, is used to transmit data from the local subscriber to the remote subscriber DTE and one time slot on the HWI to transmit data in the opposite direction. The remaining slots are 'free'. Both the HWI and the HWO are clocked by C20. The slot in which data is transmitted to the THW is aligned by the FS signal. When FS (pin 9) is HIGH the DRA clocks 8 data bits to the HWO and, during this period, data from the HWI is clocked to the DRA. The highway channel assignment is illustrated in Fig.5.

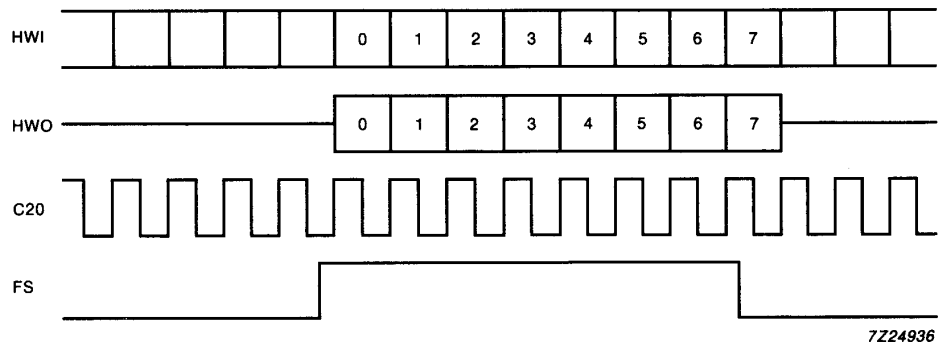

Fig.5 Highway channel assignment.

8-bit microcontroller interface

The DRA is controlled by the 8-bit microcontroller bus which is compatible with the PCB80C51 microcontroller bus. The microcontroller interface consists of:

8 data/address multiplexed I/O lines (pins 17 to 24)
A read chip enable input (RDCEN pin 16)
A write chip enable (WRCEN pin 15)
An address latch enable (ALE pin 25)

When ALE is HIGH data at the I/O port is latched to the address latch. One of the five write or three read registers can be selected (see Table 3). When RDCEN is LOW the DRA writes data from the selected read register to the I/O port.
When WRCEN is LOW data from the I/O port is written to the selected write register.

Table 3 Register addresses

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	address	WT reg	RD
X	X	X	X	X	0	0	0	0	W0	R0
X	X	X	X	X	0	0	1	1	W1	R1
X	X	X	X	X	0	1	0	2	W2	R2
X	X	X	X	X	0	1	1	3	W3	–
X	X	X	X	X	1	0	0	4	W4	–

The WRITE registers perform the following functions;

- data rate setting
- forcing and looping of the interchange circuits
- setting of test loops

The READ registers can be used to monitor the DRA and have the following functions:

- input/output synchronization indication of the DRA
- activity check on the THW and the interchange circuit T103
- readout the logic state of the interchange circuits
- readout of the data rate setting of the remote DRA

Table 4 Bit assignment registers W0 to W4

WRITE reg	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W0	–	E7	E6	E5	E4	E3	E2	E1
W1	L4	L3	L2	L1	V4	V3	V2	V1
W2	I109	I109	C105	C105	R104	R104	T103	T103
	ON	OFF	ON	OFF	1	0	0	1
W3	DE7	IC	CAI	CI	FS2R	–	CA ON	CA OFF
W4	NC	DR	H1	ND	106 ON	B OFF	106 OFF	S OFF

FUNCTIONAL DESCRIPTION (continued)

Register W0

In every 10 bytes multiframe (for data rates not exceeding 38400 bits/s) bits E1 to E7 are available to transmit information about the data rate to the remote subscriber. The information is described in the X.30/V.110 manuals.
For data rates from 600 to 1200 bits/s E7 is only inserted in the frame when DE7 is at logic 1.
If DE7 is at logic 0 a synchronization pattern will be inserted at E7 in accordance with X.30/V.110.
For data rates from 48000 to 68000 bits/s and the asynchronous mode no E-bits are transmitted.

Register W1

The 'V' bits (V1 to V4) are used to initiate the clock sections of the DRA. The relationship between the data rate and the setting of the 'V' bits is given in Table 5. With each 'L' bit (L1 to L4) a test loop can be created. If L1 is set to logic 1 then T103 (pin 11) is connected to R104 (pin 27). If L2 is set to logic 1 then data received from the remote subscriber is retransmitted back to the remote subscriber. If L3 is set to logic 1 the HWO (pin 13) is connected to HWI (pin 6) and when L4 is set to logic 1 HWI is connected to HWO. The four test loops 1 to 4 are illustrated in Figs 6 and 7.

Table 5 Data rate setting of the DRA

data rate (bits/s)	V4	V3	V2	V1	S114/115 (Hz)
600	1	1	0	0	600
1200	0	0	0	0	1200
2400	1	1	0	1	2400
4800	1	1	1	0	4800
9600	1	1	1	1	9600
19200	0	0	0	1	19200
38400	0	0	1	0	38400
48000	0	0	1	1	48000
56000	0	1	0	0	56000
64000	0	1	0	1	64000
async	0	1	1	1	48000

Register W2

With T103 0 and T103 1 it is possible to clamp the input of T103 to logic 0 or logic 1 or have the data input to the DRA at pin 11. The logic settings for T103 are given in Table 6.

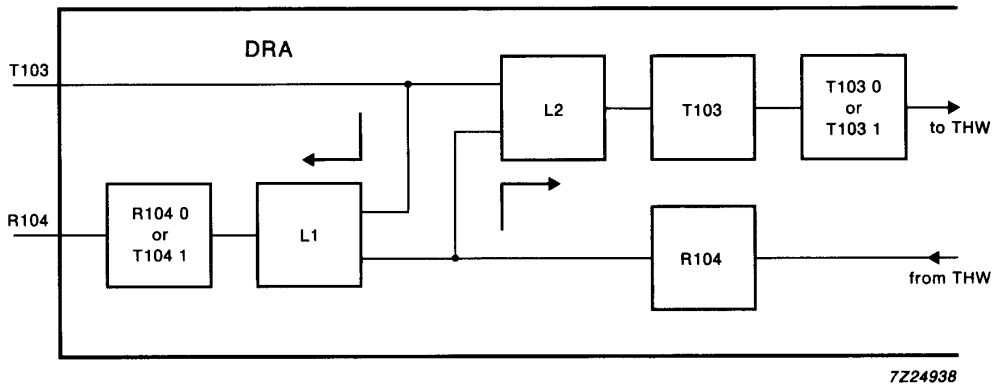

Fig.6 Test loop 1 and 2.

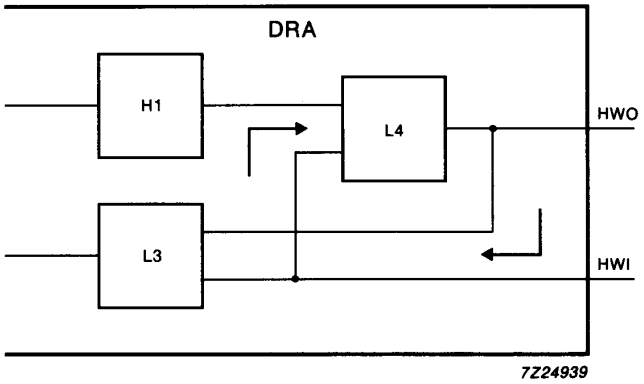

Fig.7 Test loop 3 and 4.

Table 6 Settings for T103 0 and T103 1

T103 1	T103 0	T103
0	0	DRA accepts data at input T103
0	1	input T103 clamped to logic 0
1	0	input T103 clamped to logic 1
1	1	input T103 clamped to logic 1

With R104 0 and R104 1, it is possible to clamp output R104 (pin 27) to logic 0 or logic 1, or, to indicate the received data bits on output R104. The settings for R104 are given in Table 7 (see also Fig.6).

Table 7 Settings for R104 0 and R104 1

R104 0	R104 1	R104
0	0	output R104 indicates the received data bits
0	1	output R104 clamped to logic 1
1	0	output R104 clamped to logic 0
1	1	output R104 clamped to logic 0

FUNCTIONAL DESCRIPTION (continued)

With C105 ON and C105 OFF it is possible to clamp the input C105 (pin 12) to logic 0 or logic 1, or, for the DRA to accept an input on C105. The settings for C105 are given in Table 8 (see also Fig.8).

Table 8 Settings for C105 ON and C105 OFF

C105 ON	C105 OFF	C105
0	0	DRA accepts data at input C105
0	1	input C105 clamped to logic 0
1	0	input C105 clamped to logic 1
1	1	input C105 clamped to logic 1

With I109 ON and I109 OFF it is possible to clamp output I109 (pin 26) to logic 0 or logic 1, or, to indicate the received data bits on output I109. The settings for I109 are given in Table 9 (see also Fig.8).

Table 9 Settings for I109 ON and I109 OFF

I109 OFF	I109 ON	I109
0	0	output I109 indicates the received 'S' bits
0	1	output I109 clamped to logic 0
1	0	output I109 clamped to logic 1
1	1	output I109 clamped to logic 1

Register W3

With CA ON and CA OFF it is possible to clamp the input CA (pin 10) to logic 0 or logic 1, or, for the DRA to accept an input on C105. The settings for CA ON and CA OFF are given in Table 10 (see also Fig.8).

Table 10 Settings for CA ON and CA OFF

CA OFF	CA ON	CA
0	0	DRA accepts data at input CA
0	1	input CA clamped to logic 0
1	0	input CA clamped to logic 1
1	1	input CA clamped to logic 1

The FS2R bit controls the 4-byte synchronization system for data rates greater than 38400 bits/s and asynchronous. When set to logic 1 the incoming highway data is assumed to be byte synchronous and the DRA will only search on the first bit position of every HW octet for synchronization. When set to logic 1 the DRA will search for synchronization on every bit position.

Because this may cause wrong synchronization on the 'S' and 'X' (the 8th bit) instead of the first bit the CCITT recommends that this mode be used only for international purposes and, in this case, make the 'X' bit a continuous logic 1 (by making CA logic 0).

If CI is set to logic 0 then data at input C105 is placed in the 'S' bits to be transferred. If CI is set to logic 1 then the 'S' bits received on the THW are placed in the 'S' bits to be transferred (see Fig.8).

If CAI is set to logic 0 then data at the CA input is placed in the 'X' bits to be transferred. If CAI is set to logic 1 then the 'S' bits received on the THW are placed in the 'X' bits to be transferred (see Fig.8).

If IC is set to logic 0 then the 'S' bits received on the THW are placed at output I109. If IC is set to logic 1 then output I109 is connected to input C105 (see Fig.8).
If DE7 is set to logic 0, for data rates 600 and 1200 bits/s, a synchronization pattern will be inserted at E7 in the frame (the synchronization pattern for a data rate of 600 bits/s is specified in CCITT X.30).
If DE7 is set to logic 1 the synchronization pattern will be disabled and position E7 in the frame will be filled with information from W0. The synchronization pattern is given in Tables 11 and 12.

Table 11 The synchronization pattern at E7 for 1200 bits/s

multiframe 1	00000000	1PPPPPPS 111122	1PPPPPPX 223333	1PPPPPPS 444455	1PPPPPPS 556666
	1EEEEEE1 123456	1PPPPPPS 777788	1PPQQQQX 881111	1QQQQQQS 222233	1QQQQQQS 334444
multiframe 2	00000000	1QQQQQQS 555566	1QQQQQQX 667777	1QQQQRRS 888811	1RRRRRRS 112222
	1EEEEEEO 123456	1RRRRRRS 333344	1RRRRRRX 445555	1RRRRRRS 666677	1RRRRRRS 778888

Table 12 The synchronization pattern at E7 for 600 bits/s

multiframe 1	00000000	1PPPPPPS 111111	1PPPPPPX 112222	1PPPPPPS 222233	1PPPPPPS 333333
	1EEEEEE1 123456	1PPPPPPS 444444	1PPPPPPX 445555	1PPPPPPS 555566	1PPPPPPS 666666
multiframe 2	00000000	1PPPPPPS 777777	1PPPPPPX 778888	1PPPPQQS 888811	1QQQQQQS 111111
	1EEEEEE1 123456	1QQQQQQS 222222	1QQQQQQX 223333	1QQQQQQS 333344	1QQQQQQS 444444
multiframe 3	00000000	1QQQQQQS 555555	1QQQQQQX 556666	1QQQQQQS 666677	1QQQQQQS 777777
	1EEEEEE1 123456	1QQQQQQS 888888	1QQRRRRX 881111	1RRRRRRS 111122	1RRRRRRS 222222
multiframe 4	00000000	1RRRRRRS 333333	1RRRRRRX 334444	1RRRRRRS 444455	1RRRRRRS 555555
	1EEEEEEO	1RRRRRRS 666666	1RRRRRRX 667777	1RRRRRRS 777788	1RRRRRRS 888888

After two multiframes the E7 bit changes from logic 1 to logic 0. This indicates that three complete data bytes have been transmitted.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Register W4

If S OFF is set to logic 1 S114/115 will be forced to logic 1.
If B OFF is set to logic 1 B will be forced to logic 1.
With 106 ON and 106 OFF it is possible to clamp output Q106 (pin 2) to logic 1 or logic 0, or, for Q106 to indicate the received X-bits. The settings for 106 ON and 106 OFF are given in Table 13.

Table 13 Settings for 106 ON and 106 OFF

106 OFF	106 ON	Q106
0	0	output Q106 indicates the received X bits
0	1	output Q106 clamped to logic 0
1	0	output Q106 clamped to logic 1
1	1	output Q106 clamped to logic 1

When ND is set to logic 0 R104 and I109 become byte-timing synchronous. This is realized by delaying the incoming data from the remote subscriber. For 'V' series interfaces no byte-timing is requested. When ND is set to logic 1 R104 and I109 are not byte-timing synchronous and no extra delay is inserted.

When H1 is set to logic 1 the HWO will be clamped internally to logic 1 (see Fig.7).
In the receiver section of the DRA a synchronization system searches for the E7 synchronization bits for data at 600 and 1200 bits/s. When DR is set to logic 1 the synchronization system will be switched OFF consequently R104 and I109 will not be byte-timing synchronous.

If ND is set to logic 0 the I109 signal change can be timed in two modes. When NC (no CCITT) is set to logic 0 the I109 signal will be inverted at the first logic 1 to logic 0 transition of S114/115 after the logic 1 to logic 0 transition of 'B'. When NC is set to logic 1 I109 will be inverted at the logic 1 to logic 0 transition of S114/115 when 'B' is set to logic 1. At the same time the 8th data bit will be clocked out on R104 (I109 is one bit earlier as defined in CCITT X.30).

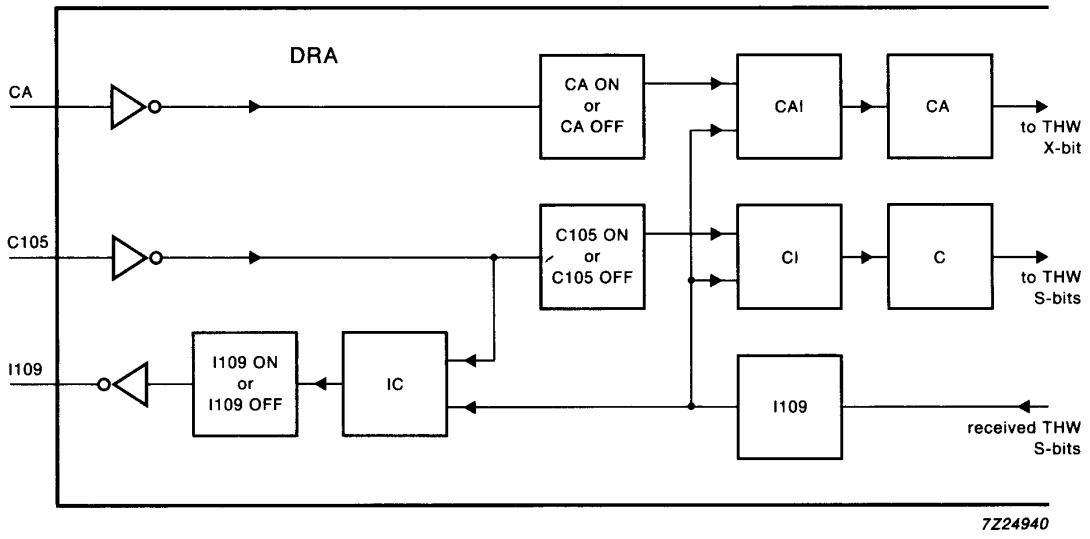

Fig.8 Interchange loops.

Registers R0 to R2

Table 14 Bit assignment registers R0 to R2

reg	7	6	5	4	3	2	1	0
R0	–	E7	E6	E5	E4	E3	E2	E1
R1	–	–	T103	R104	IA	I109	CA	C
R2	–	–	–	–	ACTT	ACTR	OOS	AL

Register R0

In every 10-byte multiframe (for data rates not exceeding 38400 bits/s) bits E1 to E7 are available to transmit information concerning the data rate.
The information that is inserted by the remote subscriber is received in these bits. For data rates of 600 and 1200 bits/s, bit 7 is only inserted in the frame when DE7 is set to logic 1.
If DE7 is set to logic 0 a synchronization pattern will be inserted at E7 in accordance with CCITT X.30/V.110.
For data rates from 48000 to 64000 bits/s and the asynchronous mode, no 'E' bits are received.

Register R1

Bit 'C' indicates the conditions of C105. If 'C' is set to logic 0 then C105 is OFF. The transmission S-bits are set to logic 0 (see Fig.8).
Bit CA indicates the condition of signal CA. If CA is set to logic 0 the signal will be OFF. The transmitted X-bits are set to logic 0 (see Fig.8).
Bit I109 indicates the condition of signal I109. If the received S-bits are set to logic 0 the bit I109 will be set to logic 0 (see Fig.8).
Bit IA is set to logic 0 if the received X-bits are at logic 0 (see Fig.8).
Bit R104 indicates the condition of signal R104. If the received data bits are at logic 0, R104 will be set to logic 0.
Bit T103 indicates the condition of signal T103. If bit T103 is at logic 0 signal T103 will be at logic 0. The transmitted data bits are set to logic 0.

Register R2

Bit AL indicates the out of synchronization (OOS) of the receiver between two successive readouts. Immediately after the readout the bit is reset. If the OOS bit is set to logic 0 then the DRA is in synchronization and at logic 1 is out of synchronization. The synchronization check is performed by the receiver section and is required to synchronize the internal clock generator for frame encoding (i.e. checks that the frame bits are correctly positioned in the frame). If the frame bits are not correctly positioned the following should be verified;

- The clock unit is preset to the correct position
- Frame bits have not been distorted. The DRA sends an OOS after three consecutive incorrect multiframes (with one or more errors per multiframe) then begins to search for the correct timing
  - after receiving eight zero frame bits the clock unit is preset to the correct position
  - if the following frame bits in that multiframe are received correctly the DRA is assumed to be in synchronization and the OOS bit will be reset
  - if the frame bits are not all correct the OOS bit will remain at logic 1 and the DRA will search for the next eight zero frame bits

Bit ACTR checks the activity of the remote subscriber by controlling the incoming highway.

Activity – ACTR = logic 1
No activity – ACTR = logic 0

After reading the register the bits are automatically set to zero ready for the next activity check.
Bit ACTT checks the activity of the local DTE transmit circuit.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
DC supply voltage		V_{DD}	−0.5	7.0	V
DC supply current		$\pm I_{DD}$	−	50	mA
DC ground current		$\pm I_{GND}$	−	30	mA
DC input diode current	$V_I < -0.5$ or $V_I > V_{DD} + 0.5$ V	$\pm I_{IK}$	−	20	mA
DC output diode current	$V_O < -0.5$ or $V_O > V_{DD} + 0.5$ V	$\pm I_{OK}$	−	20	mA
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	0	70	°C
Total power dissipation		P_{tot}	−	500	mW

DEVELOPMENT DATA

DC CHARACTERISTICS

T_{amb} = 25 °C; voltages are referenced to ground

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Quiescent supply current	V_{DD} = 5.5 V	I_{DD}	–	–	50	μA
INPUTS						
Input voltage HIGH						
CMOS input pin 4 (test)	V_{DD} = 4.5 to 5.5 V	V_{IH}	0.7×V_{DD}	–	–	V
TTL inputs and I/Os	V_{DD} = 4.5 to 5.5 V	V_{IH}	2.0	–	–	V
Input voltage LOW						
CMOS input pin 4 (test)	V_{DD} = 4.5 to 5.5 V	V_{IL}	–	–	0.3×V_{DD}	V
TTL inputs and I/Os	V_{DD} = 4.5 to 5.5 V	V_{IL}	–	–	0.8	V
Input leakage current	V_I = V_{DD} or GND	± I_I	–	–	0.1	μA
OUTPUTS						
Output 1 (pins 2,3,7,8,26 and 27)						
Output voltage LOW	V_{DD} = 5 V I_{OL} = 1.5 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	V_{DD} = 5 V $-I_{OH}$ = 2 mA	V_{OH}	2.4	–	–	V
Output 2 (pins 13 and 18 to 24)						
Output voltage LOW	V_{DD} = 5 V I_{OL} = 4.5 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	V_{DD} = 5 V $-I_{OH}$ = 3 mA	V_{OH}	4.3	–	–	V
3-state OFF current	V_O = V_{DD} or GND I_O = 0	± I_{OZ}	–	–	0.5	μA

AC CHARACTERISTICS

T_{amb} = 25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance		C_I	–	–	10	pF
Input/output capacitance		$C_{I/O}$	–	–	20	pF

TIMING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; GND = 0 V

parameter	conditions	symbol	min.	typ.	max.	unit
TERMINAL HIGHWAY						
C20						
Clock period		tw_C	–	488	–	ns
FS						
Delay time with reference to C20		td_{CLFH}	50	–	150	ns
		td_{CHFL}	50	–	430	ns
HWI						
Data set-up time		ts_I	100	–	–	ns
HWO						
Rise time	CL = 30 pF	tt_{LH}	–	–	30	ns
Fall time	CL = 30 pF	tt_{HL}	–	–	30	ns
Data set-up time		ts_O	–	–	50	ns
INTERCHANGE INTERFACE						
S114/115						
Rise time	CL = 30 pF	tt_{LH}	–	–	100	ns
Fall time	CL = 30 pF	tt_{HL}	–	–	100	ns
T103						
Data set-up time		ts_T	100	–	–	ns
Data hold time		th_T	0	–	–	ns
R104						
Rise time	CL = 30 pF	tt_{LH}	–	–	100	ns
Fall time	CL = 30 pF	tt_{HL}	–	–	100	ns
Data set-up time		ts_{SR}	–	–	100	ns
C105						
Data set-up time		ts_{BC}	100	–	–	ns
Data hold time		th_{BC}	0	–	–	ns
Q106						
Rise time	CL = 30 pF	tt_{LH}	–	–	100	ns
Fall time	CL = 30 pF	tt_{HL}	–	–	100	ns
Data set-up time		ts_{SQ}	–	–	100	ns

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
I109						
Rise time	CL = 30 pF	tt_{LH}	–	–	100	ns
Fall time	CL = 30 pF	tt_{HL}	–	–	100	ns
Data set-up time		ts_{SI}	–	–	100	ns
CA						
Data set-up time		ts_C	100	–	–	ns
Data hold time		th_C	0	–	–	ns
B						
Rise time	CL = 30 pF	tt_{LH}	–	–	100	ns
Fall time	CL = 30 pF	tt_{HL}	–	–	100	ns
MICROCONTROLLER BUS						
ALE pulse width		tw_A	100	–	–	ns
Data bus READ cycle						
Address set-up time		ts_A	25	–	–	ns
Address hold time		th_A	10	–	–	ns
RDCEN pulse width		tw_R	500	–	–	ns
READ access time	CL = 200 pF	ta_R	–	–	200	ns
Data hold time		th_D	10	–	–	ns
Time from RDCEN HIGH to ALE LOW		td_{RA}	1	–	–	μs
Data bus WRITE cycle						
Address set-up time		ts_A	25	–	–	ns
Address hold time		th_A	10	–	–	ns
WRCEN pulse width		tw_W	100	–	–	ns
Data set-up time		ts_D	10	–	–	ns
Data hold time		th_D	10	–	–	ns
Time from WRCEN HIGH to ALE LOW		td_{WA}	10	–	–	ns

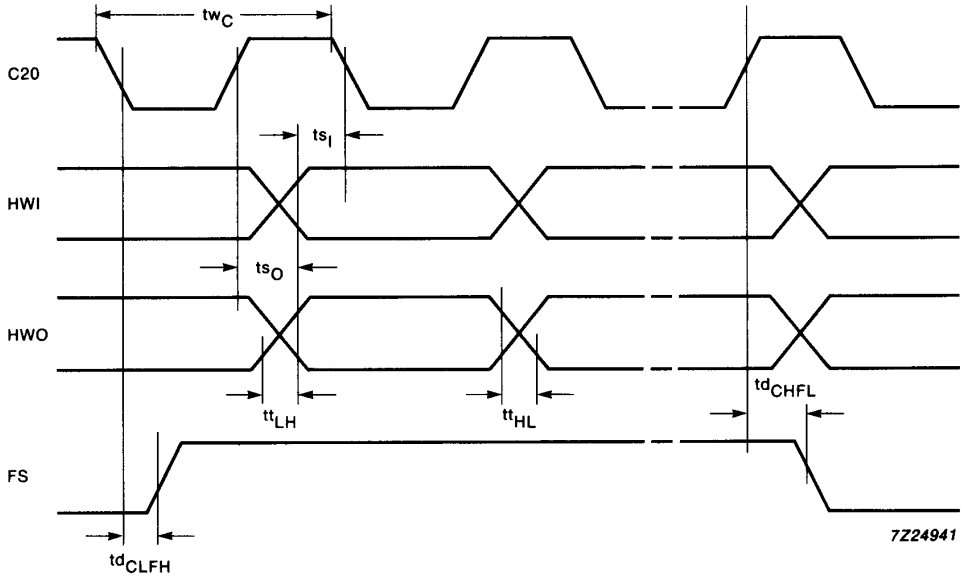

Fig.9 Terminal highway timing diagram.

DEVELOPMENT DATA

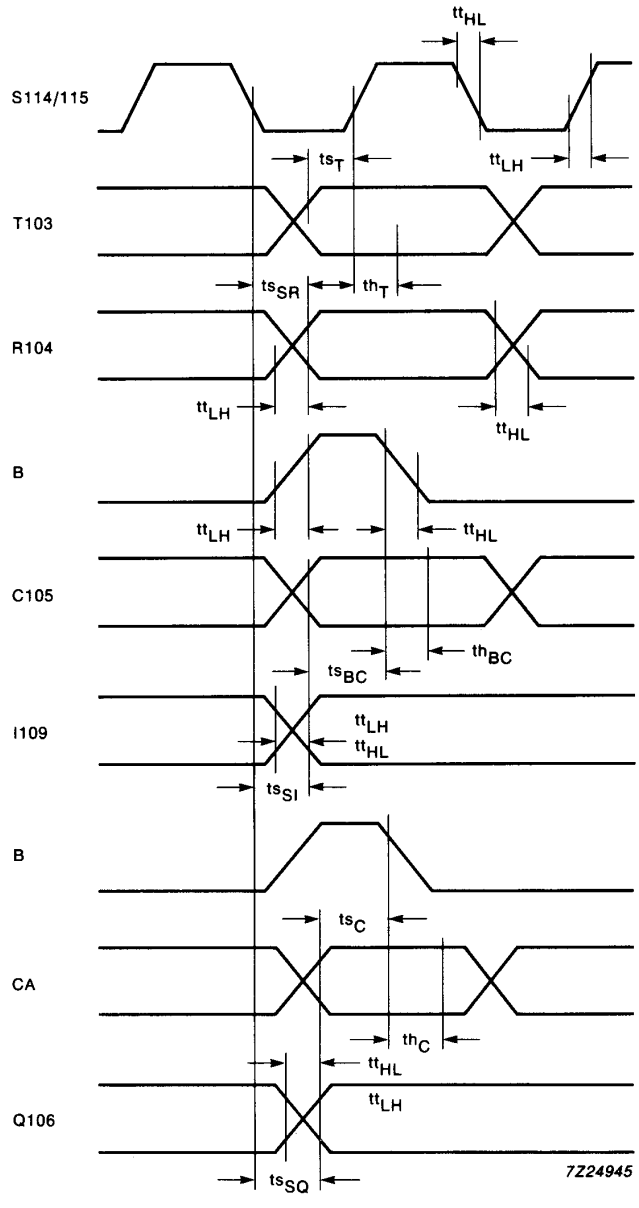

Fig.10 Interchange interface timing diagram.

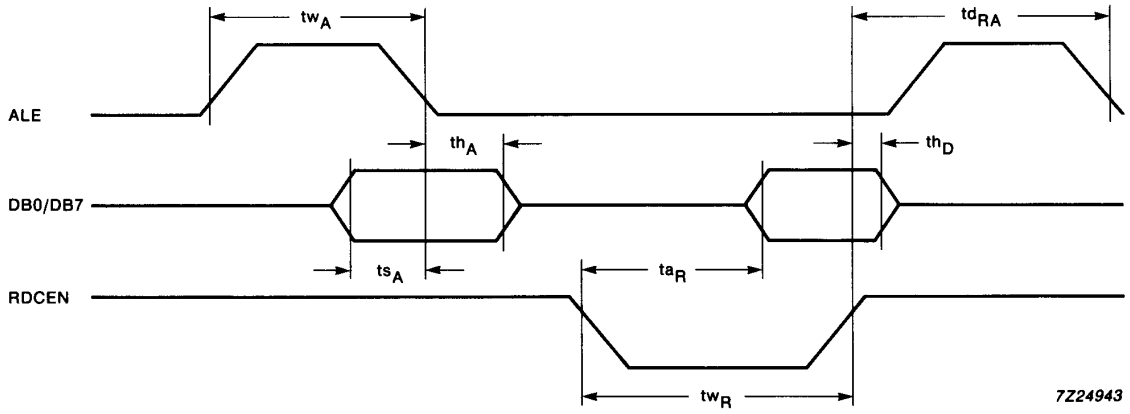

Fig.11 Data bus READ cycle timing diagram.

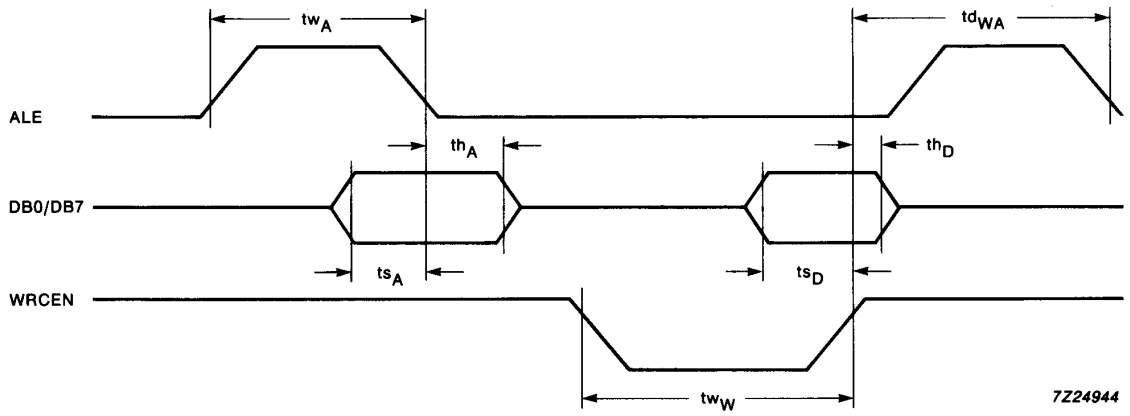

Fig.12 Data bus WRITE cycle timing diagram.

APPENDIX A

INTERMEDIATE FRAME FORMATS

Table A1 Frame format for the intermediate datastream for synchronous user data rates when no bit repetition is used (4800, 9600 and 19200 bits/s).

OCTET	bit number 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1/P1	D2/P2	D3/P3	D4/P4	D5/P5	D6/P6	S1/SQ
2	1	D7/P7	D8/P8	D9/Q1	D10/Q2	D11/Q3	D12/Q4	X
3	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
4	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D25/P1	D26/P2	D27/P3	D28/P4	D29/P5	D30/P6	S6/SQ
7	1	D31/P7	D32/P8	D33/Q1	D34/Q2	D35/Q3	D36/Q4	X
8	1	D37/Q5	D38/Q6	D39/Q7	D40/Q8	D41/R1	D42/R2	S8/SR
9	1	D43/R3	D44/R4	D45/R5	D46/R6	D47/R7	D48/R8	S9/SP

Frame format on the terminal highway for the synchronous user data rate of 38400 bits/s (V.110/X.30).

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4, S6, S8, S9 X D1 to D48	109 IA (microcontroller read) 106 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

Table A2 Frame format of the intermediate data stream (8 kbits/s) with a synchronous user data rate of 2400 bits/s (V.110/X.30).

OCTET	bit number 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1/P1	D1/P1	D2/P2	D2/P2	D3/P3	D3/P3	S1/SP
2	1	D4/P4	D4/P4	D5/P5	D5/P5	D6/P6	D6/P6	X
3	1	D7/P7	D7/P7	D8/P8	D8/P8	D9/Q1	D9/Q1	S3/SQ
4	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S4/SQ
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S6/SR
7	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D18/R2	D18/R2	X
8	1	D19/R3	D19/R3	D20/R4	D20/R4	D21/R5	D21/R5	S8/SR
9	1	D22/R6	D22/R6	D23/R7	D23/R7	D24/R8	D24/R8	S9/SP

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	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4, S6, S8, S9 X D1 to D48	109 IA (microcontroller read) 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

Table A3 Frame format of the intermediate datastream (8 kbits/s) for a synchronous user data rate of 1200 bits/s (V.110).

OCTET	bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1	D1	D1	D1	D2	D2	S1
2	1	D2	D2	D3	D3	D3	D3	X
3	1	D4	D4	D4	D4	D5	D5	S3
4	1	D5	D5	D6	D6	D6	D6	S4
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D7	D7	D7	D7	D8	D8	S6
7	1	D8	D8	D9	D9	D9	D9	X
8	1	D10	D10	D10	D10	D11	D11	S8
9	1	D11	D11	D12	D12	D12	D12	S9

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4, S6, S8, S9 X D1 to D48	109 IA (microcontroller read) 106 104

Table A4 Frame format of the intermediate datastream (8 kbits/s) for the user data rate of 600 bits/s (V.110/X.30).

OCTET	bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1/P1	D1/P1	D1/P1	D1/P1	D1/P1	D1/P1	S1/SP
2	1	D1/P1	D1/P1	D2/P2	D2/P2	D2/P2	D2/P2	X
3	1	D2/P2	D2/P2	D2/P2	D2/P2	D3/P3	D3/P3	D3/SP
4	1	D3/P3	D3/P3	D3/P3	D3/P3	D3/P3	D3/P3	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D4/P4	D4/P4	D4/P4	D4/P4	D4/P4	D4/P4	S6/SP
7	1	D4/P4	D4/P4	D5/P5	D5/P5	D5/P5	D5/P5	X
8	1	D5/P5	D5/P5	D5/P5	D5/P5	D6/P6	D6/P6	S8/SP
9	1	D6/P6	D6/P6	D6/P6	D6/P6	D6/P6	D6/P6	S9/SP
0	0	0	0	0	0	0	0	0
1	1	D7/P7	D7/P7	D7/P7	D7/P7	D7/P7	D7/P7	S1/SP
2	1	D7/P7	D7/P7	D8/P8	D8/P8	D8/P8	D8/P8	X
3	1	D8/P8	D8/P8	D8/P8	D8/P8	D9/Q1	D9/Q1	S3/SP
4	1	D9/Q1	D9/Q1	D9/Q1	D9/Q1	D9/Q1	D9/Q1	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	S6/SQ
7	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D11/Q3	D11/Q3	X
8	1	D11/Q3	D11/Q3	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S8/SQ
9	1	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	S9/SP
0	0	0	0	0	0	0	0	0
1	1	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	S1/SP
2	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D14/Q6	D14/Q6	X
3	1	D14/Q6	D14/Q6	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S3/SP
4	1	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	S6/SQ
7	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D17/R1	D17/R1	X
8	1	D17/R1	D17/R1	D17/R1	D17/R1	D18/R2	D18/R2	S8/SQ
9	1	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	S9/SP
0	0	0	0	0	0	0	0	0
1	1	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	S1/SP
2	1	D19/R3	D19/R3	D20/R4	D20/R4	D20/R4	D20/R4	X
3	1	D20/R4	D20/R4	D20/R4	D20/R4	D21/R5	D21/R5	S3/SP
4	1	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	S6/SQ
7	1	D22/R6	D22/R6	D23/R7	D23/R7	D23/R7	D23/R7	X
8	1	D23/R7	D23/R7	D23/R7	D23/R7	D24/R8	D24/R8	S8/SQ
9	1	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	S9/SP

DEVELOPMENT DATA

Table 4 (continued)

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4, S6, S8, S9 X D1 to D48	109 IA (microcontroller read) 106 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

Table A5 Frame format on the terminal highway for synchronous user data of 48 kbits/s and asynchronous user data rates up to 19.2 kbits/s (V series only).

OCTET	bit number							
	1	2	3	4	5	6	7	8
1	1	D1/P1	D2/P2	D3/P3	D4/P4	D5/P5	D6/P6	S1/SQ
2	0	D7/P7	D8/P8	D9/Q1	D10/Q2	D11/Q3	D12/Q4	X
3	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
4	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4 X D1 to D24	109 IA (microcontroller read) 106 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

DEVELOPMENT DATA

Table A6 Frame format on the terminal highway for synchronous data rates of 56 kbits/s. When 'S' is set to logic 1 the frame will comply to V.110.

OCTET	bit number							
	1	2	3	4	5	6	7	8
1	D1	D2	D3	D4	D5	D6	D7	S
2	D8	D9	D10	D11	D13	D13	D14	S
3	D15	D16	D17	D18	D19	D20	D21	S
4	D22	D23	D24	D25	D26	D27	D28	S

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S no transmission D1 to D28	109 IA (microcontroller read) 106 104
X series	C CA T	S no transmission D1 to D28	I IA (microcontroller read) R

Table A7 Frame format on the terminal highway for synchronous data rates of 64 kbits/s

OCTET	bit number							
	1	2	3	4	5	6	7	8
1	D1	D2	D3	D4	D5	D6	D7	D8
2	D9	D10	D11	D12	D13	D14	D15	D16
3	D17	D18	D19	D20	D21	D22	D23	D24
4	D25	D26	D27	D28	D29	D30	D31	D32

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	no transmission no transmission D1 to D32	109 IA (microcontroller read) 106 104
X series	C CA T	no transmission no transmission D1 to D32	I IA (microcontroller read) R

DEVELOPMENT DATA

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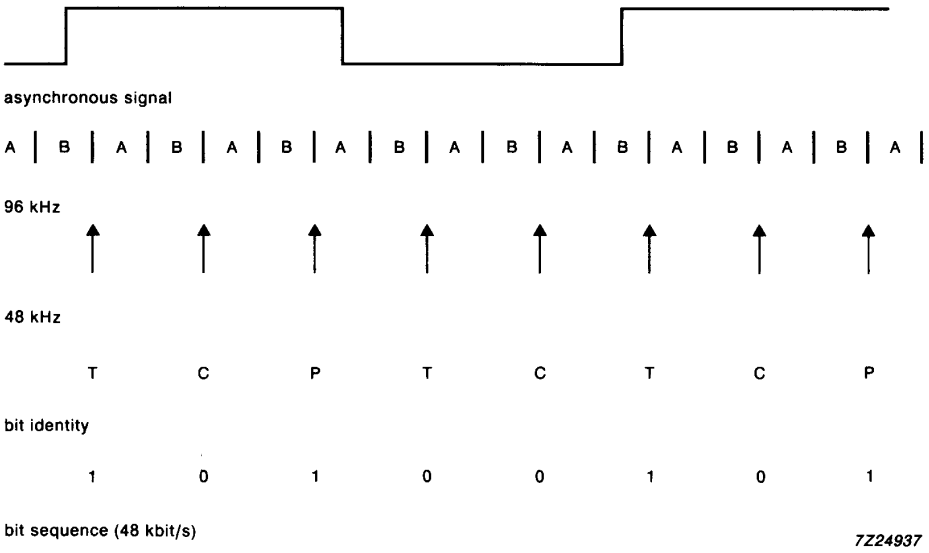
APPENDIX B

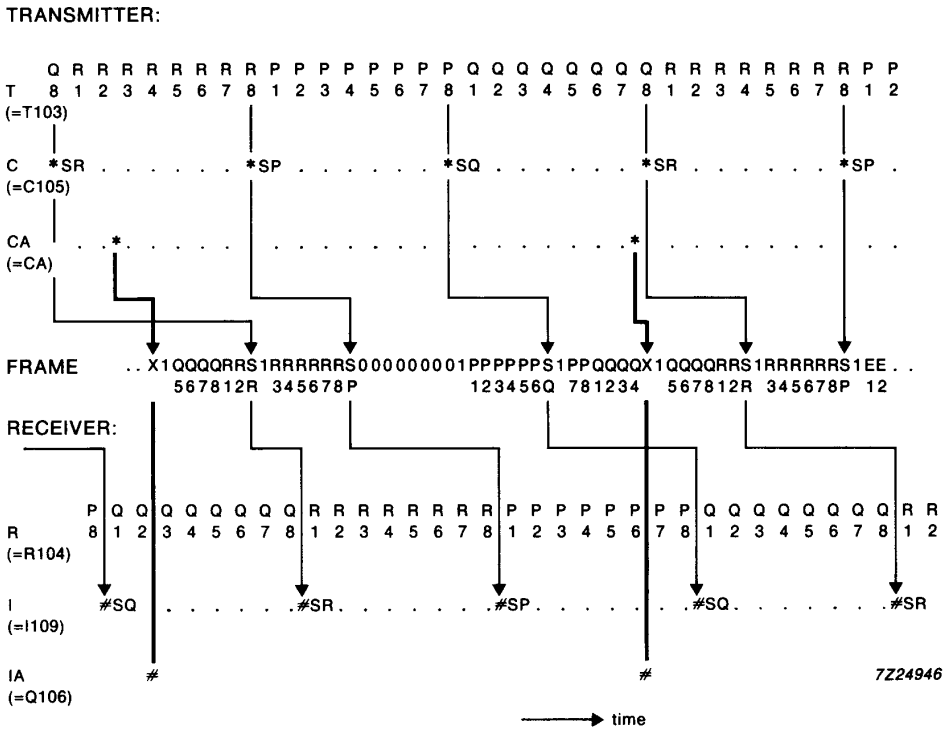
SAMPLE MOMENTS OF THE INTERCHANGE CIRCUITS



code character for a transition (C)		position of the transition in a group of two sampling pulses
from 1 to 0	from 0 to 1	
T C	T C	
0 0	1 1	in first half (A)
0 1	1 0	in second half (B)

Additional transition coding is based on R.111. However, in R.111, two transition code characters (C1 and C2) are used for each signal transition instead of one (C).

Fig.A1 Additional transition coding.

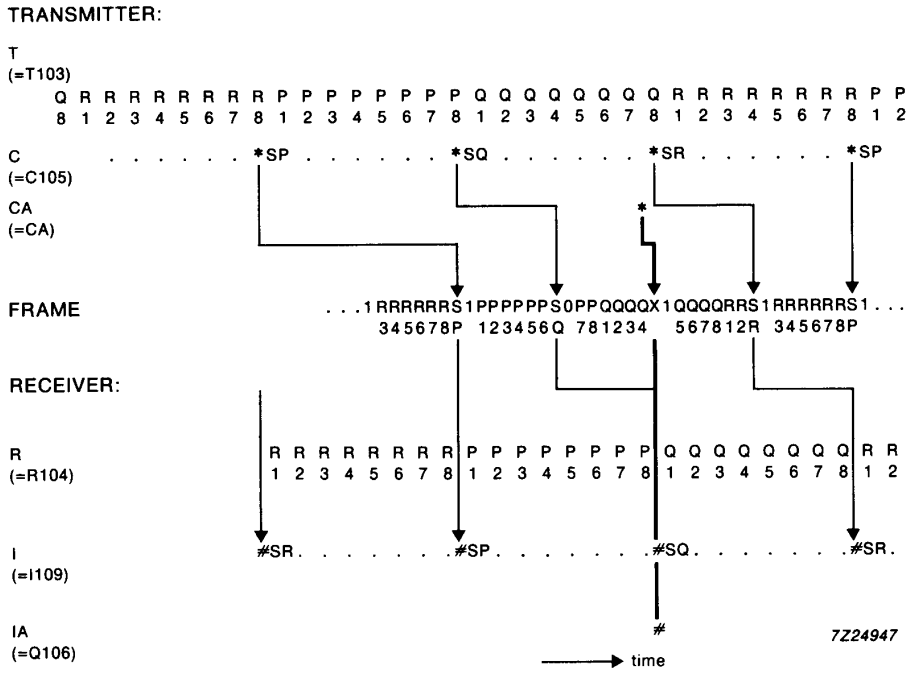


Notes

* sample moment of the interchange circuit
\# change point of the interchange circuit

When bit repetition is used (600 and 2400 bits/s) the value of the last sample of the interchange circuits is repeated in the 'S' and 'X' data bits until a new sample is made (see Appendix A Table A2 and A4).

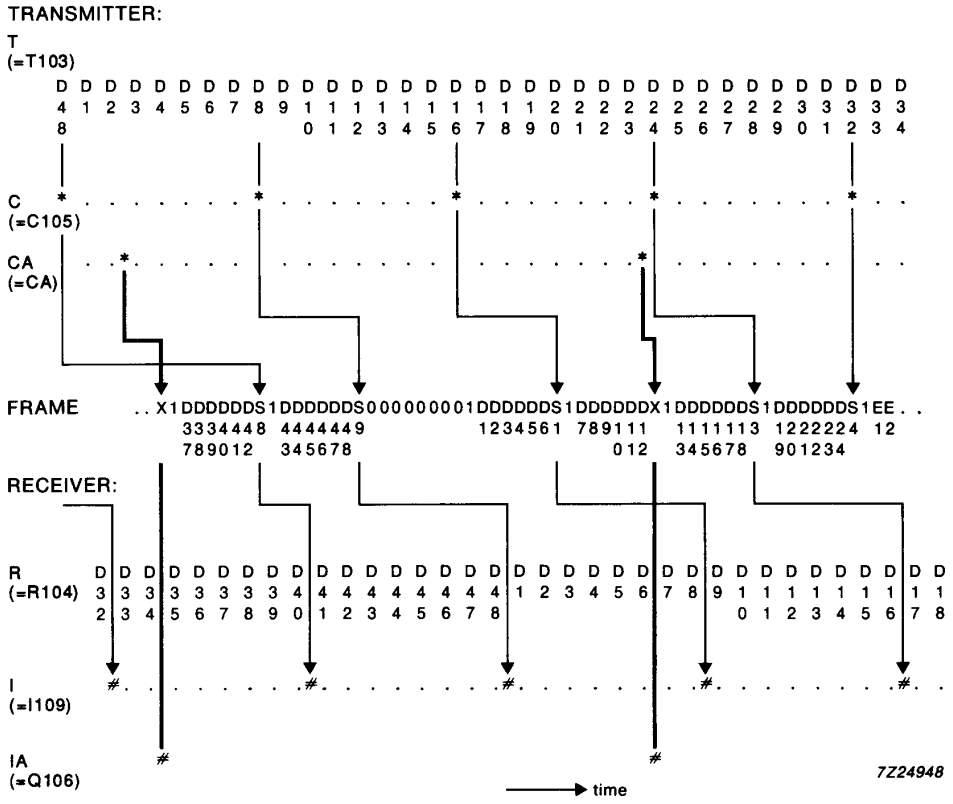
Fig.B1 Sample moments and change points of the interchange circuit C, CA, IA and I using a 10-byte frame (REC. X.30).



Notes

* sample moment of the interchange circuit
\# change point of the interchange circuit

Fig.B2 Sample moments and change points of the interchange circuit C, CA, IA and I using a 4-byte frame (REC. X.30).

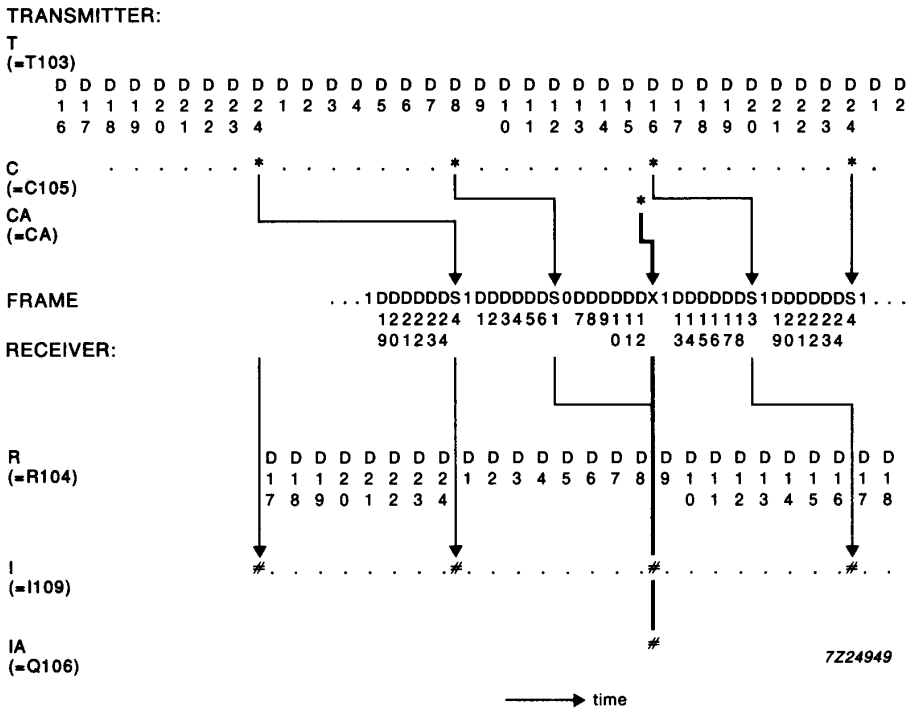


Notes

* sample moment of the interchange circuit
\# change point of the interchange circuit

When bit repetition is used (600, 1200 and 2400 bits/s) the value of the last sample of the interchange circuits is repeated in the 'S' and 'X' data bits until a new sample is made (see Appendix A Tables A2, A3 and A4).

Fig.B3 Sample moments and change points of the interchange circuit 105, CA, 106 and 109 using a 10-byte frame (REC. V.110).



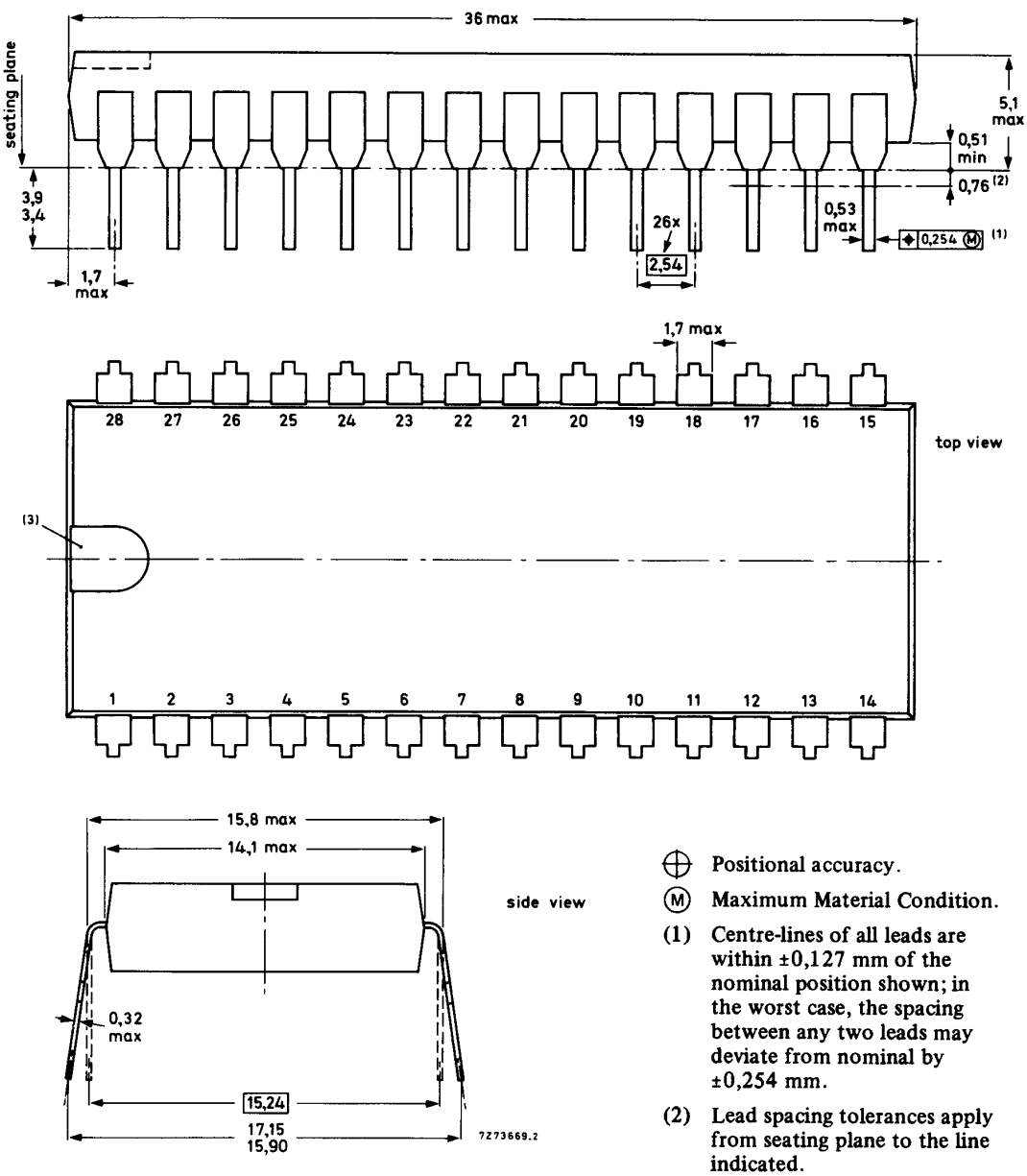
Notes

* sample moment of the interchange circuit
\# change point of the interchange circuit

Fig.B4 Sample moments and change points of the interchange circuit 105, CA, 106 and 109 using a 4-byte frame (REC. V.110).

DEVELOPMENT DATA

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.