Philips Components

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDE8712D

8-bit video digital-to-analog converter

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation (250 mW typical)
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Test and measurement
- Telecommunications
- Radar/sonar
- Image processing

DESCRIPTION

The TDE8712D is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for professional video and other applications. The operating temperature range is -55 °C to +125 °C. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8712D	16	CERDIP	ceramic	SOT74

PHILIPS

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
V_{OUT} – $\overline{V_{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 Ω	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		50	-	-	MHz
B	–3 dB bandwidth	f_{CLK} = 50 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

8-bit video digital-to-analog converter TDE8712D

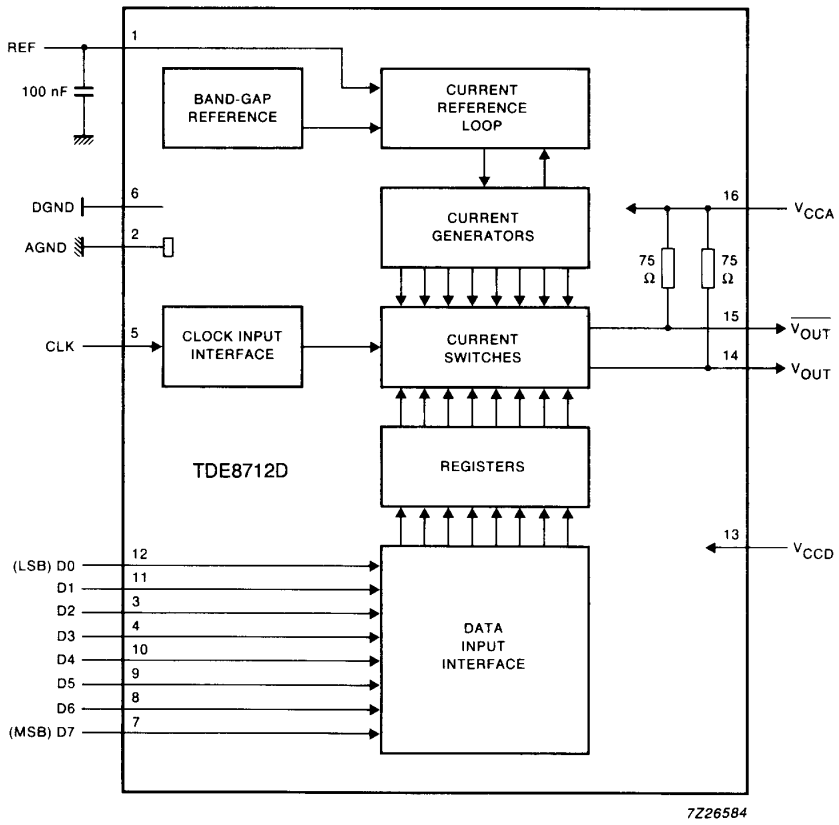


Fig.1 Block diagram.

8-bit video digital-to-analog converter TDE8712D

PIN CONFIGURATION

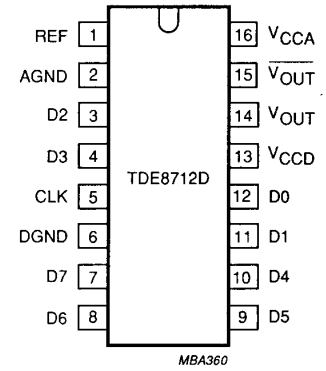


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	−0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+ 0.5	V
AGND – DGND	ground voltage differential	−0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
I_{OUT}	total output current range (pin 14)	−5	+ 26	mA
$\overline{I_{OUT}}$	total output current range (pin 15)	−5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−55	+125	°C
T_j	junction temperature	-	+175	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT74	112	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.75$ V to 5.25 V; $V_{CCD} = V_{13} - V_6 = 4.75$ V to 5.25 V; $V_{CCA} - V_{CCD} = -0.25$ V to +0.25 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = -55$ °C to +125 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
AGND – DGND	ground voltage differential		−0.1	-	0.1	V
Inputs DIGITAL INPUTS (D7 - D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	−0.3	−0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		50	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltages (peak- to-peak value)	$Z_L = 10$ kΩ	−1.45	−1.61	−1.75	V
		$Z_L = 75$ Ω	−0.72	−0.80	−0.88	V
V_{offset}	analog offset output voltage	code = 0	-	−3	−25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	−3 dB bandwidth	note 3; $f_{CLK} = 50$ MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω
Transfer function ($f_{CLK} = 50$ MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (fCLK = 50 MHz; notes 4 and 5; see Figs 3,4 and 5)						
$t_{SU;DAT}$	data set-up time		−0.3	-	-	ns
$t_{HD;DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; $f_{CLK} = 50$ MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V_{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).

5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;\ DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.

6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

DAC OUTPUT VOLTAGES					
CODE	BINARY INPUT DATA (D7 - D0)	Z_L = 10 kΩ	Z_L = 75 Ω		
		$\overline{V_{OUT}}$ (V)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)	V_{OUT} (V)
0	000 000 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	. . . . .	.	.	.	.
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	. . . . .	.	.	.	.
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0

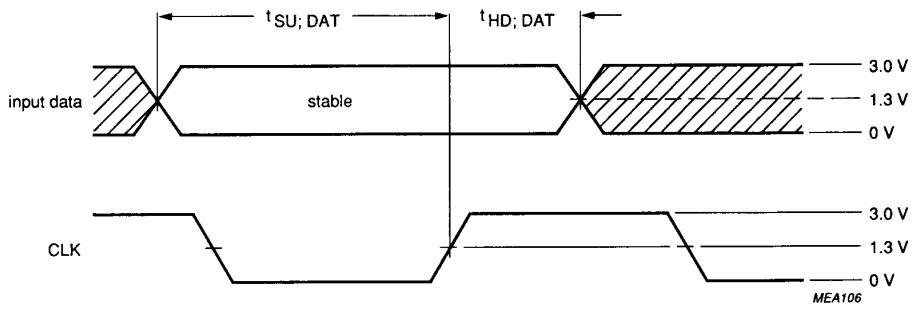


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\ DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\ DAT}$ = +2 ns).

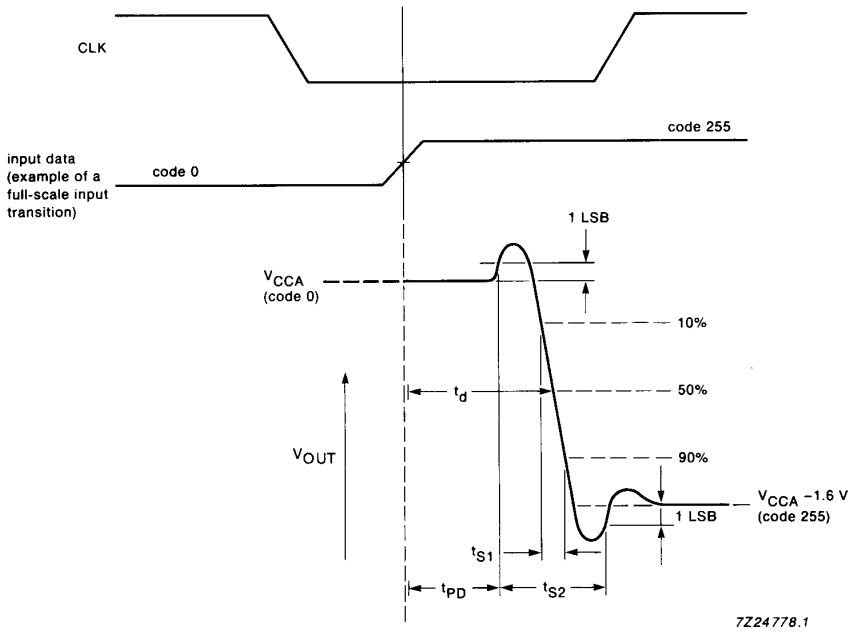


Fig.4 Switching characteristics.

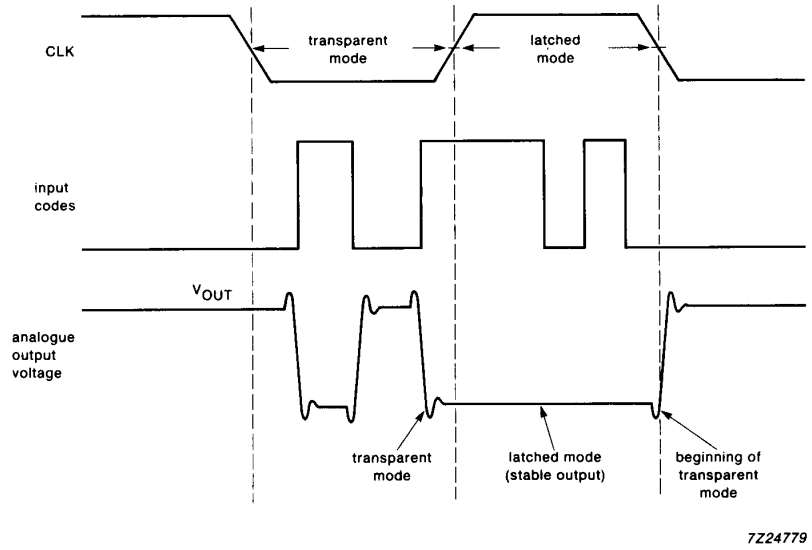


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

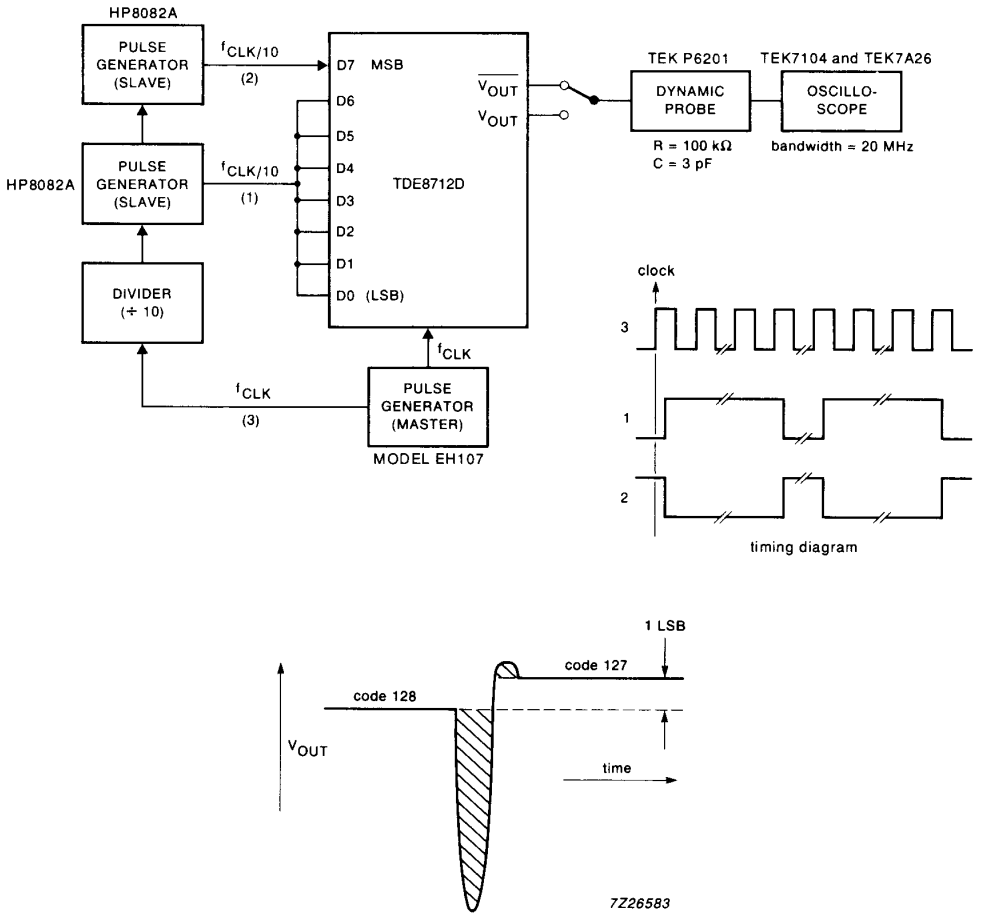


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

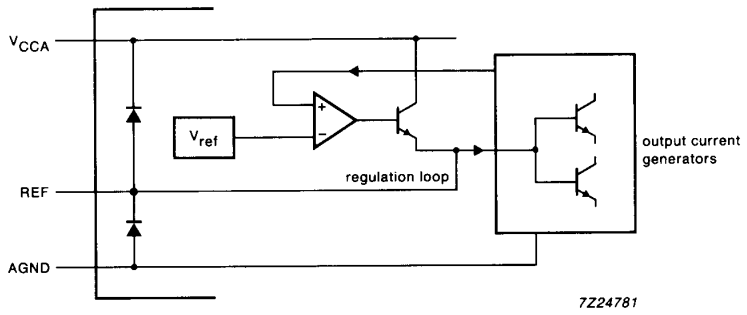


Fig.7 Reference voltage generator decoupling.

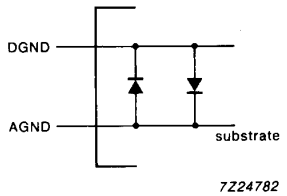


Fig.8 AGND and DGND.

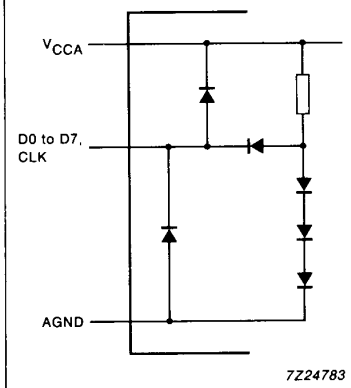


Fig.9 D7 to D0 and CLK.

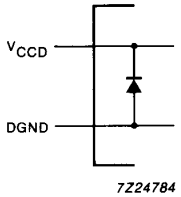


Fig.10 Digital supply.

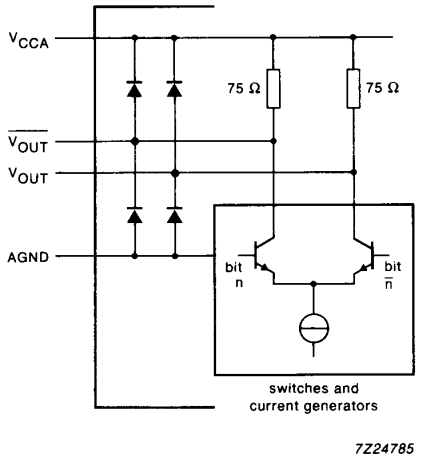


Fig.11 Analog outputs.

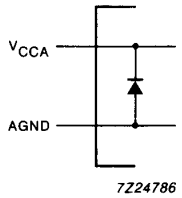


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

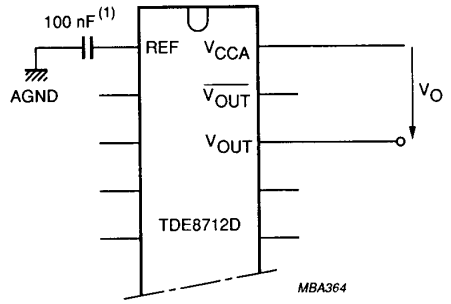


Fig.13 Analog output voltage without external load ($V_O = -\overline{V_{OUT}}$; see Table 1, Z_L = 10 kΩ).

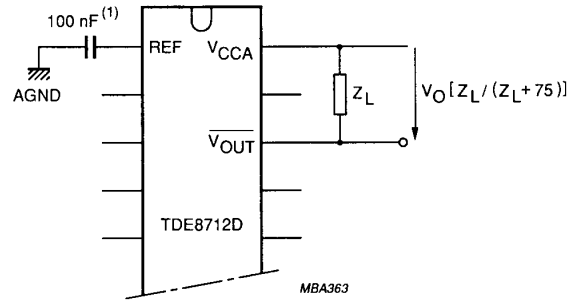


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

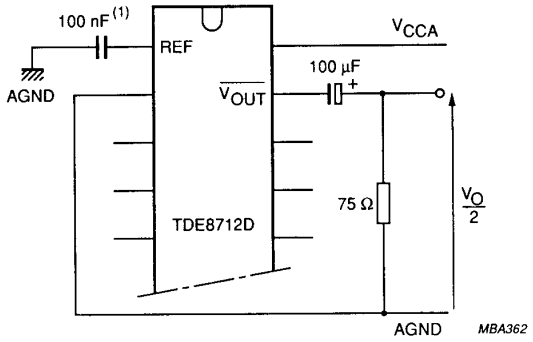


Fig.15 Analog output with AGND as reference.

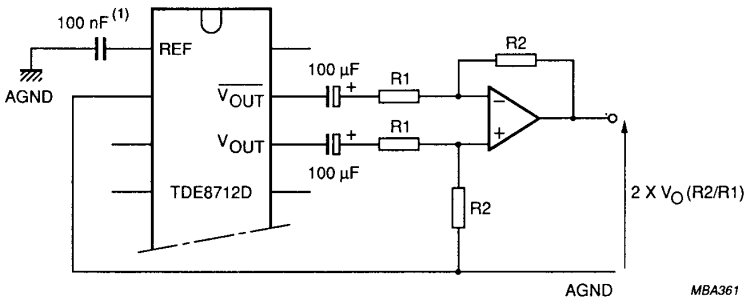
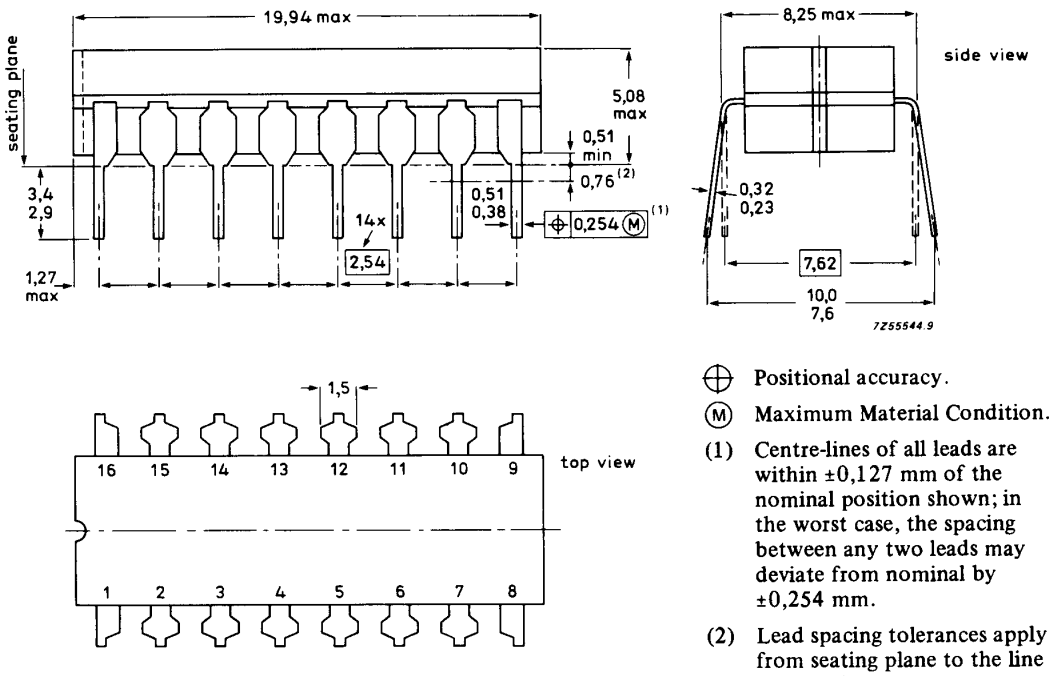


Fig.16 Differential mode (improved supply voltage ripple rejection).

Notes to Figs 13, 14, 15 and 16

1. This is a recommended value for decoupling pin 1.

PACKAGE OUTLINE



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Fig.17 16-Lead dual in-line; ceramic (cerdip)(SOT74)

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been preheated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS (BY HAND)

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	

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