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ACL Products	

74AC/ACT11191

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

FEATURES

- Synchronous, reversible counting
- Positive edge-triggered clock
- 4-bit binary
- Asynchronous Parallel Load capability
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11191 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11191 is an asynchronously presettable up/down 4-bit binary counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.3	6.9	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	66	68	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency, CP → Q_n	C_L = 50pF	135	95	MHz

Note:

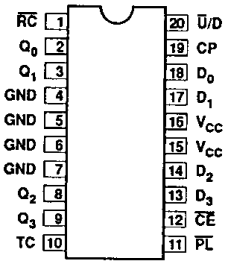
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

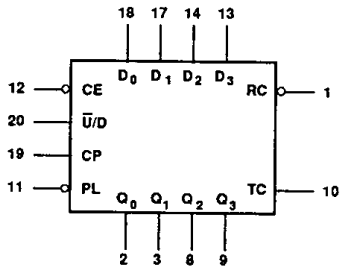
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11191N 74ACT11191N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11191D 74ACT11191D

PIN CONFIGURATION

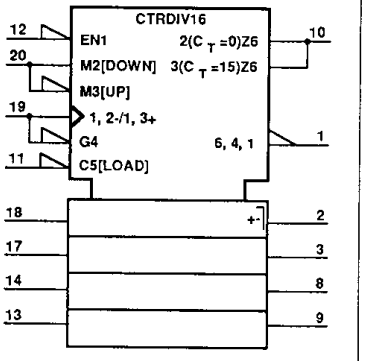
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

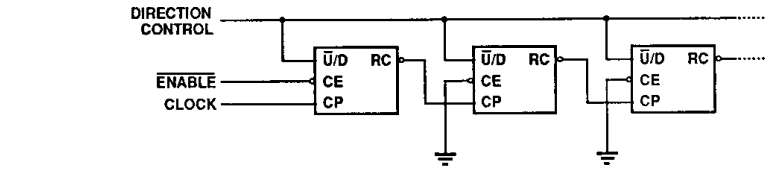
Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "15" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11191 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

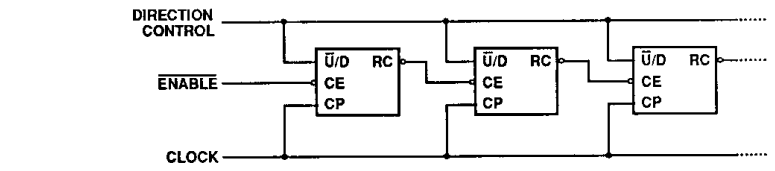
In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

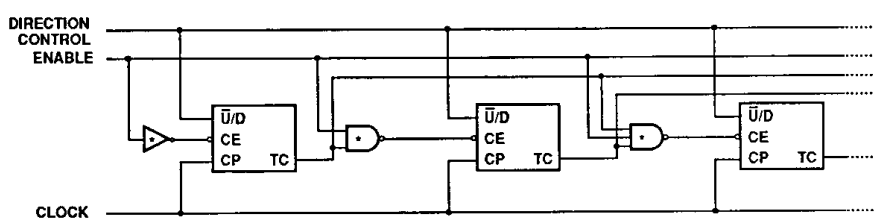
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock



b. Synchronous N-Stage Counter with Common Clock Using Ripple Clock



c. Synchronous N-Stage Counter with Common Clock and Parallel Gated Terminal Count

* Additional devices

Figure 1

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{U}/D$	Up/down count control input
12	$\overline{CE}$	Count enable input (active-Low)
18, 17, 14, 13	D_0 - D_3	Data inputs
19	CP	Clock pulse input (active rising edge)
11	$\overline{PL}$	Asynchronous load input (active-Low)
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	$\overline{RC}$	Ripple clock output (active-Low)
10	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	H	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
↑ = Low-to-High clock transition
↓ = High-to-Low Trickle Clock transition
⊓ = Low pulse

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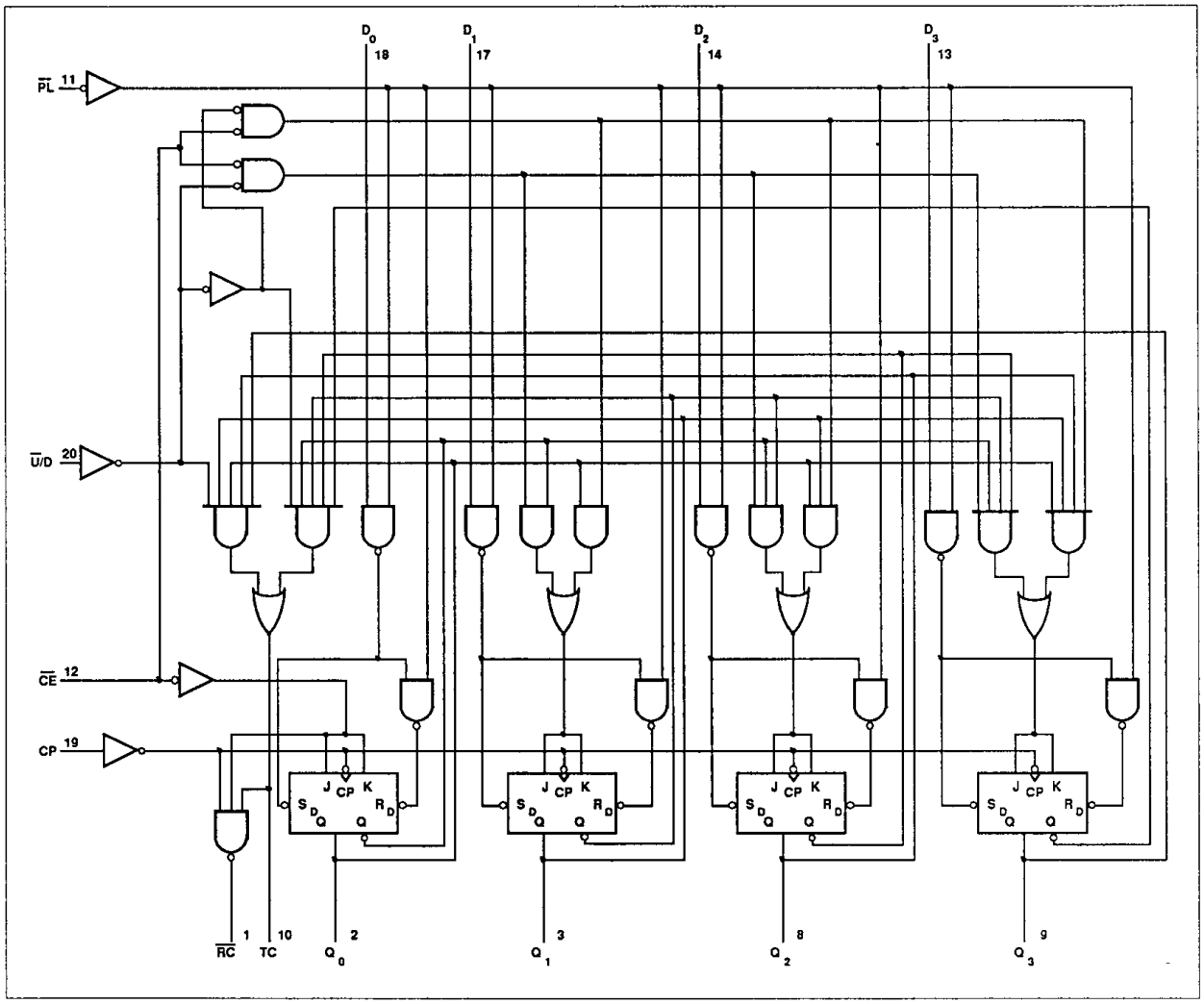
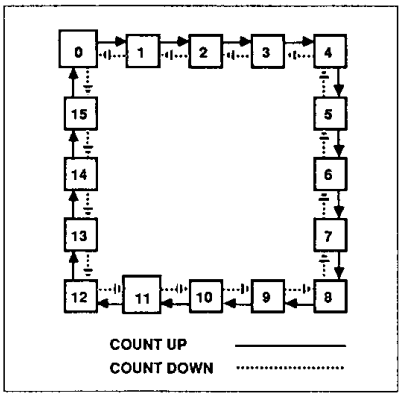
LOGIC DIAGRAM



STATE DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11191			74ACT11191			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11191				74ACT11191				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	50	80		50		MHz
		CP to $\overline{RC}$, TC		50	80		50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	2.2 2.7	7.5 7.5	9.8 11.0	2.2 2.7	11.1 12.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	3.7 4.1	9.9 10.2	12.2 14.4	3.7 4.1	13.8 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	2.8 2.8	8.7 7.8	11.5 10.6	2.8 2.8	12.9 11.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	2.5 2.6	7.2 6.6	9.0 8.8	2.5 2.6	10.3 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	4.1 4.1	11.2 10.2	14.4 14.3	4.1 4.1	15.9 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	2.7 3.1	8.7 8.3	11.5 11.8	2.7 3.1	12.7 13.6	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	3.4 3.5	9.8 8.9	12.3 12.1	3.4 3.5	13.8 13.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	4.7 4.0	13.5 11.8	18.2 17.1	4.7 4.0	20.7 19.3	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	5.0 5.3	14.7 15.1	19.9 21.1	5.0 5.3	22.5 24.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	3.7 3.6	10.7 9.3	13.4 12.3	3.7 3.6	14.9 14.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	5.0 4.6	14.2 12.6	18.7 17.5	5.0 4.6	21.1 19.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	5.2 6.0	15.4 15.7	20.2 21.6	5.2 6.0	22.9 24.7	ns
t_S	Setup time, High or Low D_n to $\overline{PL}$		6	4.0			4.0		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{CE}$ to CP		6	12.5			12.5		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{U}$/D to CP		6	13.5			13.5		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.8			4.8		ns
t_w	CP pulse width, High or Low		1	10.0			10.0		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.5			2.5		ns

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	100	135		100		MHz
		CP to $\overline{RC}$, TC		70	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.9 2.4	5.2 5.4	7.6 8.0	1.9 2.4	8.4 9.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	3.0 3.6	6.5 7.1	8.8 10.4	3.0 3.6	10.4 10.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	2.4 2.9	5.9 5.6	8.4 7.7	2.4 2.9	9.1 8.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	2.1 2.2	4.9 4.8	6.8 6.7	2.1 2.2	7.7 7.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	3.5 3.5	7.2 6.9	10.2 10.0	3.5 3.5	11.3 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	2.3 2.7	5.7 5.9	8.1 8.6	2.3 2.7	9.1 9.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	2.9 3.0	6.2 6.1	8.7 8.7	2.9 3.0	9.8 9.8	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	4.1 3.5	8.4 8.0	12.2 11.8	4.1 3.5	13.7 13.4	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	4.3 4.7	9.2 9.7	13.5 14.0	4.3 4.7	15.1 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	3.1 3.0	6.7 6.4	9.4 9.0	3.1 3.0	10.6 10.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	4.3 4.0	8.8 8.4	12.5 12.0	4.3 4.0	14.3 13.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	4.5 5.0	9.7 10.1	13.7 14.4	4.5 5.0	15.4 16.3	ns
t_s	Setup time, High or Low D_n to $\overline{PL}$		6	3.0			3.0		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	1.5			1.5		ns
t_s	Setup time, High or Low $\overline{CE}$ to CP		6	8.0			8.0		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	0.5			0.5		ns
t_s	Setup time, High or Low $\overline{U}$/D to CP		6	8.5			8.5		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.0			4.0		ns
t_w	CP pulse width, High or Low		1	7.2			7.2		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74ACT11191					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	65	95		65		MHz
		CP to $\overline{RC}$, TC		65	95		65		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	3.6 4.2	6.7 7.1	9.2 9.4	3.6 4.2	10.4 10.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	5.0 5.3	8.0 8.6	10.3 11.5	5.0 5.3	11.7 13.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	4.4 3.5	7.4 6.7	9.5 9.5	4.4 3.5	11.0 10.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	3.9 2.8	6.4 6.0	8.2 8.4	3.9 2.8	9.2 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	4.4 4.2	8.4 8.8	11.7 11.3	4.4 4.2	13.1 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	3.2 3.6	6.9 7.2	9.6 10.3	3.2 3.6	11.0 11.6	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	4.5 3.7	7.6 7.1	10.1 10.3	4.5 3.7	11.6 11.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	5.1 4.7	9.5 9.2	13.6 13.4	5.1 4.7	15.4 15.2	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	5.5 5.9	10.3 10.9	14.8 15.5	5.5 5.9	17.2 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	4.0 3.8	7.6 7.4	10.8 10.5	4.0 3.8	12.2 11.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	5.2 4.7	9.7 9.5	13.9 13.6	5.2 4.7	15.8 15.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	5.4 5.8	10.5 11.0	15.1 15.7	5.4 5.8	17.1 17.9	ns
t_S	Setup time, High or Low D_n to $\overline{PL}$		6	3.0			3.0		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	2.5			2.5		ns
t_S	Setup time, High or Low $\overline{CE}$ to CP		6	7.5			7.5		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	1.5			1.5		ns
t_S	Setup time, High or Low $\overline{U}$/D to CP		6	8.5			8.5		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.5			0.5		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.0			4.0		ns
t_w	CP pulse width, High or Low		1	7.7			7.7		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

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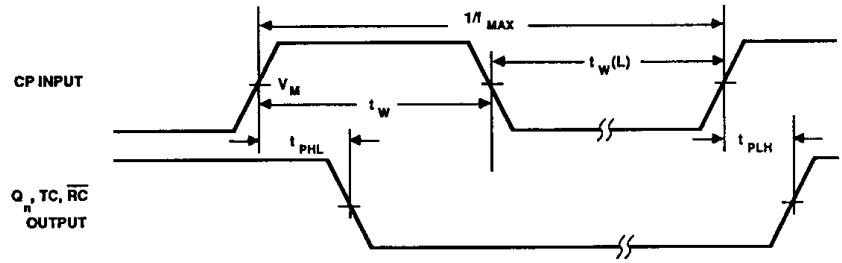
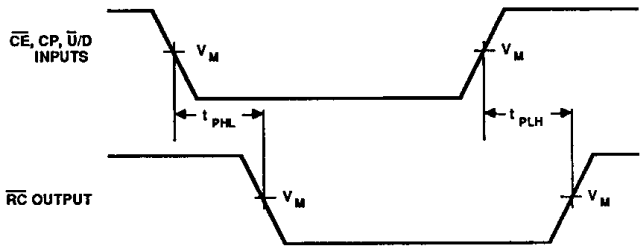
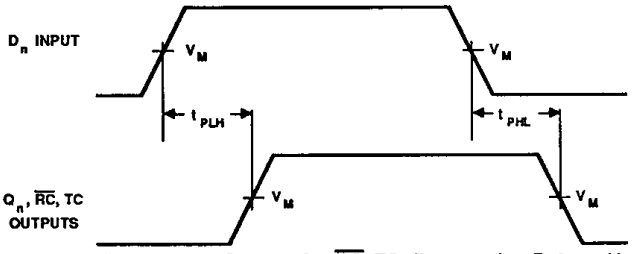
AC WAVEFORMS



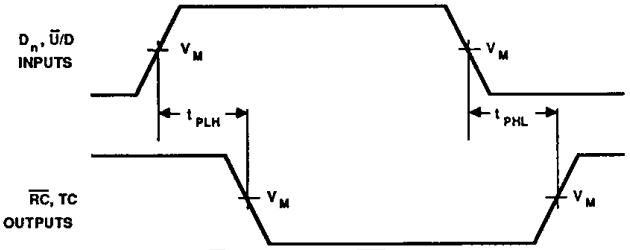
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Clock, Count Enable, or U/D to Ripple Clock Output Propagation Delay

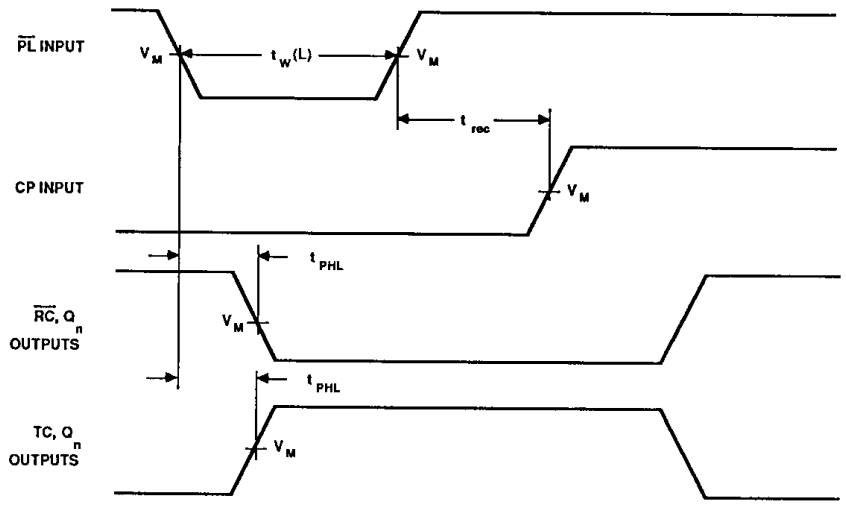


Waveform 3. Waveforms Showing the Input (D_n) to Output (Q_n, $\overline{RC}$, TC) Propagation Delays, Non-Inverting Path

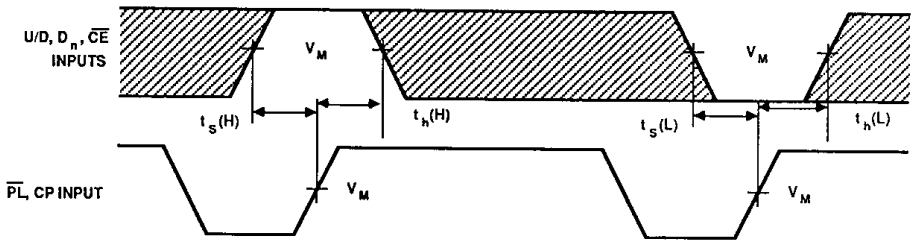


Waveform 4. Waveforms Showing the Input (D_n, $\overline{U}$/D) to Output ($\overline{RC}$, TC) Propagation Delays, Inverting Path

AC WAVEFORMS (continued)



Waveform 5. Waveforms Showing the Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



Waveform 6. Waveforms Showing Setup Time and Hold Time for D_n to $\overline{PL}$, $\overline{U}$/D to CP and $\overline{CE}$ to CP

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

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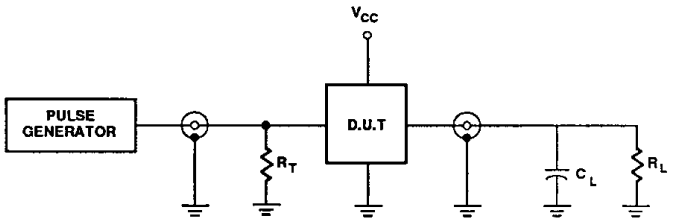
TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$