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ACL Products	

74AC/ACT11194

4-bit bidirectional universal shift register

FEATURES

- Shift left and shift right capability
- Synchronous Parallel and Serial data transfers
- Easily expanded for both Serial and Parallel operation
- Asynchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11194 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11194 4-bit Bidirectional Universal Shift Register is fully synchronous, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{MR}$ = High)	C_L = 50pF	4.2	6.2	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	66	69	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	130	130	MHz

Note:

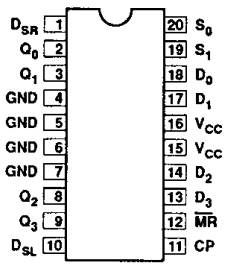
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

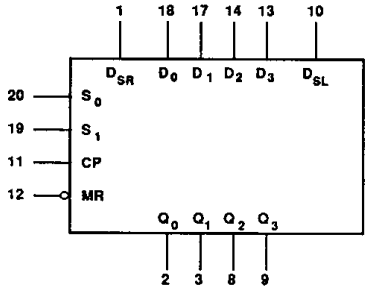
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11194N 74ACT11194N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11194D 74ACT11194D

PIN CONFIGURATION

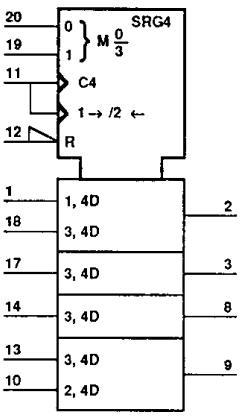
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4-bit bidirectional universal shift register

74AC/ACT11194

The 74AC/ACT11194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Function Table, data can be entered and shifted from left to right (shift right, Q_0 Æ Q_1, etc.), or right to left (shift left, Q_3 Æ Q_2, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data input (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

The only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select (S_0, S_1), Parallel Data (D_0 - D_3) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge are observed.

The four Parallel Data inputs (D_0 - D_3) are D-type inputs. Data appearing on D_0 - D_3 inputs when S_0 and S_1 are High is transferred to the Q_0 - Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	$\overline{MR}$	Asynchronous master reset (active Low)
11	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
1	D_{SR}	Serial data input (shift right)
10	D_{SL}	Serial data input (shift left)
20, 19	S_0, S_1	Mode control inputs
2, 3, 8, 9	Q_0 - Q_3	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

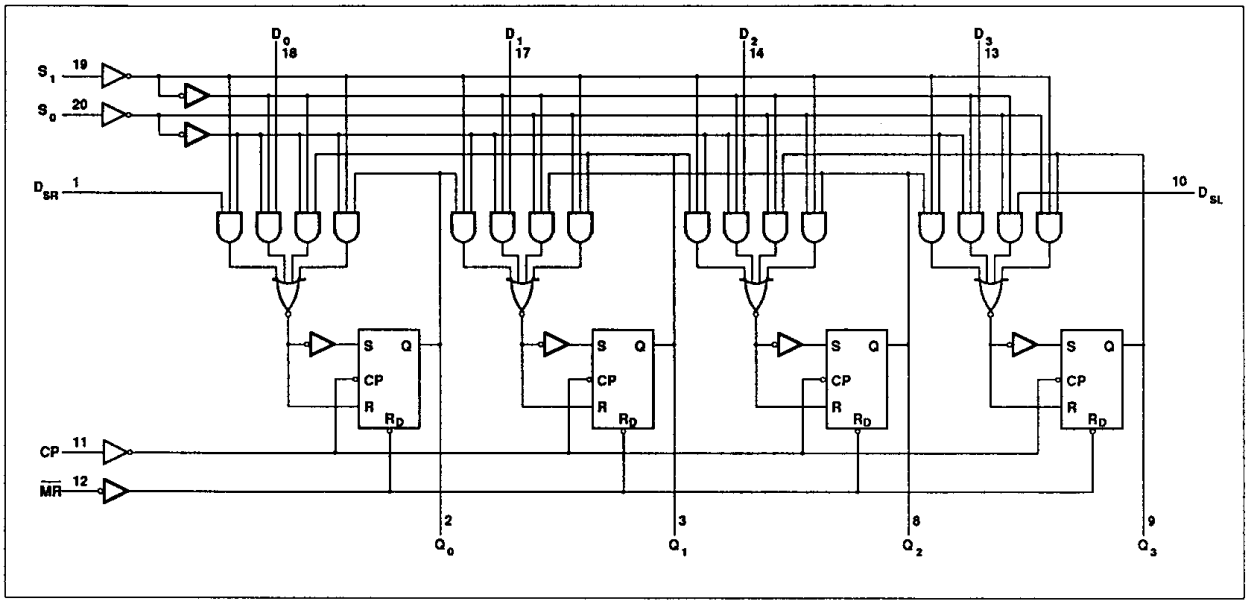
OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	dn	d_0	d_1	d_2	d_3

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
d_n (q_n) = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

4-bit bidirectional universal shift register

74AC/ACT11194

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11194			74ACT11194			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11194				74ACT11194				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

4-bit bidirectional universal shift register | 74AC/ACT11194

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.0 1.0	5.8 6.6	8.4 8.9	1.0 1.0	9.5 10.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.7	7.1	9.5	1.7	10.7	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	0.5			0.5		ns
t_S	Setup time, High or Low S_n to CP	3	5.0			5.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	5.5			5.5		ns
t_W	Clock pulse width (count) High or Low	1	5.5			5.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

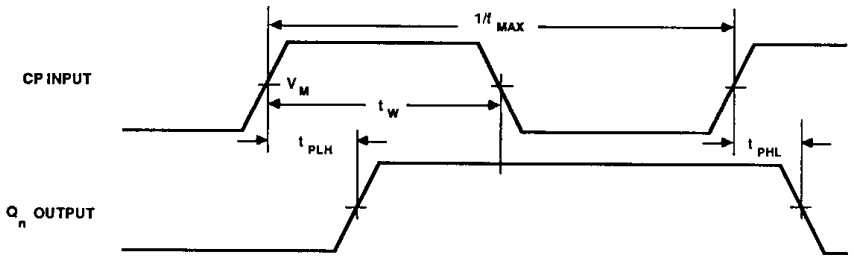
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	0.8 1.1	3.9 4.4	6.2 6.6	0.8 1.1	6.8 7.7	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	4.6	7.0	1.5	7.8	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	2.5			2.5		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

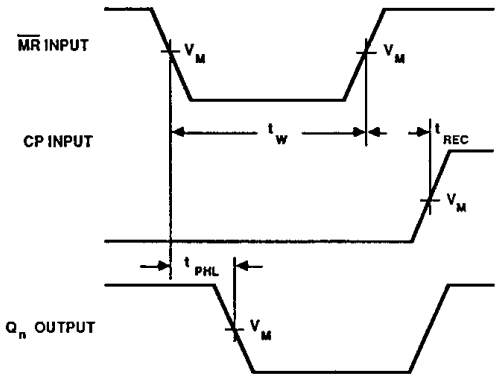
SYMBOL	PARAMETER	WAVEFORM	74ACT11194					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	2.2 2.6	5.8 6.6	6.9 7.7	2.2 2.6	7.7 8.8	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	2.9	7.1	9.1	2.9	10.3	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC WAVEFORMS

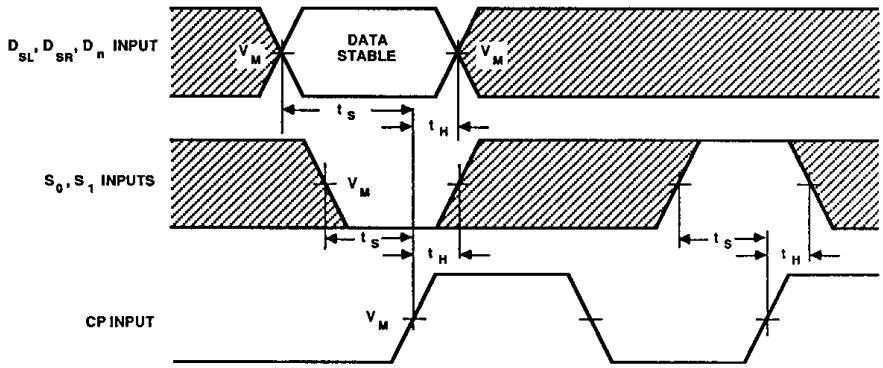


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Q_n) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

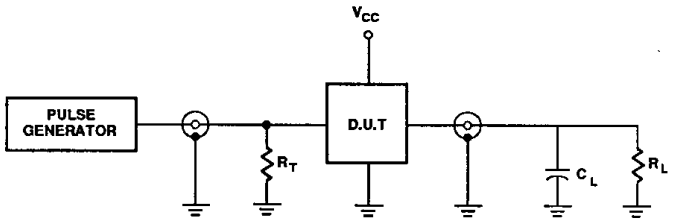


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n, D_{SL}, D_{SR}) and for S_0 and S_1 Inputs

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns