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ACL Products	

74AC/ACT11251

8-input multiplexer (3-State)

FEATURES

- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11251 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11251 provides an 8-to-1 multiplexer with three select lines and a common output enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The Output Enable (\overline{OE}) input is active-Low. When \overline{OE} is High, both the Y output and the \overline{Y} output are in the High-impedance "OFF" state regardless of all other input conditions.

The device is the logic implementation of a single pole, 8 position switch where the position of the switch is determined

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$		TYPICAL		UNIT
				AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay I_n to Y	$C_L = 50\text{pF}$		3.9	5.5	ns
C_{PD}	Power dissipation capacitance ¹	$f = 1\text{MHz};$	Enabled	55	60	pF
		$C_L = 50\text{pF}$	Disabled	13	16	
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}		3.5	3.5	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or $V_{CC};$ Disabled		8.0	8.0	pF

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

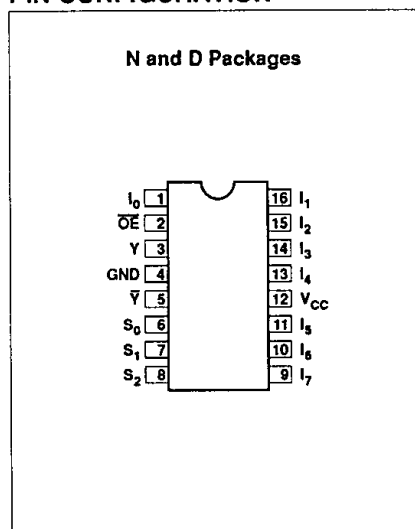
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

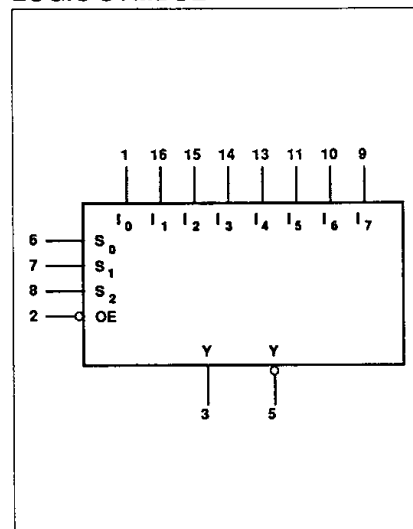
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11251N 74ACT11251N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11251D 74ACT11251D

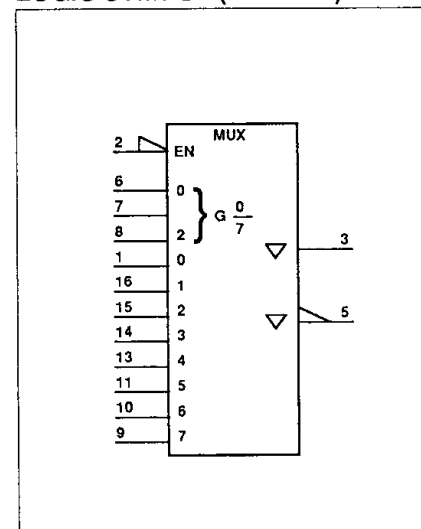
PIN CONFIGURATION



LOGIC SYMBOL



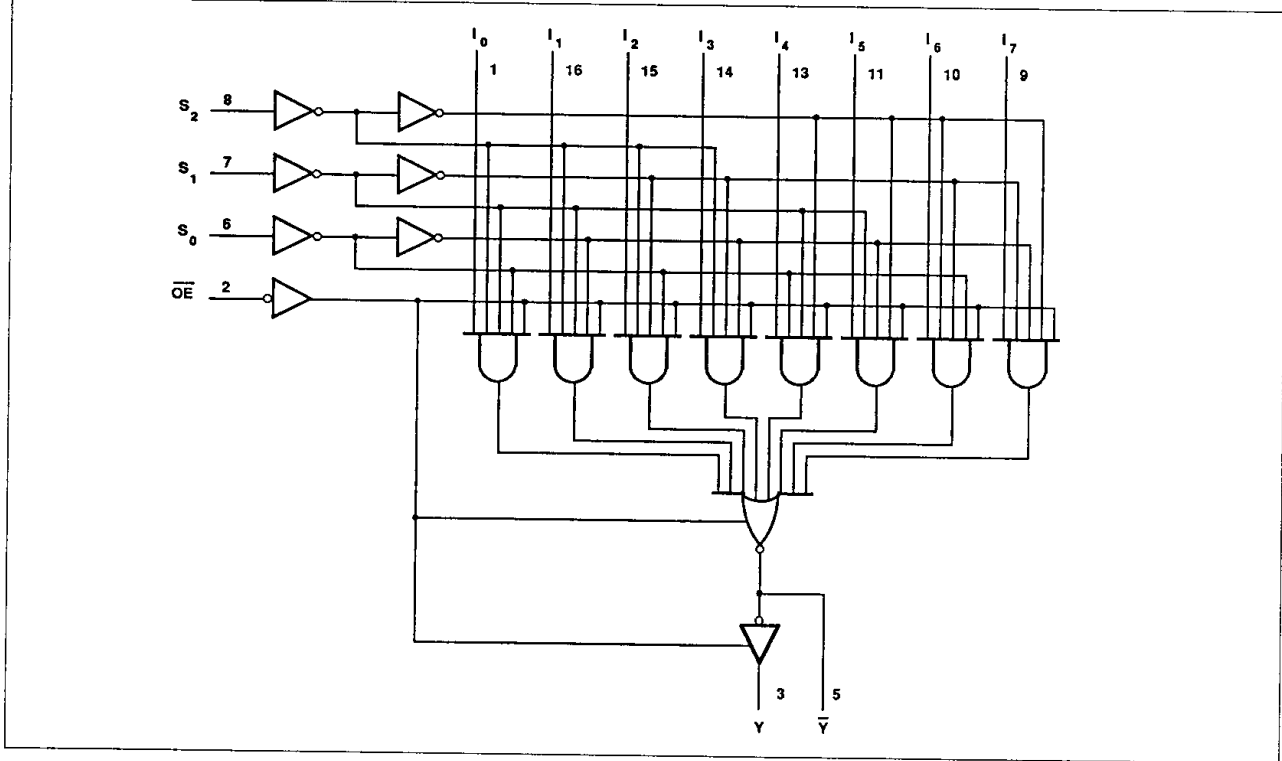
LOGIC SYMBOL (IEEE/IEC)



8-input multiplexer (3-State)

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LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
6, 7, 8	S_n	Select inputs
2	\overline{OE}	Output enable input
1, 16, 15, 14 13, 11, 10, 9	$I_0 - I_7$	Data inputs
3, 5	Y, \overline{Y}	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	\overline{OE}	Y	\overline{Y}
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I_0}$
L	L	H	L	I_1	$\overline{I_1}$
L	H	L	L	I_2	$\overline{I_2}$
L	H	H	L	I_3	$\overline{I_3}$
H	L	L	L	I_4	$\overline{I_4}$
H	L	H	L	I_5	$\overline{I_5}$
H	H	L	L	I_6	$\overline{I_6}$
H	H	H	L	I_7	$\overline{I_7}$

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11251			74ACT11251			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} current		± 100	mA
	DC ground current		± 100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11251				74ACT11251				UNIT	
				T _{amb} = +25°C		T _{amb} = -40°C to +85°C		T _{amb} = +25°C		T _{amb} = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
			I _{OH} = -4mA	5.5	5.4		5.4		5.4		5.4		
				3.0	2.58		2.48						
			I _{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	5.5		0.1		0.1		0.1			0.1
				3.0		0.36		0.44					
			I _{OL} = 24mA	4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I _{OL} = 75mA ¹	3.0				1.65				1.65				
	5.5				1.65				1.65				
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		5.0		±0.5		5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n to Y	1	2.2 2.0	6.3 6.1	8.2 8.0	2.2 2.0	9.0 8.8	ns
t _{PLH} t _{PHL}	Propagation delay I _n to \bar{Y}	1	1.7 2.1	5.7 6.3	7.5 8.2	1.7 2.1	8.2 9.1	ns
t _{PLH} t _{PHL}	Propagation delay S _n to Y	1	2.6 2.8	8.1 8.3	10.8 10.8	2.6 2.8	12.1 11.9	ns
t _{PLH} t _{PHL}	Propagation delay S _n to \bar{Y}	1	2.6 2.5	7.9 8.0	10.2 10.8	2.6 2.5	11.3 12.1	ns
t _{PZH} t _{PZL}	Propagation delay \overline{OE} to Y	2	1.3 1.6	4.1 4.9	5.7 6.6	1.3 1.6	6.1 7.2	ns
t _{PZH} t _{PZL}	Propagation delay \overline{OE} to \bar{Y}	2	1.2 1.5	4.0 4.8	5.5 6.5	1.2 1.5	5.9 7.1	ns
t _{PHZ} t _{PLZ}	Propagation delay \overline{OE} to Y	2	2.9 2.7	4.5 4.7	5.9 6.3	2.9 2.7	6.1 6.6	ns
t _{PHZ} t _{PLZ}	Propagation delay \overline{OE} to \bar{Y}	2	2.9 2.8	4.5 4.7	5.9 6.3	2.9 2.8	6.2 6.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n to Y	1	1.8 1.7	4.0 3.8	5.9 5.7	1.8 1.7	6.5 6.3	ns
t _{PLH} t _{PHL}	Propagation delay I _n to \bar{Y}	1	1.4 1.7	3.5 4.1	5.4 5.9	1.4 1.7	5.8 6.6	ns
t _{PLH} t _{PHL}	Propagation delay S _n to Y	1	2.2 2.4	5.3 5.0	7.5 7.5	2.2 2.4	8.3 8.4	ns
t _{PLH} t _{PHL}	Propagation delay S _n to \bar{Y}	1	2.1 2.2	4.7 5.4	7.1 7.5	2.1 2.2	7.9 8.5	ns
t _{PZH} t _{PZL}	Propagation delay \overline{OE} to Y	2	1.0 1.3	2.7 3.1	4.4 4.8	1.0 1.3	4.7 5.2	ns
t _{PZH} t _{PZL}	Propagation delay \overline{OE} to \bar{Y}	2	1.0 1.2	2.6 3.0	4.3 4.7	1.0 1.2	4.6 5.1	ns
t _{PHZ} t _{PLZ}	Propagation delay \overline{OE} to Y	2	2.8 2.6	4.2 4.2	5.6 5.7	2.8 2.6	5.9 6.0	ns
t _{PHZ} t _{PLZ}	Propagation delay \overline{OE} to \bar{Y}	2	2.8 2.7	4.3 4.2	5.7 5.7	2.8 2.7	6.0 5.9	ns

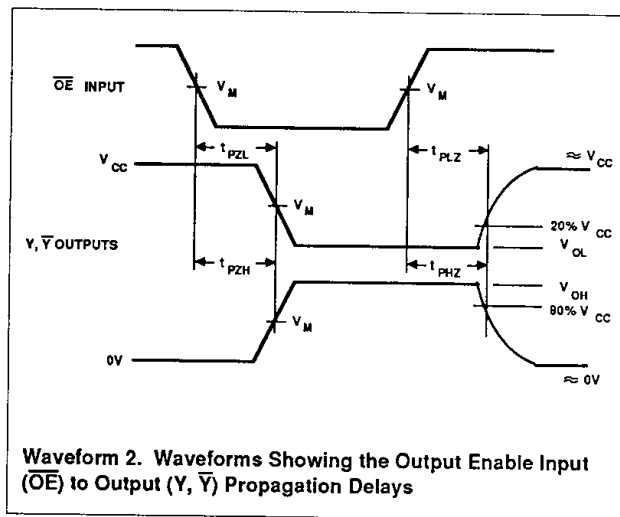
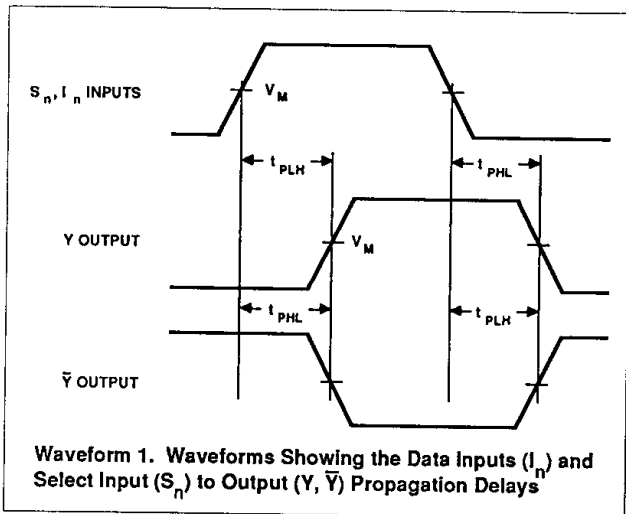
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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11251					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n to Y	1	3.0 2.0	5.7 5.2	7.8 7.9	3.0 2.0	8.7 8.6	ns
t _{PLH} t _{PHL}	Propagation delay I _n to \bar{Y}	1	1.7 2.7	4.7 5.1	7.1 7.2	1.7 2.7	7.8 8.0	ns
t _{PLH} t _{PHL}	Propagation delay S _n to Y	1	3.2 2.7	6.8 6.7	10.2 9.5	3.2 2.7	11.4 10.5	ns
t _{PLH} t _{PHL}	Propagation delay S _n to \bar{Y}	1	2.5 2.8	6.3 6.3	8.8 9.7	2.5 2.8	9.8 10.8	ns
t _{PZH} t _{PZL}	Propagation delay \overline{OE} to Y	2	1.3 1.3	3.7 4.0	6.2 6.0	1.3 1.3	6.8 6.8	ns
t _{PZH} t _{PZL}	Propagation delay \overline{OE} to \bar{Y}	2	1.0 1.3	4.4 4.1	6.4 5.8	1.0 1.3	7.0 6.4	ns
t _{PHZ} t _{PLZ}	Propagation delay \overline{OE} to Y	2	4.1 3.1	5.7 4.0	7.6 6.6	4.1 3.1	8.1 6.9	ns
t _{PHZ} t _{PLZ}	Propagation delay \overline{OE} to \bar{Y}	2	4.1 3.2	5.7 4.1	7.7 6.6	4.1 3.2	8.2 6.9	ns

AC WAVEFORMS



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WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$, $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$, $V_M = 1.5V$	$V_M = 50\% V_{CC}$

TEST CIRCUIT

Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: $PRR \leq 10\text{MHz}$

$t_r = t_f = 3\text{ns}$