

Document No.	853-1498
ECN No.	00731
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

# 74AC/ACT11379

## Quad D-type flip-flop with data enable

### FEATURES

- Output capability:  $\pm 24$  mA
- Edge-triggered D-type inputs
- Positive edge-triggered clock
- Common asynchronous Enable ( $\bar{E}$ ) input
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

### DESCRIPTION

The 74AC/ACT11379 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11379 provides four edge-triggered D-type flip-flops with individual Data inputs ( $D_0 - D_3$ ) and Q and  $\bar{Q}$  outputs. The flip-flops load the data on the rising edge of the common clock (CP) providing that the common Enable ( $\bar{E}$ ) is held Low. When the Enable is High, the flip-flops hold their previous state.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay CP to $Q_n$ or $\bar{Q}_n$	$C_L = 50\text{pF}$	5.3	6.1	ns
$C_{PD}$	Power dissipation capacitance per flip-flop <sup>1</sup>	$f = 1\text{MHz}; C_L = 50\text{pF}$	38	38	pF
$C_{IN}$	Input capacitance	$V_I = 0\text{V or } V_{CC}$	4.0	4.0	pF
$I_{LATCH}$	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
$f_{MAX}$	Maximum clock frequency	$C_L = 50\text{pF}$	130	125	MHz

**Note:**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

$f_I$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

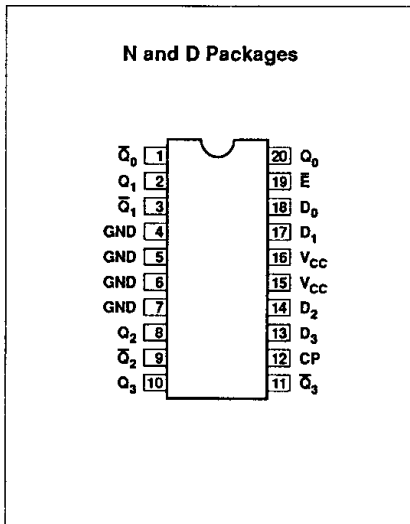
$f_O$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$  = sum of outputs

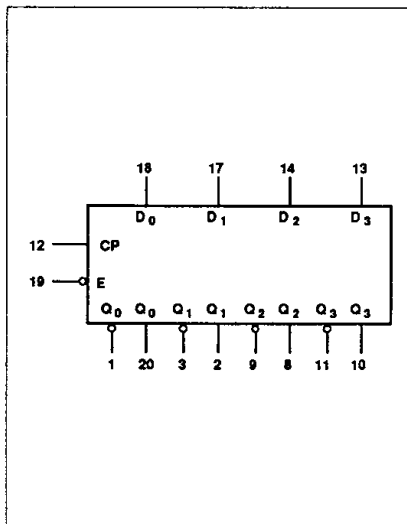
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11379N 74ACT11379N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11379D 74ACT11379D

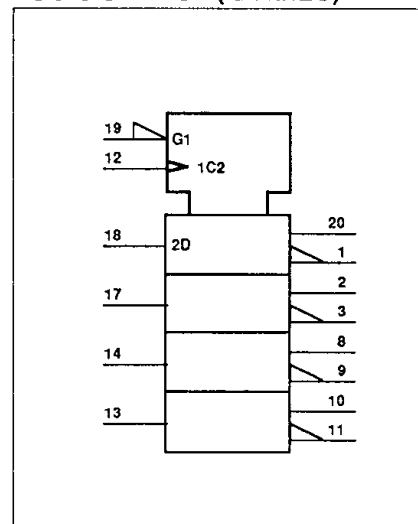
### PIN CONFIGURATION



### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



# Quad D-type flip-flop with data enable

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## PIN DESCRIPTION

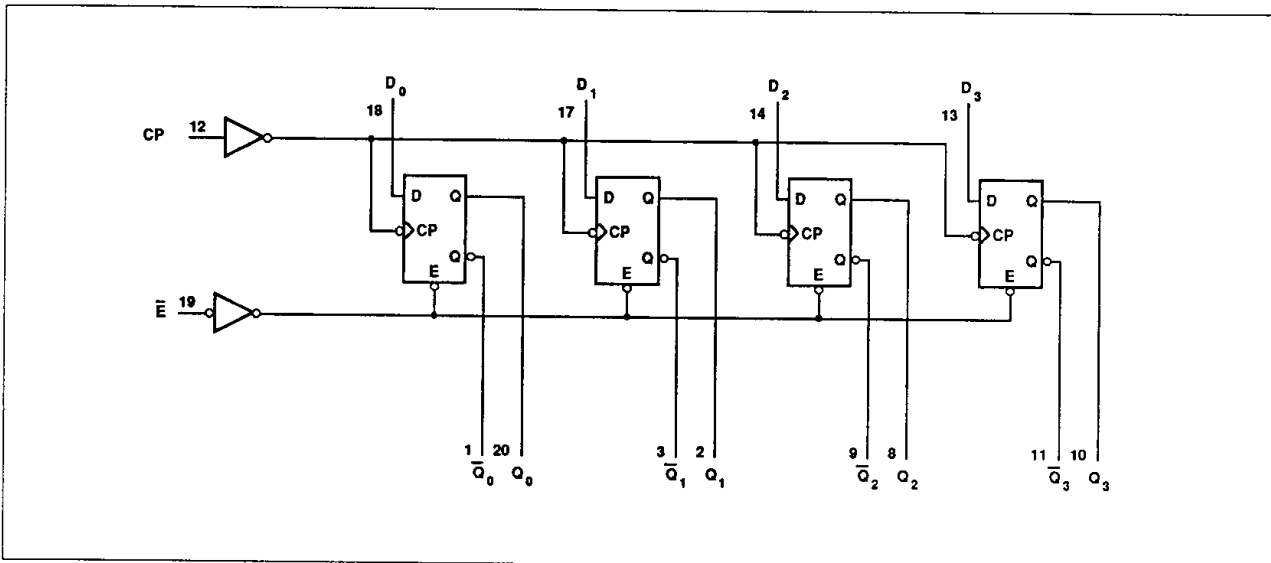
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	$D_0 - D_3$	Data inputs
20, 2, 8, 10	$Q_0 - Q_3$	Data outputs
1, 3, 9, 11	$\bar{Q}_0 - \bar{Q}_3$	Data outputs (complements of $Q_n$ outputs)
19	$\bar{E}$	Data enable input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	$V_{CC}$	Positive supply voltage

## FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\bar{E}$	CP	$D_n$	$Q_n$	$\bar{Q}_n$
Disabled input (hold)	H	$\uparrow$	X	NC	NC
Load "1" (set)	L	$\uparrow$	h	H	L
Load "0" (reset)	L	$\uparrow$	l	L	H

H = High voltage level steady state  
 h = High voltage level one set-up time prior to the Low-to-High clock transition  
 L = Low voltage level steady state  
 l = Low voltage level one set-up time prior to the Low-to-High clock transition  
 X = Don't care  
 NC = No Change  
 $\uparrow$  = Low-to-High clock transition

## LOGIC DIAGRAM



## Quad D-type flip-flop with data enable

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11379			74ACT11379			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta V/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40		+85	-40		+85	°C

## NOTE:

- No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 TO +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		±200	mA
	DC ground current		±200	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Quad D-type flip-flop with data enable

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	74AC11379				74ACT11379				UNIT	
				T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C		T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
			I <sub>OH</sub> = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I <sub>OL</sub> = 24mA	4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I <sub>OL</sub> = 75mA <sup>1</sup>	5.5				1.65				1.65				
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

## NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

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## AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	90	115		90		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub> , $\overline{Q}_n$	1	1.8 3.0	6.7 9.5	8.4 13.0	1.8 3.0	9.9 14.0	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> to CP	1	7.5			7.5		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub>	1	0.0			0.0		ns
t <sub>S</sub>	Setup time, High or Low $\overline{E}$ to CP	1	4.5			4.5		ns
t <sub>H</sub>	Hold time, High or Low CP to $\overline{E}$	1	0.0			0.0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	5.5			5.5		ns

## AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	100	130		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub> , $\overline{Q}_n$	1	1.5 2.6	4.3 6.2	6.0 9.1	1.5 2.6	6.7 10.3	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> to CP	1	5.0			5.0		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub>	1	0.0			0.0		ns
t <sub>S</sub>	Setup time, High or Low $\overline{E}$ to CP	1	3.0			3.0		ns
t <sub>H</sub>	Hold time, High or Low CP to $\overline{E}$	1	0.0			0.0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	5.0			5.0		ns

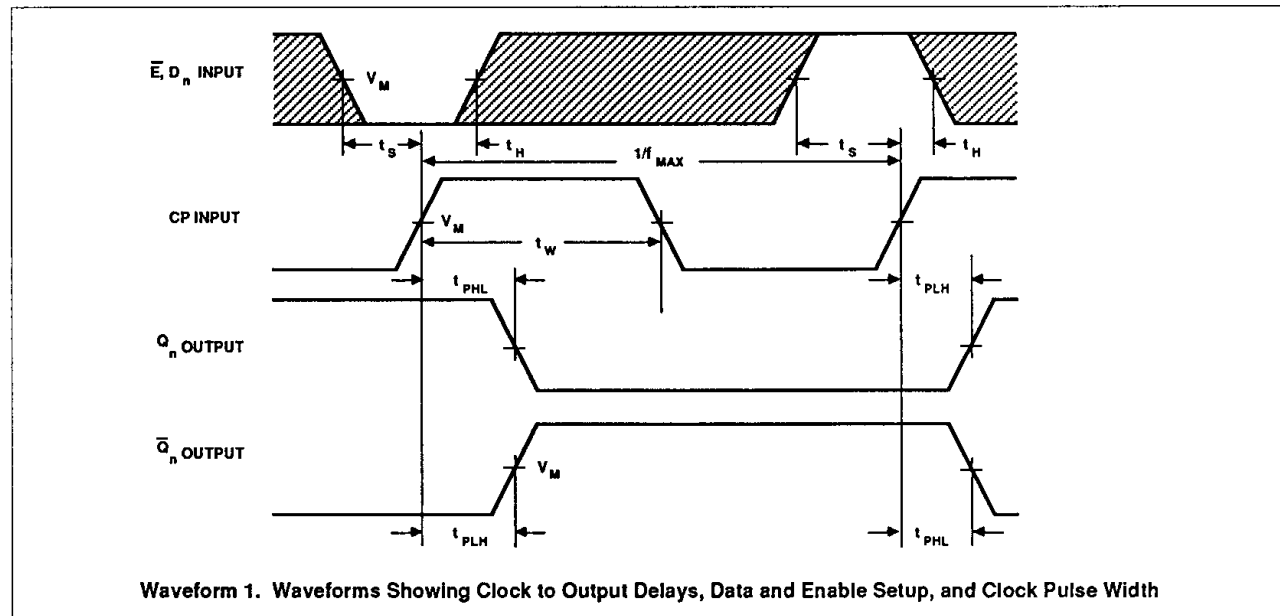
# Quad D-type flip-flop with data enable

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## AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

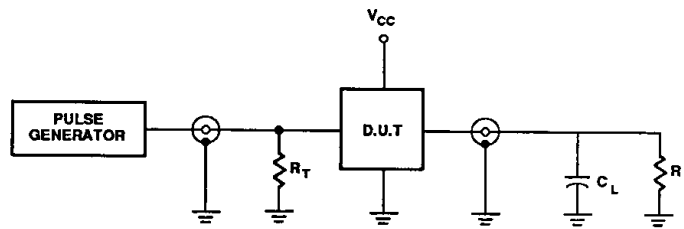
SYMBOL	PARAMETER	WAVEFORM	74ACT11379					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	100	125		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub> , $\bar{Q}_n$	1	2.2 3.1	5.0 7.2	6.6 9.8	2.2 3.1	7.4 11.2	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> to CP	1	5.0			5.0		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub>	1	0.0			0.0		ns
t <sub>S</sub>	Setup time, High or Low $\bar{E}$ to CP	1	3.5			3.5		ns
t <sub>H</sub>	Hold time, High or Low CP to $\bar{E}$	1	0.5			0.5		ns
t <sub>W</sub>	Clock pulse width High or Low	1	5.0			5.0		ns

## AC WAVEFORMS



## WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

**Quad D-type flip-flop with data enable****74AC/ACT11379****TEST CIRCUIT****Test Circuit****DEFINITIONS**

$C_L$  = Load capacitance, 50pF; includes jig  
and probe capacitance

$R_L$  = Load resistor, 500 $\Omega$

$R_T$  = Termination resistance should be  
equal to  $Z_{OUT}$  of pulse generators

Input pulses: PRR  $\leq$  10MHz

$t_r = t_f = 3$ ns

# Data Sheet Specification Guide

## ACL Products

### INTRODUCTION

The 74ACL data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

### TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of  $t_{PLH}$  and  $t_{PHL}$  for a typical data path through the device with a 50pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on  $t_R$  and  $t_F$ .

### LOGIC SYMBOLS

Two logic symbols are given for each device - the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEEE/IEC Logic Symbol.

The IEEE/IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic.

### ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table lists the maximum limits to which the device can be subjected without damage. This does not imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life will not have been shortened.

### RECOMMENDED OPERATING CONDITIONS

The "Recommended Operating Conditions" table lists the operating ambient temperature and the conditions under which the limits in the "DC Characteristics" and "AC Characteristics" table will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC Characteristics tables.

### TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground plate) should be used for the same reasons. A  $V_{CC}$  decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 3ns, a signal swing of 0V to  $V_{CC}$  for 74AC and 0V to 3V for 74ACT; a 5MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing  $f_{MAX}$ . Two pulse generators are usually required for testing such parameters as setup time, hold time and removal time.  $f_{MAX}$  is also tested with 3ns input rise and fall times, with a 50% duty factor, but for typical  $f_{MAX}$  as high as 150MHz, there are no constraints on rise and fall times.

### DC CHARACTERISTICS

The "DC Characteristics" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of  $V_{IH}$  and  $V_{IL}$  are applied to the inputs, the output voltages will be those published in the "DC

Characteristics" table. There is a tendency, by some, to use the published  $V_{IH}$  and  $V_{IL}$  thresholds to test a device for functionality in a "function-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 meter. Parametric tests, such as those used for the output levels under the  $V_{IH}$  and  $V_{IL}$  conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use  $V_{IH}$  and  $V_{IL}$  to test the functionality of any ACL device type; instead, use input voltages of  $V_{CC}$  (for the High state) and 0V (for the Low state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical  $V_{IL}$  is higher than the maximum  $V_{IL}$ . However, this is because  $V_{ILMAX}$  is the maximum  $V_{IL}$  (guaranteed) for all devices that will be recognized as a logic Low. However, typically a higher  $V_{IL}$  will also be recognized as a logic Low. Conversely, the typical  $V_{IH}$  is lower than its minimum guaranteed level.

The quiescent supply current  $I_{CC}$  is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors.

### AC CHARACTERISTICS

The "AC Characteristics" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveform section.