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74AC/ACT11874

Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

FEATURES

- 3-State output buffers
- Asynchronous clear
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11874 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11874 devices are dual 4-bit D-type edge-triggered flip-flops with asynchronous resets, making them suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The edge-triggered flip-flops enter data on the low-to-high transition of the clock. All four Q outputs will be forced low, in-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay nCP to Q_n	C_L = 50pF		5.6	7.2	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	31	35	pF
			Disabled	13	17	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		13.5	13.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V		140	140	MHz

Note:

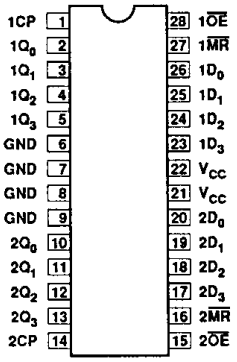
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

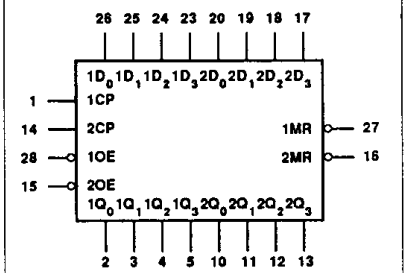
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11874N 74ACT11874N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11874D 74ACT11874D

PIN CONFIGURATION

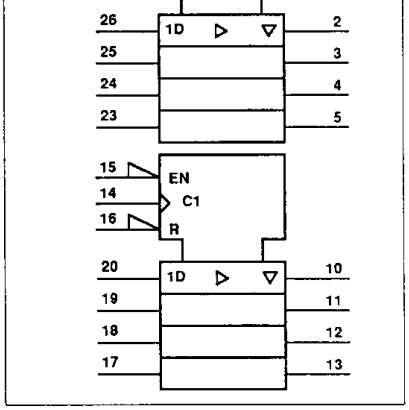
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

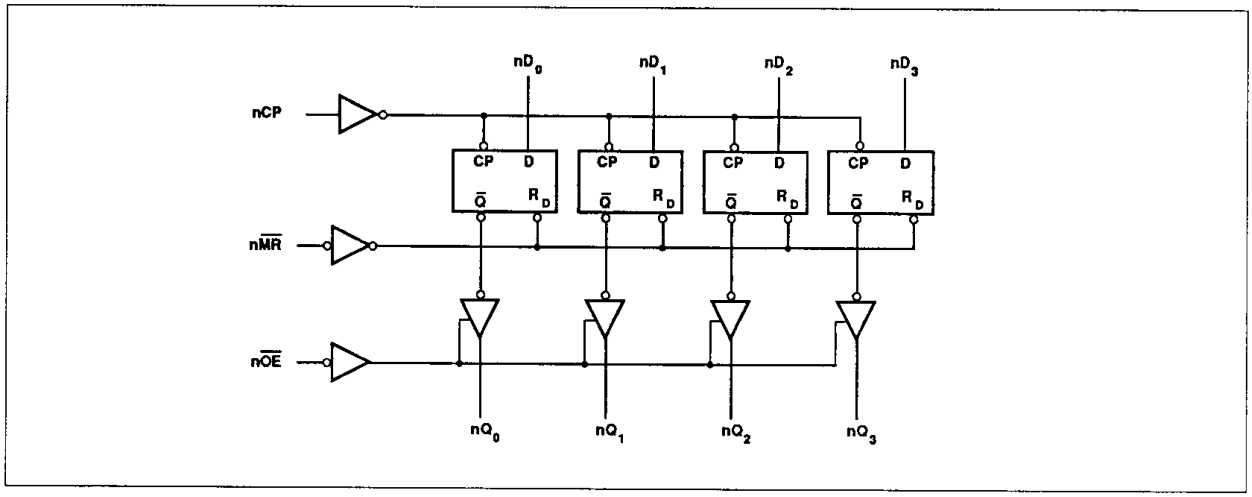
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$1\overline{OE}$, $2\overline{OE}$	Output enables
26, 25, 24, 23, 20, 19, 18, 17	$1D_0$ - $1D_3$, $2D_0$ - $2D_3$	Data inputs
2, 3, 4, 5, 10, 11, 12, 13	$1Q_0$ - $1Q_3$, $2Q_0$ - $2Q_3$	Data outputs
1, 14	1CP, 2CP	Clock inputs
27, 16	$1\overline{MR}$, $2\overline{MR}$	Master reset inputs
6, 7, 8, 9	GND	Ground (0V)
22, 21	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{MR}$	$n\overline{OE}$	nCP	nD_n	nQ_n
Reset (clear)	L	L	X	X	L
Load flip-flop	H H	L L	↑ ↑	l h	L H
Disable outputs	X	H	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance "OFF" state
↑ = Low-to-High transition

LOGIC DIAGRAM



dependent of clock or data inputs, by taking $\overline{MR}$ Low.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (OE) controls all eight 3-State buffers independent of the latch operation.

When the $\overline{OE}$ inputs are Low, the latched or transparent data appears at the outputs. When the $\overline{OE}$ inputs are high, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11874			74ACT11874			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11874				74ACT11874				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.0V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11874					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	60	80		60		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQ_n	1	2.9 3.7	7.3 8.8	11.0 13.1	2.9 3.7	12.5 14.6	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	4	3.9	9.3	14.0	3.9	15.7	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	2	2.1 3.1	5.6 8.4	8.7 13.1	2.1 3.1	9.8 14.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	2	4.0 3.9	6.2 6.3	8.2 8.5	4.0 3.9	8.7 9.0	ns
t_W	Clock pulse width High or Low	1	8.3			8.3		ns
t_W	$n\overline{MR}$ pulse width Low	4	4.0			4.0		ns
t_S	Setup time nD_n to nCP	3	3.0			3.0		ns
t_H	Hold time nD_n to nCP	3	1.0			1.0		ns
t_{rec}	Recovery time $n\overline{MR}$ to nCP	4	1.5			1.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11874					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	140		125		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQ_n	1	2.3 2.9	5.2 6.1	7.4 8.6	2.3 2.9	8.3 9.6	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	4	2.9	6.3	8.9	2.9	10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	2	1.5 2.3	4.0 5.4	5.9 7.8	1.5 2.3	6.6 8.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	2	3.8 3.7	5.7 5.5	7.3 7.1	3.8 3.7	7.7 7.5	ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{MR}$ pulse width Low	4	4.0			4.0		ns
t_S	Setup time nD_n to nCP	3	2.0			2.0		ns
t_H	Hold time nD_n to nCP	3	1.0			1.0		ns
t_{rec}	Recovery time $n\overline{MR}$ to nCP	4	1.5			1.5		ns

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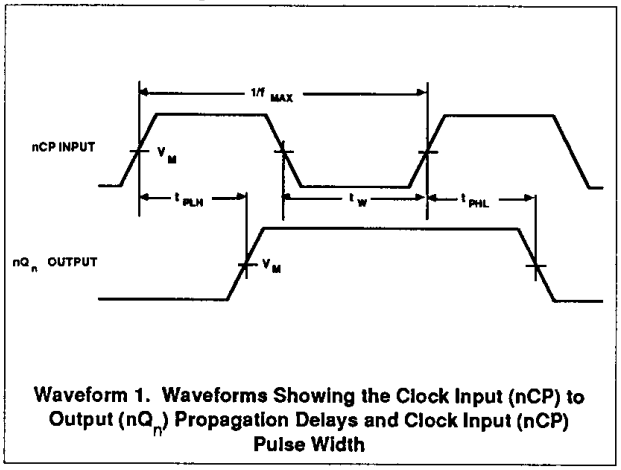
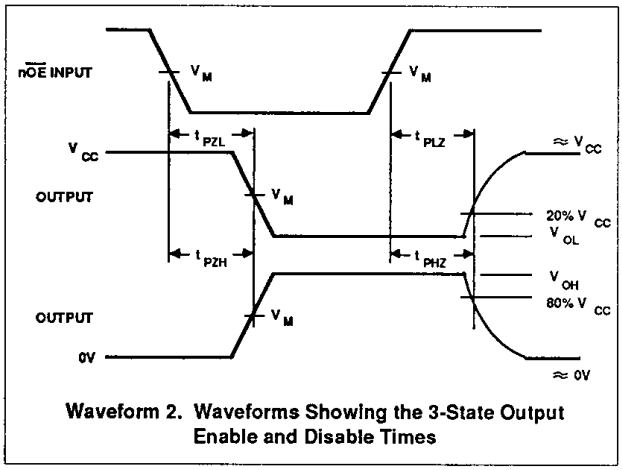
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11874					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	140		125		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQ_n	1	3.7 4.1	6.6 7.8	8.4 9.5	3.7 4.1	9.4 10.6	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	4	3.5	7.8	10.5	3.5	11.8	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	2	1.6 2.4	4.6 6.0	6.7 8.6	1.6 2.4	7.4 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	2	5.4 4.9	7.4 7.1	8.9 8.5	5.4 4.9	9.4 9.1	ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{MR}$ pulse width Low	4	4.0			4.0		ns
t_S	Setup time nD_n to nCP	3	5.0			5.0		ns
t_H	Hold time nD_n to nCP	3	1.0			1.0		ns
t_{rec}	Recovery time $n\overline{MR}$ to nCP	4	2.0			2.0		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Clock Input (nCP) to Output (nQ_n) Propagation Delays and Clock Input (nCP) Pulse Width



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

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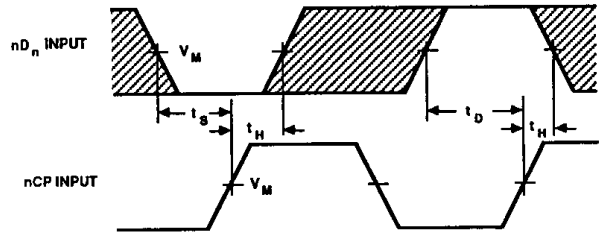
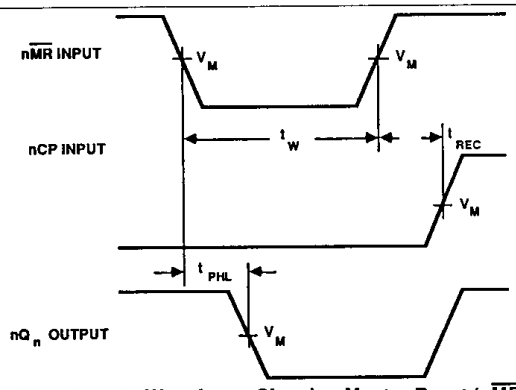
WAVEFORMS (continued)



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for nD_n Input to nCP Input

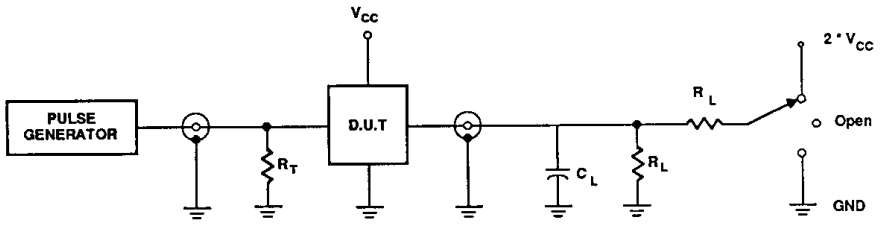


Waveform 4. Waveforms Showing Master Reset ($\overline{nMR}$) Pulse Width, Master Reset to Output Delay and Master Reset to Clock (nCP) Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns