T1 TRANSCEIVER

FEATURES

- Monolithic single chip device which integrates a full featured T1 framer with an on-chip analog line interface.
- Supports SF, ESF, T1DM (DDS) and SLC®96 format DS1 signals. Supports unframed mode. Supports B8ZS or AMI line codes.
- Recovers clock and data from the incoming DSX-1 signal, generates DSX-1 output signal.
- Supports transfer of PCM and signalling to/from 1.544 Mbit/s and 2.048 Mbit/s backplane buses. Supports gapped data streams used in higher rate multiplexing.
- Provides robbed bit signalling insertion/extraction, idle code substitution, digital milliwatt code substitution, data inversion and 2 superframes of signalling debounce on a per channel basis.
- Pin compatible with the PM6341 E1XC E1 Transceiver.
- Software compatible with the PM4344 TQUAD Quad T1 Framer and PM4388 TOCTL Octal T1 Framer.
- Provides an 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Low-power 5V CMOS technology.
- Avalable in a high density 80-pin (14 by14mm) PQFP or in a 68-pin PLCC package.

APPLICATIONS

- T1 & T3 Multiplexers
- T1 Frame Relay Interfaces
- T1 ATM UNI Interfaces
- Fractional T1
- T1 Channel Service Units (CSUs) and Data Service Units (DSUs)
- Digital Access and Cross-Connect Systems (DACS) and Electronic Digital Cross-Connects (EDSX)
- Digital Loop Carriers (DLCs)
- SONET Add-Drop Multiplexers (ADM)
- ISDN Primary Rate Interfaces (PRI)
- Digital Private Branch Exchanges (PBX)
- T1 & T3 Test Equipment

SLC®96 is a registered trademark of AT&T

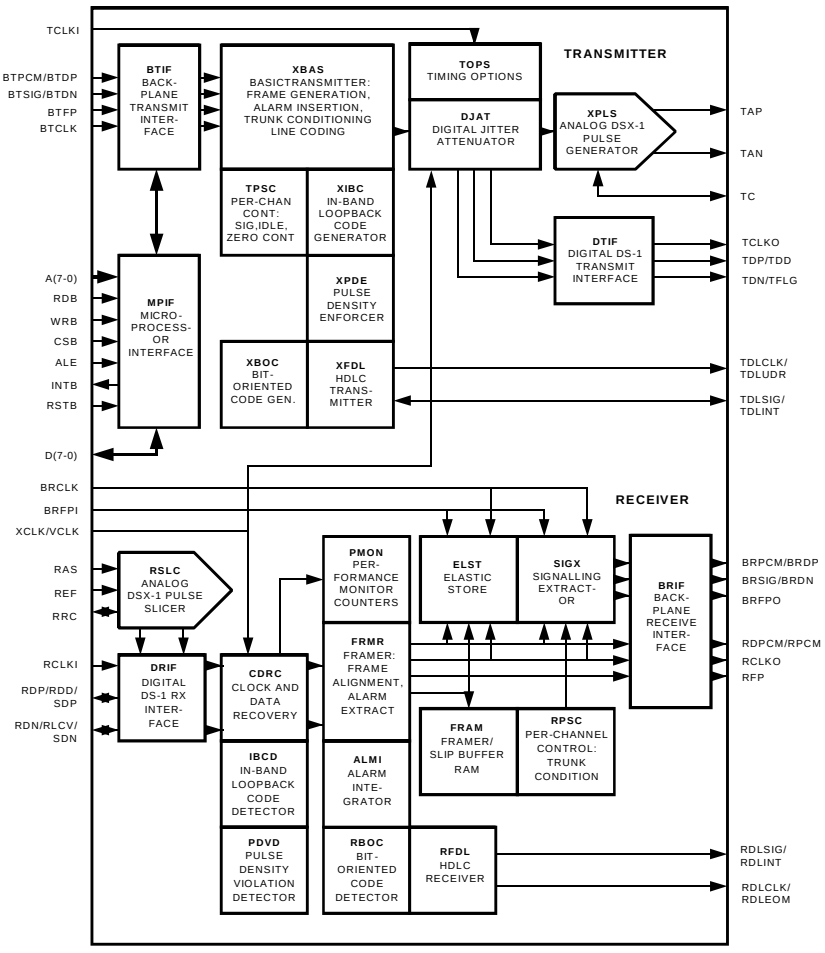
RECEIVE SECTION

- Provides loss of signal, red alarm, yellow alarm and AIS alarm indication. Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window.
- Supports line and path performance monitoring per Bellcore, AT&T and ANSI recommendations.
- Accumulators are provided for ESF CRC-6 and framing bit errors, Line Code Violations and Loss Of Frame or Change Of Frame Alignment events.
- Extracts the data link in ESF, T1DM and SLC®96 formats. Extracts the D-channel for primary rate interfaces.
- Provides ESF bit-oriented code detection and an HDLC interface for terminating the ESF datalink.
- Provides a 2 frame elastic store for jitter and wander attenuation.
- Detects programmable in-band loopback codes.

TRANSMIT SECTION

- Provides per channel minimum ones density through Bell (Bit 7), GTE or DDS zero code suppression.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window.
- Inserts the data link in ESF, T1DM and SLC®96 formats. Inserts the D-channel for primary rate interfaces.
- Generates AIS and yellow alarm in all formats.
- Inserts the data link in ESF, T1DM and SLC®96 formats. Inserts the D-channel for primary rate interfaces.
- Generates ESF bit-oriented codes and provides an HDLC interface for generating the ESF datalink.
- Inserts programmable in-band loopback codes.
- Provides a FIFO buffer for jitter attenuation and rate conversion.

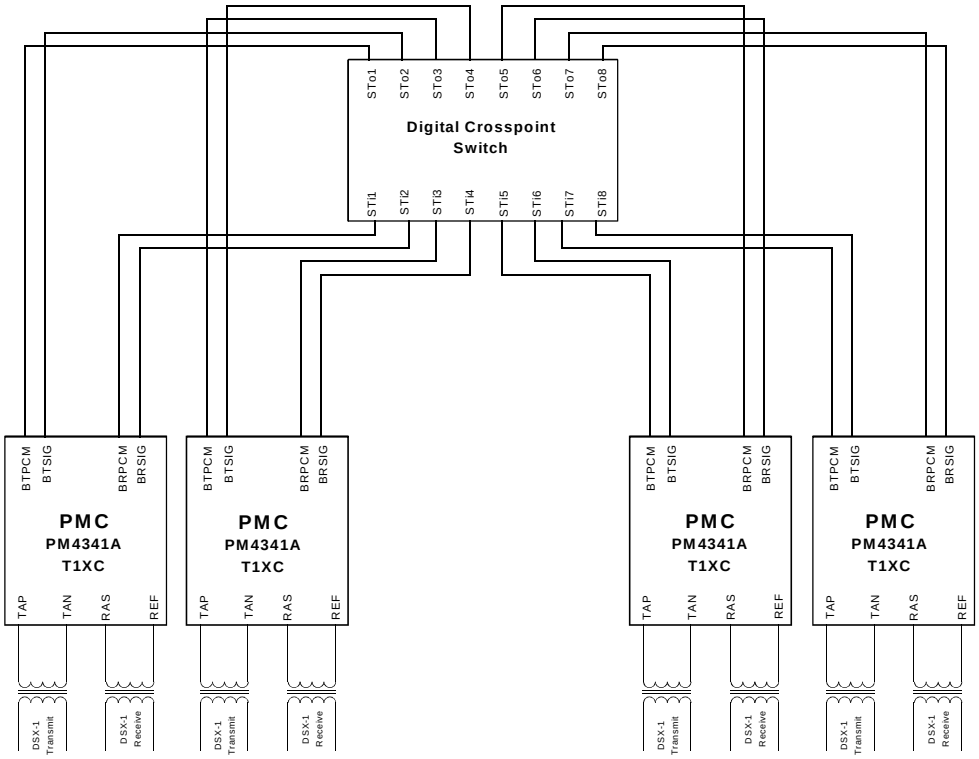
BLOCK DIAGRAM



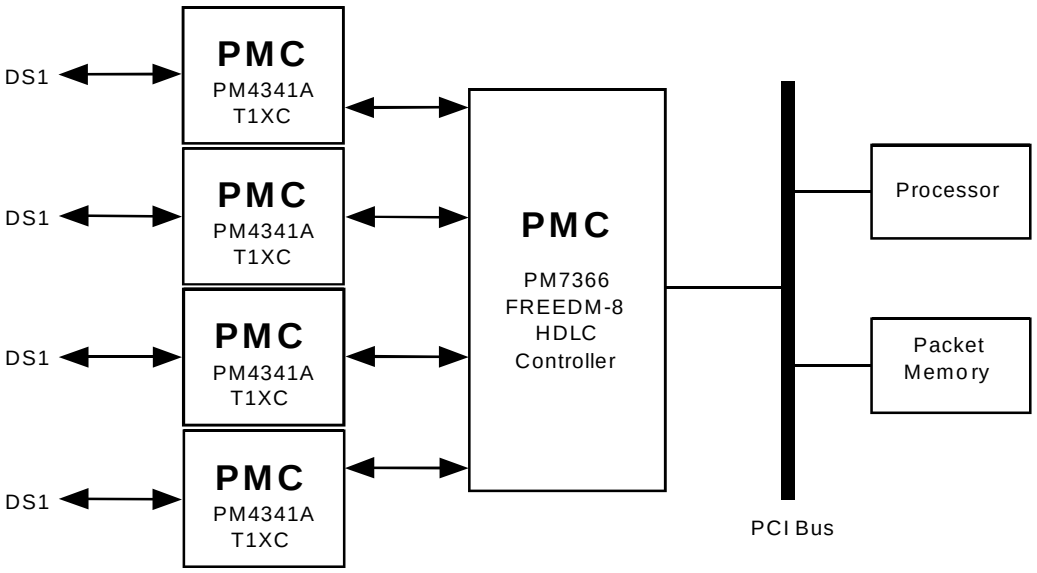
T1 TRANSCEIVER

TYPICAL APPLICATIONS:

1/0 CROSS-CONNECT WITH DSX-1 INTERFACE:



FULLY CHANNELIZED QUAD DS1 HDLC CARD:



Head Office:
PMC-Sierra, Inc.
Suite 105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation, send email to:
document@pmc-sierra.com
or contact the head office,
Attn:Document Coordinator

All product documentation is available on our web site at:
http://www.pmc-sierra.com
For corporate information, send email to:
info@pmc-sierra.com

PMC-920108(R7)