PM4388

TOCTL

OCTAL T1 FRAMER

DATASHEET

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1 FEATURES

- Integrates eight T1 framers in a single device for terminating duplex DS-1 signals.
- Supports SF and ESF format DS-1 signals.
- Supports transfer of PCM data to/from 1.544 MHz system-side devices. Also supports a fractional T1 system interface with independent ingress/egress NxDS0 rates. Supports a 2.048 MHz system-side interface without external clock gapping.
- Provides jitter attenuation in the receive and transmit directions.
- Provides per-DS0 line loopback and per link diagnostic and line loopbacks.
- Provides an integral pattern generator/detector that may be programmed to generate and detect common pseudo-random or repetitive sequences. The programmed sequence may be inserted/detected in the entire DS-1 frame, or on an NxDS0 basis, in both the ingress and egress directions. May be configured to transmit or detect in only the 7 most significant bits of selected channels, in order to support fractional T1 loopback codes in an N x 56kbps fractional T1 setup. Each framer possesses its own independent pattern generator/detector, and each detector counts pattern errors using a 32-bit saturating error counter.
- Provides robbed bit signaling extraction and insertion on a per-DS0 basis.
- Provides programmable idle code substitution, data and sign inversion, and digital milliwatt code insertion on a per-DS0 basis.
- Software compatible with the PM4341A T1XC Single T1 Transceiver and the PM4344 TQUAD Quad T1 Framer.
- Seamless interface to the PM8313 D3MX single chip M13 multiplex and to the PM4314 QDSX Quad Line Interface.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 3.3V CMOS technology with 5V tolerant inputs.
- Supports standard 5 signal P1149.1 JTAG boundary scan.

- Available in a 14 mm by 20 mm 128 pin Plastic Quad Flat Pack (PQFP) or an 11mm by 11mm 128 pin Chip Array Ball Grid Array (CABGA) package.

Each one of eight receiver sections:

- Accepts gapped data streams to support higher rate demultiplexing.
- Provides Red, Yellow, and AIS alarms integration.
- Provides programmable in-band loopback code detection.
- Indicates signaling state change, and 2 superframes of signaling debounce on a per-DS0 basis.
- Provides an HDLC interface with 128 bytes of buffering for terminating the facility data link.
- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.
- Provides an optional elastic store which may be used to time the ingress streams to a common clock and frame alignment, or to facilitate per-DS0 loopbacks.

Each one of eight transmitter sections:

- May be timed to its associated receive clock (loop timing) or may derive its timing from a common egress clock or a common transmit clock; the transmit line clock may be synthesized from an N*8kHz reference.
- Provides minimum ones density through Bell (bit 7), GTE or “jammed bit 8” zero code suppression on a per-DS0 basis.Provides a 128 byte buffer to allow insertion of the facility data link using the host interface.
- Supports transmission of the alarm indication signal (AIS) or the Yellow alarm signal in both SF and ESF formats.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter.

2 APPLICATIONS

- High density Internet T1 interfaces for multiplexers, switches, routers and digital modems.
- Frame Relay switches and access devices (FRADS)
- SONET/SDH Add Drop Multiplexers

3 REFERENCES

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3. American National Standard for Telecommunications - Carrier to Customer Installation - DS-1 Metallic Interface Specification, ANSI T1.403-1995

4. American National Standard for Telecommunications - Integrated Services Digital Network (ISDN) Primary Rate- Customer Installation Metallic Interfaces Layer 1 Specification, ANSI T1.408-1990

5. Bell Communications Research - DS-1 Rate Digital Service Monitoring Unit Functional Specification, TA-TSY-000147, Issue 1, October, 1987.

6. Bell Communications Research - Alarm Indication Signal Requirements and Objectives, TR-TSY-000191 Issue 1, May 1986.

7. Bell Communications Research - Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface, TR-NWT-000303, Issue 2, December, 1992.

8. Bell Communications Research - Functional Criteria for the DS-1 Interface Connector, TR-TSY-000312, Issue 1, March, 1988.

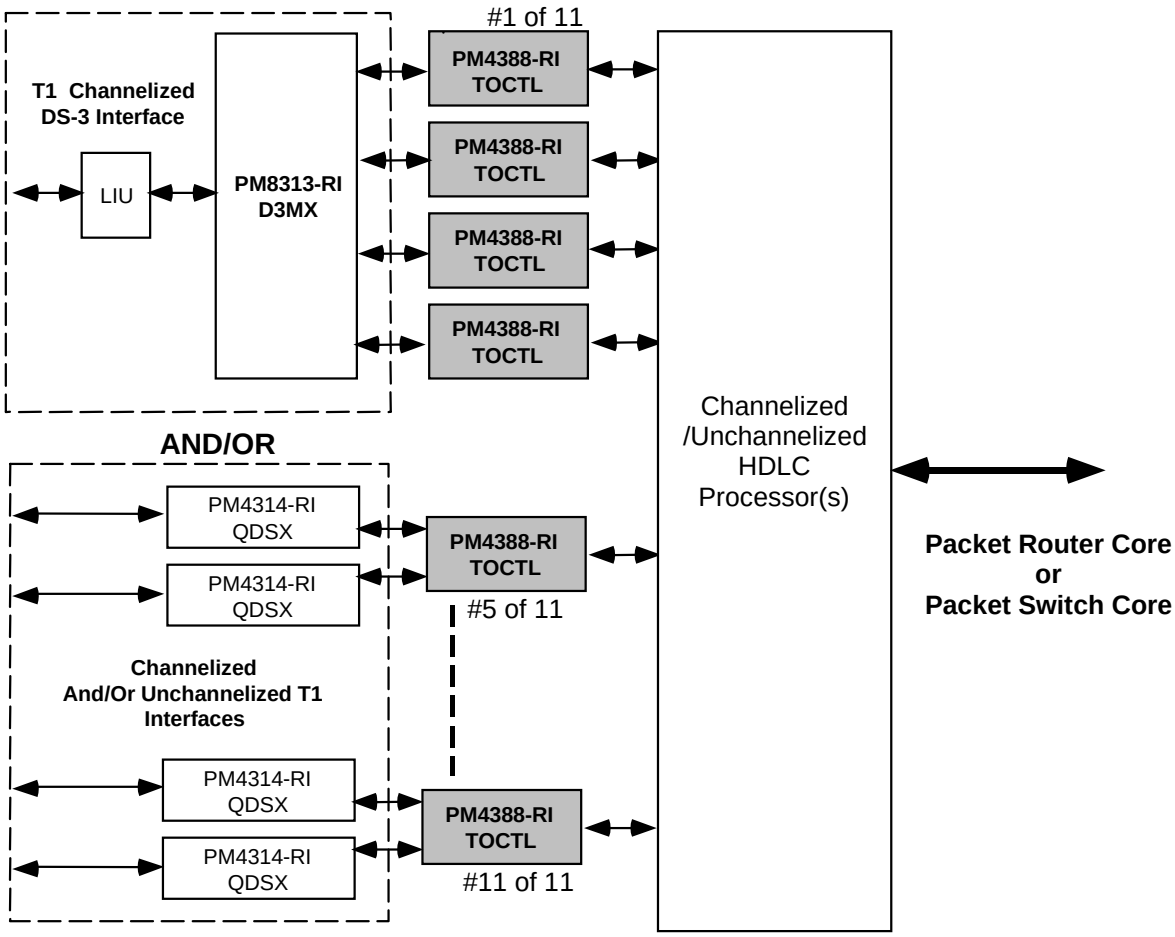
9. Bell Communications Research - Transport Systems Generic Requirements (TSGR): Common Requirement, TR-TSY-000499, Issue 5, December, 1993.

10. AT&T - Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, TR 54016, September, 1989.

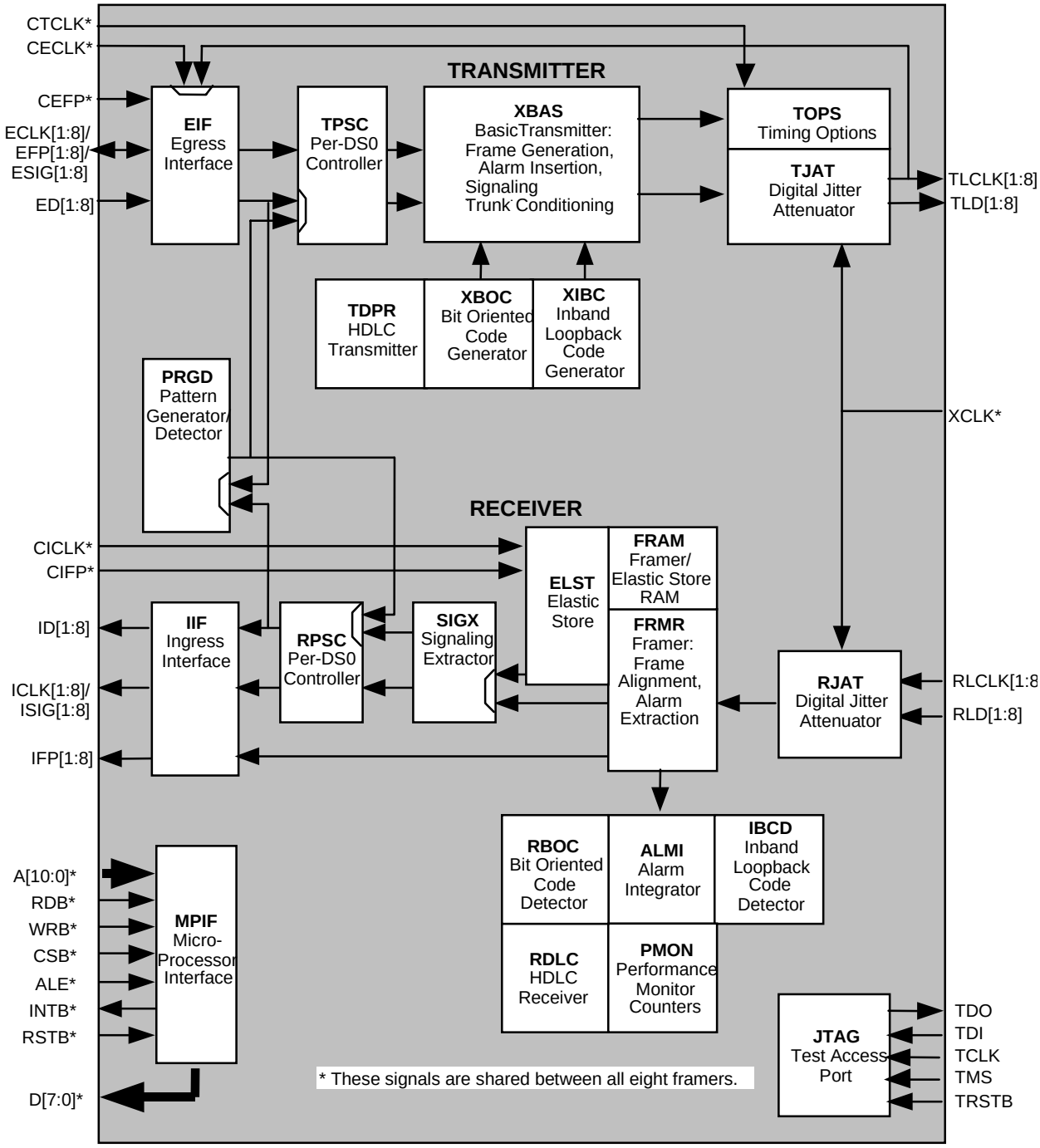
11. AT&T, TR 62411 - Accunet T1.5 - "Service Description and Interface Specification" December, 1990.

4 APPLICATION EXAMPLES

Figure 1 - High Density Channelized Port Card



5 BLOCK DIAGRAM



6 DESCRIPTION

The PM4388 Octal T1 Framer (TOCTL) is a feature-rich device for use primarily in systems carrying data (frame relay, Point to Point Protocol, or other protocols) over DS-1 facilities. Each of the framers and transmitters is independently software configurable, allowing feature selection without changes to external wiring.

On the receive side, each of eight independent framers can be configured to frame to either of the common DS-1 signal formats: (SF, ESF) or to be bypassed (unframed mode). The TOCTL detects and indicates the presence of Yellow and AIS patterns and also integrates Yellow, Red, and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided. The TOCTL also detects the presence of in-band loopback codes, ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. The HDLC messages are terminated in a 128 byte FIFO. An elastic store that optionally supports slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The TOCTL also supports idle code substitution and detection, digital milliwatt code insertion, data extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation or detection on a per-DS0 basis.

On the transmit side, the TOCTL generates framing for SF or ESF DS-1 formats, or framing can be optionally disabled. The TOCTL supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion, zero-code suppression, and pattern generation or detection on a per-DS0 basis.

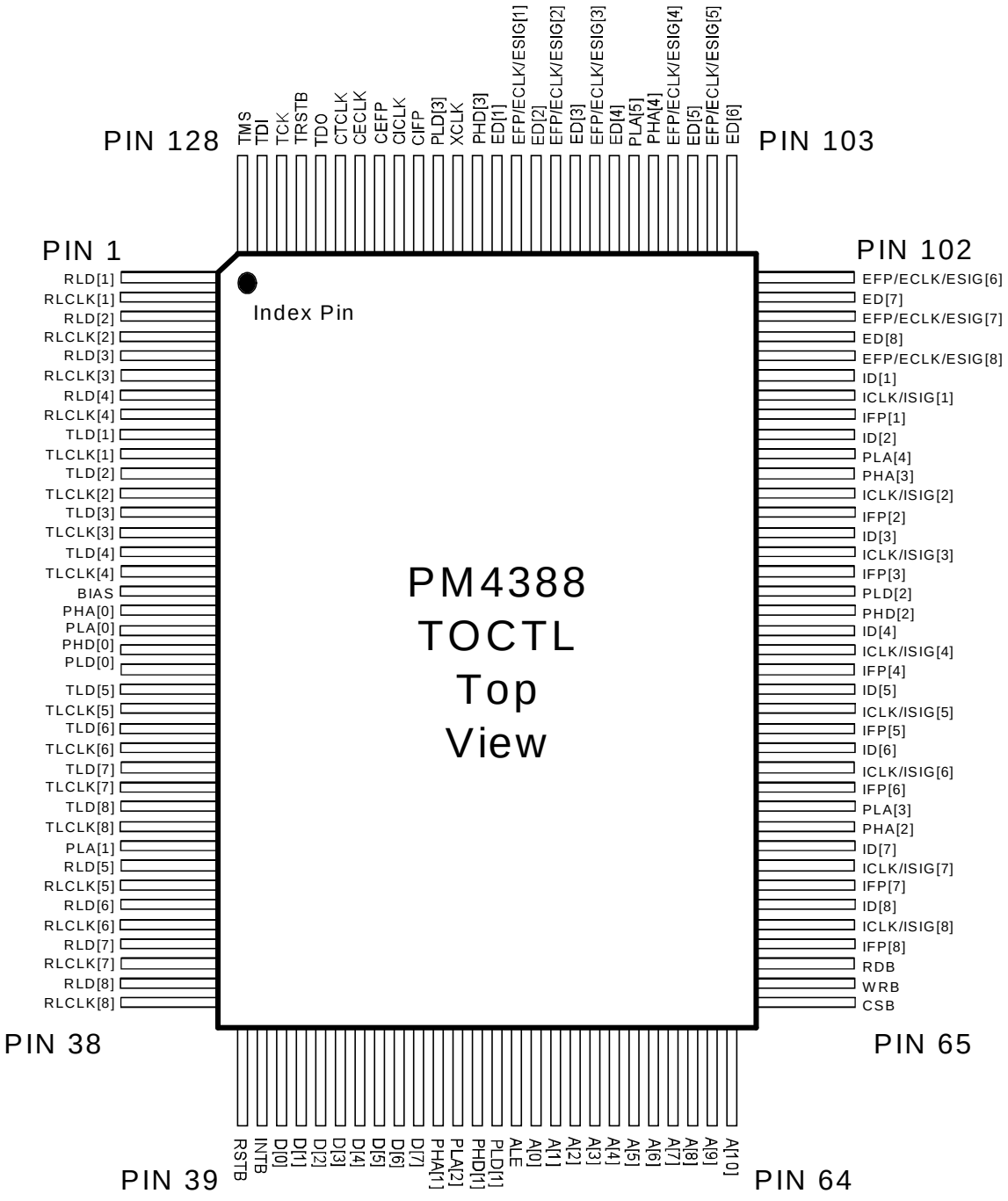
The TOCTL can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path.

The TOCTL provides a parallel microprocessor interface for controlling the operation of the TOCTL device. Serial PCM interfaces allow 1.544 Mbit/s ingress/egress system interfaces to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

It should be noted that the TOCTL device operates on unipolar data only: B8ZS substitution and line code violation monitoring, if required, must be processed by the T1 LIU.

7 PIN DIAGRAM

The TOCTL is packaged in a 128-pin plastic QFP package having a body size of 14mm by 20mm and a pin pitch of 0.5mm.



The TOCTL is also available in a 128 pin Chip Array Ball Grid Array (CABGA) package having a body size of 11mm by 11mm and a ball pitch of 0.8mm.

	12	11	10	9	8	7	6	5	4	3	2	1	
A	ED[7]	ED[6]	EFP/ ECLK/ ESIG[4]	PLA[5]	ED[3]	EFP/ ECLK/ ESIG[1]	PHD[3]	CICLK	CTCLK	TCK	RLD[1]	RLD[3]	A
B	ID[1]	ED[8]	EFP/ ECLK/ ESIG[6]	ED[5]	EFP/ ECLK/ ESIG[2]	ED[1]	XCLK/ VCLK	CIFP	CECLK	TMS	RLD[2]	RLD[4]	B
C	ID[2]	ICLK/ ISIG[1]	EFP/ ECLK/ ESIG[8]	EFP/ ECLK/ ESIG[7]	PHA[4]	EFP/ ECLK/ ESIG[3]	PLD[3]	CEFP	TDO	RLCLK[1]	RLCLK[3]	TLCLK[1]	C
D	ICLK/ ISIG[2]	IFP[2]	PHA[3]	IFP[1]	EFP/ ECLK/ ESIG[5]	ED[4]	ED[2]	TRSTB	TDI	RLCLK[2]	TLD[1]	TLCLK[2]	D
E	ICLK/ ISIG[3]	IFP[3]	ID[3]	PLA[4]					RLCLK[4]	TLD[2]	TLCLK[4]	TLD[4]	E
F	ID[4]	PHD[2]	PLD[2]	ID[5]					TLD[3]	TLCLK[3]	PLA[0]	PHA[0]	F
G	IFP[4]	ICLK/ ISIG[4]	ID[6]	ICLK/ ISIG[6]		**BOTTOM VIEW**			BIAS	TLD[5]	PLD[0]	PHD[0]	G
H	IFP[5]	ICLK/ ISIG[5]	PLA[3]	ICLK/ ISIG[7]					TLCLK[8]	TLCLK[6]	TLCLK[5]	TLD[6]	H
J	IFP[6]	ID[7]	IFP[8]	A[9]	A[7]	PHA[1]	D[4]	INTB	RLD[5]	TLD[8]	TLD[7]	TLCLK[7]	J
K	PHA[2]	ID[8]	WRB	A[6]	A[3]	A[0]	D[5]	D[2]	RLCLK[7]	RLCLK[6]	RLCLK[5]	PLA[1]	K
L	IFP[7]	RDB	A[10]	A[4]	A[1]	ALE	PHD[1]	D[7]	D[0]	RLCLK[8]	RLD[7]	RLD[6]	L
M	ICLK/ ISIG[8]	CSB	A[8]	A[5]	A[2]	PLD[1]	PLA[2]	D[6]	D[3]	D[1]	RSTB	RLD[8]	M
	12	11	10	9	8	7	6	5	4	3	2	1	

8 PIN DESCRIPTION

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
RLD[1] RLD[2] RLD[3] RLD[4] RLD[5] RLD[6] RLD[7] RLD[8]	Input	1 3 5 7 31 33 35 37	A2 B2 A1 B1 J4 L1 L2 M1	Receive Line Data (RLD[1:8]). RLD[1:8] contain the receive stream from each of the eight DS-1 line interface units, or from a higher order demultiplex interface. These inputs are sampled on the active edge of the corresponding RLCLK[1:8].
RLCLK[1] RLCLK[2] RLCLK[3] RLCLK[4] RLCLK[5] RLCLK[6] RLCLK[7] RLCLK[8]	Input	2 4 6 8 32 34 36 38	C3 D3 C2 E4 K2 K3 K4 L3	Receive Line Clocks (RLCLK[1:8]). Each input is an externally recovered 1.544 MHz line clock that samples the RLD[x] inputs on its active edge. RLCLK[x] may be a gapped clock subject to the timing constraints in the AC Timing section of this datasheet.

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
ICLK[1] ICLK[2] ICLK[3] ICLK[4] ICLK[5] ICLK[6] ICLK[7] ICLK[8]/	Output	96 91 88 83 80 77 72 69	C11 D12 E12 G11 H11 G9 H9 M12	Ingress Clocks (ICLK[1:8]). The Ingress Clocks are active when the external signaling interface is disabled. Each ingress clock is a smoothed (jitter attenuated) version of the associated receive line clock (RLCLK[x]). When the Clock Master: NxDS0 mode is active, ICLK[x] is a gapped version of the smoothed RLCLK[x]. When Clock Slave: ICLK Reference mode is active, ICLK[x] may optionally be the smoothed RLCLK[x], or the smoothed RLCLK[x] divided by 193. When Clock Master: Full DS1 mode is active, IFP[x] and ID[x] are updated on the active edge of ICLK[x]. When the Clock Master: NxDS0 mode is active, ID[x] is updated on the active edge of ICLK[x].
ISIG[1] ISIG[2] ISIG[3] ISIG[4] ISIG[5] ISIG[6] ISIG[7] ISIG[8]				Ingress Signaling (ISIG[1:8]). When the Clock Slave: External Signaling mode is enabled, each ISIG[x] contains the extracted signaling bits for each channel in the frame, repeated for the entire superframe. Each channel's signaling bits are valid in bit locations 5,6,7,8 of the channel and are channel-aligned with the ID[x] data stream. ISIG[x] is updated on the active edge of the common ingress clock, CICLK.
IFP[1] IFP[2] IFP[3] IFP[4] IFP[5] IFP[6] IFP[7] IFP[8]	Output	95 90 87 82 79 76 71 68	D9 D11 E11 G12 H12 J12 L12 J10	Ingress Frame Pulse (IFP[1:8]). The IFP[x] outputs are intended as timing references. IFP[x] indicates the frame alignment or the superframe alignment of the ingress stream, ID[x]. When Clock Master: Full DS1 mode is active, IFP[x] is updated on the active edge of the associated ICLK[x]. When Clock Master: NxDS0 mode is active, ICLK[x] is gapped during the pulse on IFP[x]. When the Clock Slave ingress modes are active, IFP[x] is updated on the active edge of CICLK.

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
ID[1] ID[2] ID[3] ID[4] ID[5] ID[6] ID[7] ID[8]	Output	97 94 89 84 81 78 73 70	B12 C12 E10 F12 F9 G10 J11 K11	Ingress Data (ID[1:8]). Each ID[x] signal contains the recovered data stream which may have been passed through the elastic store. When the Clock Slave ingress modes are active, the ID[x] stream is aligned to the common ingress timing and is updated on the active edge of CICLK. When the Clock Master ingress modes are active, ID[x] is aligned to the receive line timing and is updated on the active edge of the associated ICLK[x].
CICLK	Input	120	A5	Common Ingress Clock (CICLK). CICLK is either a 1.544MHz or 2.048MHz clock with optional gapping for adaptation to non-uniform backplane data streams. CICLK is common to all eight framers. CIFP is sampled on the active edge of CICLK. When the Clock Slave ingress modes are active, ID[x], ISIG[x], and IFP[x] are updated on the active edge of CICLK.
CIFP	Input	119	B5	Common Ingress Frame Pulse (CIFP). When the elastic store is enabled (Clock Slave mode is active on the ingress side), CIFP is used to frame align the ingress data to the system frame alignment. CIFP is common to all eight framers. When frame alignment is required, a pulse at least 1 CICLK cycle wide must be provided on CIFP a maximum of once every frame (nominally 193 bit times or 256 bit times if the 2.048 MHz rate is selected). If ingress signaling alignment is required, ingress signaling alignment must be enabled, and a pulse at least 1 CICLK cycle wide must be provided on CIFP every 12 or 24 frame times. CIFP is sampled on the active edge of CICLK.

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
ED[1] ED[2] ED[3] ED[4] ED[5] ED[6] ED[7] ED[8]	Input	115 113 111 109 105 103 101 99	B7 D6 A8 D7 B9 A11 A12 B11	Egress Data (ED[1:8]). The egress data streams to be transmitted are input on these pins. When the Clock Master: Full DS1 mode is active, ED[x] is sampled on the rising edge of TLCLK[x]. When the Clock Master: NxDS0 mode is active, ED[x] is sampled on the active edge of ECLK[x]. When the Clock Slave egress modes are active, ED[x] is sampled on the active edge of CECLK.
EFP[1] EFP[2] EFP[3] EFP[4] EFP[5] EFP[6] EFP[7] EFP[8]/	I/O	114 112 110 106 104 102 100 98	A7 B8 C7 A10 D8 B10 C9 C10	Egress Frame Pulse (EFP[1:8]). When the Clock Master: Full DS1 or Clock Slave: EFP Enabled modes are active, the EFP[1:8] outputs indicate the frame alignment or the superframe alignment of each of the eight framers. When the Clock Master modes are active, EFP[x] is updated by the falling edge of the TLCLK[x]. When the Clock Slave egress modes are active, EFP[x] is updated on the active edge of CECLK.
ECLK[1] ECLK[2] ECLK[3] ECLK[4] ECLK[5] ECLK[6] ECLK[7] ECLK[8]				Egress Clock (ECLK[1:8]). When the Clock Master: NxDS0 mode is active, the ECLK[x] output is used to sample the associated egress data (ED[x]). ECLK[x] is a version of TLCLK[x] that is gapped during the framing bit position and optionally for between 1 and 23 DS0 channels in the associated ED[x] stream. ED[x] is sampled on the active edge of the associated ECLK[x].
ESIG[1] ESIG[2] ESIG[3] ESIG[4] ESIG[5] ESIG[6] ESIG[7] ESIG[8]				Egress Signaling (ESIG[1:8]). When the Clock Slave: External Signaling mode is active, the ESIG[8:1] inputs contain the signaling bits for each channel in the transmit data frame, repeated for the entire superframe. Each channel's signaling bits are in bit locations 5,6,7,8 of the channel and are frame-aligned by the common egress frame pulse, CEFP. ESIG[x] is sampled on the active edge of CECLK.

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
CTCLK	Input	123	A4	Common Transmit Clock (CTCLK). This input signal is used to generate the TLCLK[x] clock signals. Depending on the configuration of the TOCTL, CTCLK may be a 12.352 MHz clock (so TLCLK[x] is generated by dividing CTCLK by 8), or a line rate clock (so TLCLK[x] is generated directly from CTCLK, or from CTCLK after jitter attenuation), or a multiple of 8kHz (Nx8khz, where 1•N•256) so long as CTCLK is jitter-free when divided down to 8kHz (in which case TLCLK is derived by the DJAT PLL using CTCLK as a reference). The TOCTL may be configured to ignore the CTCLK input and utilize CECLK or RLCLK[x] instead. RLCLK[x] is automatically substituted for CTCLK if line loopback is enabled.
CECLK	Input	122	B4	Common Egress Clock (CECLK). The common egress clock is used to time the egress interface when Clock Slave mode is enabled in the egress side. CECLK may be a 1.544MHz or 2.048MHz clock with optional gapping for adaptation from non-uniform system clocks. When the Clock Slave: EFP Enabled mode is active, CEFP and ED[x] are sampled on the active edge of CECLK, and EFP[x] is updated on the active edge of CECLK. When the Clock Slave: External Signaling mode is active, CEFP, ESIG[x] and ED[x] are sampled on the active edge of CECLK.

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
CEFP	Input	121	C5	Common Egress Frame Pulse. CEFP may be used to frame align the framers to the system backplane. If frame alignment only is required, a pulse at least 1 CECLK cycle wide must be provided on CEFP every 193 bit times. If superframe alignment is required, transmit superframe alignment must be enabled, and a pulse at least 1 CECLK cycle wide must be provided on CEFP every 12 or 24 frame times, on the last F-bit of the multiframe. CEFP is sampled on the active edge of CECLK. CEFP has no effect in the Clock Master egress modes
TLCLK[1] TLCLK[2] TLCLK[3] TLCLK[4] TLCLK[5] TLCLK[6] TLCLK[7] TLCLK[8]	Output	10 12 14 16 23 25 27 29	C1 D1 F3 E2 H2 H3 J1 H4	Transmit Line Clock (TLCLK[1:8]). The TLD[x] outputs are updated on the active edge of the associated TLCLK[x]. When the Clock Master: Full DS1 mode is active, ED[1:8] is sampled on the active edge of TLCLK[x] and EFP[1:8] is updated on the active edge of TLCLK[x]. TLCLK[x] is a 1.544 MHz clock that is adequately jitter and wander free in absolute terms to permit an acceptable DS-1 signal to be generated. Depending on the configuration of the TOCTL, TLCLK[x] may be derived from CTCLK, CECLK, or RLCLK[x], with or without jitter attenuation.
TLD[1] TLD[2] TLD[3] TLD[4] TLD[5] TLD[6] TLD[7] TLD[8]	Output	9 11 13 15 22 24 26 28	D2 E3 F4 E1 G3 H1 J2 J3	Transmit Line Data (TLD[1:8]). TLD[1:8] contain the transmit stream for each of the eight DS-1 line interface units, or for the higher order multiplex interface. These outputs are updated on the active edge of the corresponding TLCLK[1:8].

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
XCLK/	Input	117	B6	Crystal Clock Input (XCLK). This signal provides timing for many portions of the TOCTL. XCLK is nominally a 37.056 MHz ± 32ppm, 50% duty cycle clock.
VCLK				Vector Clock (VCLK). The VCLK signal is used during TOCTL production test to verify internal functionality.
INTB	Output	40	J5	Active low open-drain Interrupt signal (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
CSB	Input	65	M11	Active low chip select (CSB). This signal must be low to enable TOCTL register accesses. CSB must go high at least once after a powerup to clear internal test modes. If CSB is not used, then it should be tied to an inverted version of RSTB, in which case, RDB and WRB determine register accesses.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	41 42 43 44 45 46 47 48	L4 M3 K5 M4 J6 K6 M5 L5	Bidirectional data bus (D[7:0]). This bus is used during TOCTL read and write accesses.
RDB	Input	67	L11	Active low read enable (RDB). This signal is pulsed low to enable a TOCTL register read access. The TOCTL drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
WRB	Input	66	K10	Active low write strobe (WRB). This signal is pulsed low to enable a TOCTL register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
ALE	Input	53	L7	Address latch enable (ALE). This signal latches the address bus contents, A[10:0], when low, allowing the TOCTL to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent. ALE has an integral pull-up.
RSTB	Input	39	M2	Active low reset (RSTB). This signal is set low to asynchronously reset the TOCTL. RSTB is a Schmitt-trigger input with integral pull-up. When resetting the device, RSTB must be asserted for a minimum of 100 ns to ensure that the TOCTL is completely reset.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	54 55 56 57 58 59 60 61 62 63 64	K7 L8 M8 K8 L9 M9 K9 J8 M10 J9 L10	Address bus (A[10:0]). This bus selects specific registers during TOCTL register accesses.
TCK	Input	126	A3	Test Clock (TCK).The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	128	B3	Test Mode Select (TMS). The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
TDI	Input	127	D4	Test Input (TDI).The test data input (TDI) signal carries test data into the TOCTL via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate	124	C4	Test Output (TDO).The test data output (TDO) signal carries test data out of the TOCTL via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is tristated except when scanning of data is in progress.
TRSTB	Input	125	D5	Test Reset (TRSTB).The active low test reset (TRSTB) signal provides an asynchronous TOCTL test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. The JTAG TAP controller must be initialized when the TOCTL is powered up. If the JTAG port is not used TRSTB must be connected to the RSTB input or grounded.
BIAS	Input	17	G4	+5V Bias (BIAS). The BIAS input is used to implement 5V tolerance on the inputs. BIAS must be connected to a well decoupled +5V rail if 5V tolerant inputs are required. If 5V tolerant inputs are not required, BIAS must be connected to a well-decoupled 3.3V DC supply together with the power pins PHA[3:0] and PHD[3:0].
PHA[0] PHA[1] PHA[2] PHA[3] PHA[4]	Power	18 49 74 92 107	F1 J7 K12 D10 C8	Pad ring power pins (PHA[4:0]). These pins must be connected to a common, well decoupled +3.3V DC supply together with the core power pins PHD3:0] .
PHD[0] PHD[1] PHD[2] PHD[3]	Power	20 51 85 116	G1 L6 F11 A6	Core power pins (PHD[3:0]). These pins must be connected to a common, well decoupled +3.3V DC supply together with the pad ring power pins PHA[4:0].

Pin Name	Type	Pin No. -RI	Pin No. -NI	Function
PLA[0] PLA[1] PLA[2] PLA[3] PLA[4] PLA[5]	Ground	19 30 50 75 93 108	F2 K1 M6 H10 E9 A9	Pad ring ground pins (PLA[5:0]). These pins must be connected to a common ground together with the core ground pins PLD[3:0].
PLD[0] PLD[1] PLD[2] PLD[3]	Ground	21 52 86 118	G2 M7 F10 C6	Core ground pins (PLD[3:0]). These pins must be connected to a common ground together with the pad ring ground pins PLA[5:0].

Notes on Pin Description:

1. The PLA[5:0] and PLD[3:0] ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. The PHA[4:0] and PHD[3:0] power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. These power supply connections must all be utilized and must all connect to a common +3.3 V or ground rail, as appropriate.

2. During power-up, and power-down the voltage on the BIAS pin must be kept equal to or greater than the voltage on the PHA[4:0] and PHD[3:0] pins, to avoid damage to the device.

3. Inputs RSTB, TMS, TDI, and ALE have integral pull-up resistors.

4. All outputs have 2 mA drive capability except for the D[7:0] bidirectionals and the TLCLK[8:1], ECLK[8:1], and ICLK[8:1] clock outputs which have 3 mA drive capability.

5. All inputs and bidirectionals present minimum capacitive loading.

6. Certain inputs are described as being sampled by the "active edge" of a particular clock. These inputs may be enabled to be sampled on either the rising edge or the falling edge of that clock, depending on the software configuration of the device.

9 FUNCTIONAL DESCRIPTION

9.1 Framer (FRMR)

The framing function is provided by the FRMR block. This block searches for the framing bit position in the ingress stream. It works in conjunction with the FRAM block to search for the framing bit pattern in the standard superframe (SF), or extended superframe (ESF) framing formats. When searching for frame, the FRMR simultaneously examines each of the 193 (SF) or each of the 772 (ESF) framing bit candidates. The FRAM block is addressed and controlled by the FRMR while frame synchronization is acquired.

The time required to acquire frame alignment to an error-free ingress stream, containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0), is dependent upon the framing format. For SF format, the FRMR block will determine frame alignment within 4.4ms 99 times out of 100. For ESF format, the FRMR will determine frame alignment within 15 ms 99 times out of 100.

Once the FRMR has found frame, the ingress data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or a CRC-6 error in ESF), and severely errored framing events. The FRMR also detects out-of-frame, based on a selectable ratio of framing bit errors.

The FRMR can also be disabled to allow reception of unframed data. While the FRMR is disabled, control of the FRAM block is relinquished for use as the elastic store.

9.2 Framer/Slip Buffer RAM (FRAM)

The Framer/Slip Buffer RAM function is provided by the Framer RAM (FRAM) block. The FRAM is used to store up to 4 frames of data while the FRMR is acquiring frame and up to 2 frames of data during normal operation (i.e. when accessed by Elastic Store). The FRAM is shared between the Elastic Store (ELST) and the FRMR: when frame synchronization is lost, the FRMR takes control of the FRAM and uses it to find frame; when frame synchronization is determined, the FRMR relinquishes control of FRAM to ELST which buffers the incoming PCM data.

9.3 Inband Loopback Code Detector (IBCD)

The Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and DEACTIVATE code sequences in either framed or unframed data streams. The inband code sequences are expected to be overwritten by the framing bit in framed data streams. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code in the ingress stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

If inband code detection is not desired, the IBCD_IDLE bit may be set in the Receive Line Options register, allowing the IBCD to be used to detect the DS1 idle code in the receive stream. Setting the IBCD_IDLE bit gaps the data to the IBCD block during the frame bit so that the IBCD searches for the programmed pattern in the payload.

9.4 Performance Monitor Counters (PMON)

The Performance Monitor Counters function is provided by the PMON block. The block accumulates CRC error events, Frame Synchronization bit error events, out-of-frame events, and Change of Frame Alignment (COFA) events with saturating counters over consecutive intervals as defined by the time between writes of the Revision/Chip ID/Global PMON update register (00CH), or every second via the AUTOUPDATE feature in the Receive Line Options register, or by writing to any of the PMON holding registers. The PMON uses a 12-bit counter for Bit Error Events (CRC-6 failures in ESF or framing bit errors in SF), a 9-bit counter for framing bit errors, a 5-bit counter for OOF events, and a 3-bit counter for Change of Frame Alignment events. When an update is initiated by any means, the PMON in each framer transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. The holding register addresses are contiguous to facilitate polling operations.

9.5 Bit Oriented Code Detector (RBOC)

The Bit Oriented Code detection function is provided by the RBOC block. This block detects the presence of 63 of the possible 64 bit oriented codes transmitted in the Facility Data Link channel in ESF framing format, as defined in

ANSI T1.403 and in TR-TSY-000194. The 64th code (111111) is similar to the HDLC flag sequence and is used by the RBOC to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated at least 10 times. The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the control register.

Valid BOC are indicated through an internal status register. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

9.6 RDLC Facility Data Link Receiver

The RDLC is a microprocessor peripheral used to receive HDLC frames on the 4kHz ESF facility data link.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

9.7 Alarm Integrator (ALMI)

The Alarm Integration function is provided by the ALMI block. This block detects the presence of Yellow, Red, and AIS Carrier Fail Alarms (CFA) in SF, or ESF formats. The alarm detection and integration is compatible with the specifications defined in ANSI T1.403 and TR-TSY-000191.

The ALMI block declares the presence of Yellow alarm when the Yellow pattern has been received for 425 ms (± 50 ms); the Yellow alarm is removed when the Yellow pattern has been absent for 425 ms (± 50 ms). The presence of Red alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the Red alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms). The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream have been present for 1.5 sec (±100 ms); the AIS alarm is removed when the AIS condition has been absent for 16.8 sec (±500 ms).

CFA alarm detection algorithms operate in the presence of a 10^{-3} bit error rate.

The ALMI also indicates the presence or absence of the Yellow, Red, and AIS alarm signal conditions over 40 ms, 40 ms, and 60 ms intervals, respectively, allowing an external microprocessor to integrate the alarm conditions via software with any user-specific algorithms. Alarm indication is provided through internal register bits.

9.8 Elastic Store (ELST)

The Elastic Store (ELST) synchronizes ingress frames to the common ingress clock and frame pulse (CICLK, CIFP) in the Clock Slave ingress modes. The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

The elastic store can be bypassed to eliminate the 2 frame delay. In this configuration (the Clock Master ingress modes), the elastic store is used to synchronize the ingress frames to the transmit line clock (TLCLK[x]) so that per-DS0 loopbacks may be enabled. Per-DS0 loopbacks are only available when the elastic store is bypassed, or when CECLK and CICLK are tied together and CEFP and CIFP are tied together, and the CICLKRISE and CECLKFALL register bits are either both logic 1 or both logic 0. CICLKRISE and CECLKFALL are found in registers 3 and 4 of each octant, respectively.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The subsequent ingress frame is deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The previous ingress frame is repeated.

A slip operation is always performed on a frame boundary.

For payload conditioning, the ELST inserts a programmable idle code into all channels when the FRMR is out of frame synchronization. If the data is required to pass through the TOCTL unchanged during an out-of-frame condition, then the elastic store may be bypassed.

9.9 Signaling Extractor (SIGX)

The Signaling Extraction (SIGX) block provides signaling bit extraction from the ingress stream for ESF, and SF framing formats. When the external signaling interface is enabled, the SIGX serializes the bits into a serial stream aligned to the synchronized outgoing data stream. The signaling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5,6,7,8) in ESF framing format. In SF format, the A and B bits are repeated in locations C and D (i.e. the signaling stream contains the bits ABAB for each channel). The SIGX also provides user control over signaling freezing and provides control over signaling bit fixing and signaling debounce on a per-DS0 basis. The block contains three superframes worth of signal buffering to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801. With signaling debounce enabled, the per-DS0 signaling state must be in the same state for 2 superframes before appearing on the serial output stream. The SIGX indicates the occurrence of a change of signaling state for each DS0 via an interrupt and by a change of signaling state bit for each DS0.

9.10 Receive Per-DS0 Serial Controller (RPSC)

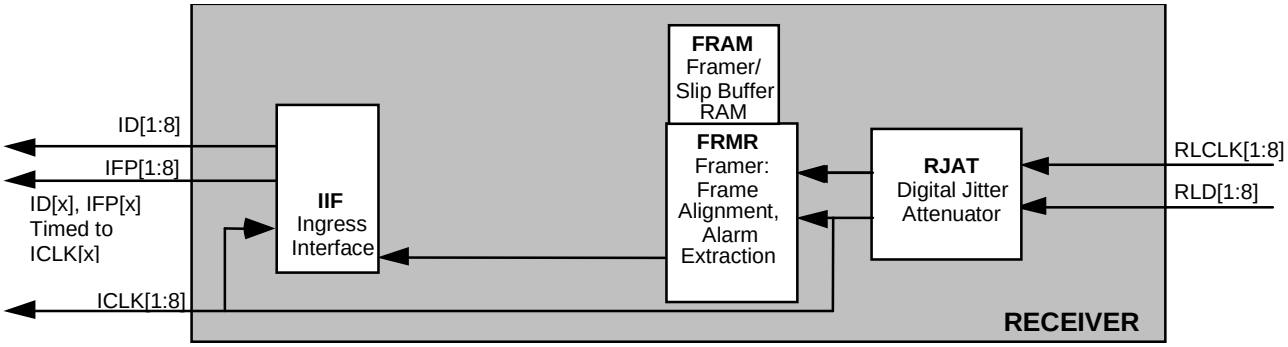
The RPSC allows data and signaling trunk conditioning to be applied on the receive DS-1 stream on a per-DS0 basis. It also allows per-DS0 control of data inversion, the extraction of clock and data on ICLK[x] and ID[x] (when the Clock

Master: NxDS0 mode is active), and the detection or generation of pseudo-random or repetitive patterns. The RPSC operates on the data after its passage through ELST, so that data and signaling conditioning may overwrite the ELST trouble code.

9.11 Ingress Interface (IIF)

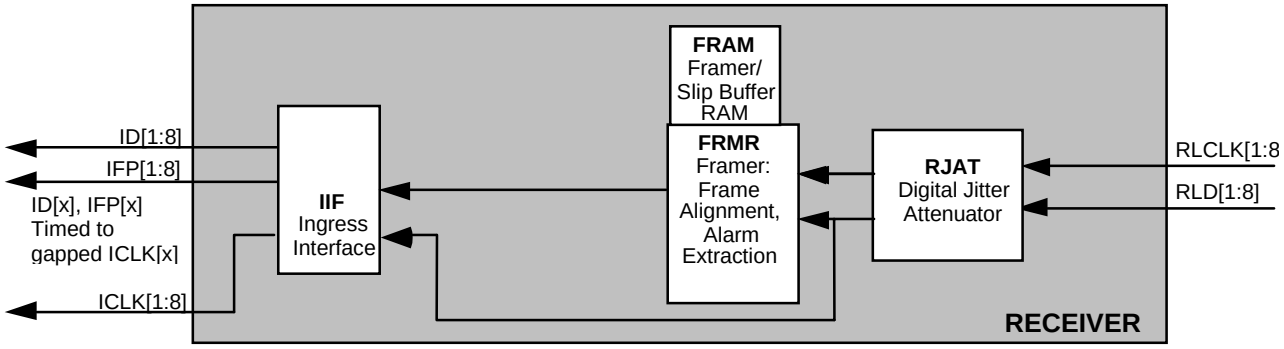
The Ingress Interface allows ingress data to be presented to a system using one of four possible modes as selected by the IMODE[1:0] bits in the Ingress Interface Options Register (Register 001H, 081H, 101H, 181H, 201H, 281H, 301H, 381H): Clock Master: Full DS1, Clock Master : NxDS0, Clock Slave : ICLK Reference, or Clock Slave: External Signaling.

Figure 2 - Clock Master: Full DS1



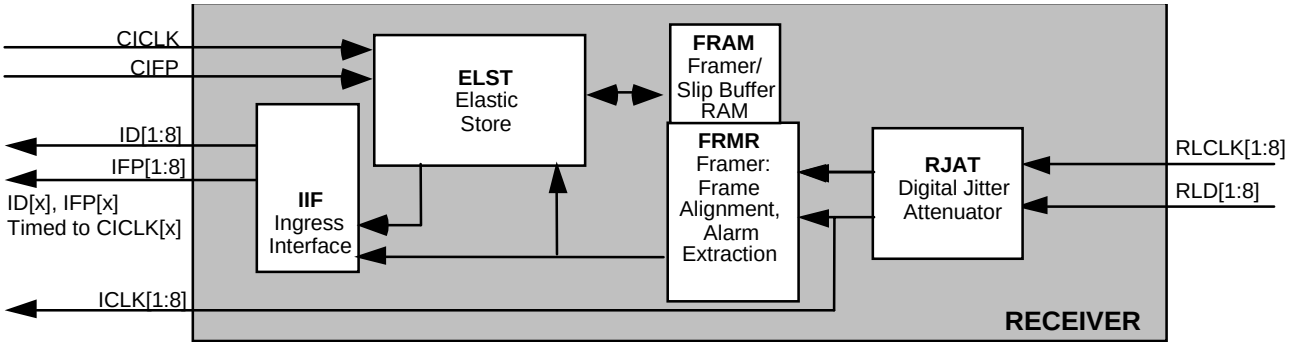
In Clock Master: Full DS1 mode, the elastic store is bypassed and the ingress clock (ICLK[x]) is a jitter attenuated version of the 1.544 MHz receive line clock (RLCLK[x]). ICLK[x] is pulsed for each bit in the 193 bit frame. The ingress data appears on ID[x] and the ingress frame alignment is indicated by IFP[x]. In this mode, data passes through the TOCTL unchanged during out-of-frame conditions, similar to an offline framer system. When the TOCTL is the clock master in the ingress direction, then the elastic store is used to buffer between the ingress and egress clocks to facilitate per-DS0 loopback.

Figure 3 - Clock Master: NxDS0



In this mode, ICLK[x] is derived from RLCLK[x], and is gapped on a per DS0 basis so that a subset of the 24 channels in the T1 frame is extracted on ID[x]. Channel extraction is controlled by the RPSC block. The framing bit position is always gapped, so the number of ICLK[x] pulses is controllable from 0 to 192 pulses per frame on a per-DS0 basis. In this mode, data passes through the TOCTL unchanged during out-of-frame conditions. The parity functions are not usable in NxDS0 mode. When the TOCTL is the clock master in the ingress direction, then the elastic store is used to buffer between the ingress and egress clocks to facilitate per-DS0 loopback.

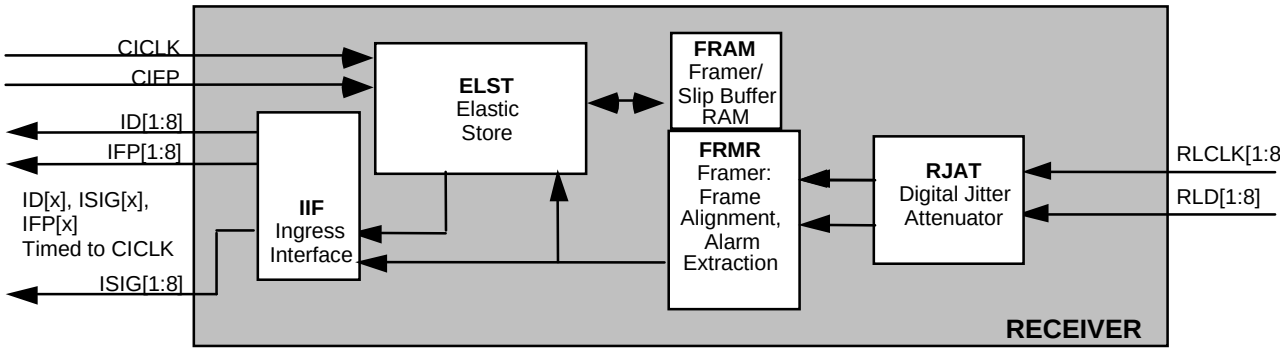
Figure 4 - Clock Slave: ICLK Reference



In this mode, the elastic store is enabled to permit CICLK to specify the ingress-side timing. The ingress data on ID[x] is bit aligned to the 1.544 MHz common ingress clock (CICLK) and is frame aligned to the common ingress frame pulse (CIFP). CICLK can be enabled to be a 1.544 MHz clock or a 2.048 MHz clock. ICLK[x] can be enabled to be either a 1.544 MHz jitter attenuated version of

RLCLK[x] or an 8 kHz version of RLCLK[x] (by dividing RLCLK[x] by 193). IFP[x] indicates either the frame or superframe alignment on ID[x].

Figure 5 - Clock Slave: External Signaling



In this mode, the elastic store is enabled to permit CICLK to specify the ingress-side timing. The ingress data on ID[x] and signaling ISIG[x] are bit aligned to the 1.544 MHz common ingress clock (CICLK) and are frame aligned to the common ingress frame pulse (CIFP). CICLK can be enabled to be a 1.544 MHz clock or a 2.048 MHz clock. ISIG[x] contains the robbed-bit signaling state (ABCD or ABAB) in the lower four bits of each channel.

9.12 Pattern Detector/Generator (PRGD)

The Pattern Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer. Patterns may be generated in either the transmit or receive directions, and detected in the opposite direction. Two types of ITU-T O.151 compliant test patterns are provided : pseudo-random and repetitive.

The PRGD can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern. The PRGD can perform an auto synchronization to the expected pattern, and generate interrupts on detection and loss of the specified pattern. The PRGD can accumulate the total number of bits received and the total number of bit errors in two saturating 32-bit counters. The counters accumulate over an interval defined by writes to the Revision/Chip ID/Global

PMON Update register (register 00CH), by writes to any PRGD accumulation register, or over a one-second interval timed to the receive line clock, via the AUTOUPDATE feature in the Receive Line Options register (000H, 080H, 100H, 180H, 200H, 280H, 300H, 380H). When an accumulation is forced by either method, then the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation. In addition to the two counters, a record of the 32 bits received immediately prior to the accumulation is available.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N bits, the PRGD will load N bits from the detected stream, and determine whether the received pattern repeats itself every N subsequent bits. Should it fail to find such a pattern, it will continue loading and checking until it finds a repetitive pattern. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences. Whenever a PRGD accumulation is forced, the PRGD stores a snapshot of the 32 bits received immediately prior to the accumulation. This snapshot may be examined in order to determine the exact nature of the repetitive pattern received by PRGD.

9.13 Basic Transmitter (XBAS)

The Basic Transmitter (XBAS) block generates the 1.544 Mbit/s T1 data stream according to SF or ESF frame formats.

A internal control stream, generated by the TPSC block, provides per-DS0 control of idle code substitution, data inversion , and zero code suppression. Three types of zero code suppression (GTE, Bell and "jammed bit 8") are supported and selected on a per-DS0 basis to provide minimum ones density control. An internal signaling control stream provides per-DS0 control of robbed bit signaling and selection of the signaling source. All channels can be forced into a trunk conditioning state (idle code substitution and signaling conditioning) by use of the Master Trunk Conditioning bit in the Configuration Register.

The transmitter can be disabled for framing via the disable bit in the Transmit Functions Enable register. When transmitting ESF formatted data, the framing bit, datalink bit, or the CRC-6 bit from the egress stream can be by-passed to the output PCM stream. Finally, the transmitter can be by-passed completely to provide an unframed operating mode.

9.14 Transmit Per-DS0 Serial Controller (TPSC)

The Transmit Per-DS0 Serial Controller allows data and signaling trunk conditioning or idle code to be applied on the transmit DS-1 stream on a per-DS0 basis. It also allows per-DS0 control of zero code suppression, data inversion, DS0 loopback (from the ingress stream), channel insertion, and the detection or generation of pseudo-random or repetitive patterns.

The TPSC interfaces directly to the XBAS block and provides serial streams for signaling control, idle code data and egress data control.

9.15 Signaling Aligner (SIGA)

When enabled, the Signaling Aligner is positioned in the egress path between the egress interface and XBAS. Its purpose is to ensure that, if the signaling on ESIG[x] is changed in the middle of a superframe, the XBAS completes transmitting the A,B,C, and D bits for the current superframe before switching to the new values. This permits signaling integrity to be preserved independent of the superframe alignment of the XBAS or the signaling data source.

9.16 Inband Loopback Code Generator (XIBC)

The Inband Loopback Code Generator function is provided by the XIBC block. This block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code and can be either framed or unframed. When the XIBC is enabled to generate framed IBC, the framing bit overwrites the inband code pattern. The contents of the code and its length are programmable from 3 to 8 bits.

9.17 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator function is provided by the XBOC block. This block transmits 63 of the possible 64 bit oriented codes in the Facility Data Link channel in ESF framing format, as defined in ANSI T1.403-1989. The 64th code (111111) is similar to the HDLC Flag sequence and is used in the XBOC to disable transmission of any bit oriented codes.

Bit oriented codes are transmitted on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The transmitted bit oriented codes have priority over any data transmitted on the FDL

except for ESF Yellow Alarm. The code to be transmitted is programmed by writing the code register.

9.18 TDPR Facility Data Link Transmitter

The Facility Data Link Transmitter (TDPR) provides a serial data link for the 4 kHz ESF facility data link. The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) may be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits the flag sequence (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the Transmit Data Register. The TDPR performs a parallel-to-serial conversion of each data byte before transmitting it.

The TDPR automatically begins transmission of data once at least one complete packet is written into its FIFO. All complete packets of data will be transmitted. After the last data byte of a packet, the CRC word (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. The TDPR will also force transmission of the FIFO data once the FIFO depth has surpassed the programmable upper limit threshold. Transmission commences regardless of whether or not a packet has been completely written into the FIFO. The user must be careful to avoid overfilling the FIFO. Underruns can only occur if the packet length is greater than the programmed upper limit threshold because, in such a case, transmission will begin before a complete packet is stored in the FIFO. An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data.

Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been

depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDRI interrupt.

9.19 Receive and Transmit Digital Jitter Attenuator (RJAT, TJAT)

The Digital Jitter Attenuation function is provided by the DJAT blocks. Each framer in the TOCTL contains two separate jitter attenuators, one between the receive line data and the ingress interface (RJAT) and the other between the egress interface and the transmit line data (TJAT). Each DJAT block receives jittered data and stores the stream in a FIFO timed to the associated clock (either RLCLK[x] or CECLK). The jitter attenuated data emerges from the FIFO timed to the jitter attenuated clock. In the RJAT, the jitter attenuated clock (ICLK[x]) is referenced to RLCLK[x]. In the TJAT, the jitter attenuated clock TLCLK[x] may be referenced to either CTCLK, CECLK, or RLCLK[x].

Each jitter attenuator generates its output clock by adaptively dividing the 37.056 MHz XCLK signal according to the phase difference between the jitter attenuated clock and the reference clock. Jitter fluctuations in the phase of the reference clock are attenuated by the phase-locked loop within each DJAT so that the frequency of the jitter attenuated clock is equal to the average frequency of the reference. To best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 6.6 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 6.6 Hz are tracked by the jitter attenuated clock. The jitter attenuated clock (ICLK[x] for the RJAT and TLCLK[x] for the TJAT) is used to read data out of the FIFO.

If the FIFO read pointer comes within one bit of the write pointer, DJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

Each DJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 28 UIpp of input jitter at jitter frequencies above 6 Hz. For jitter frequencies below 6 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications the each DJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The DJAT blocks meet the stringent low frequency jitter tolerance

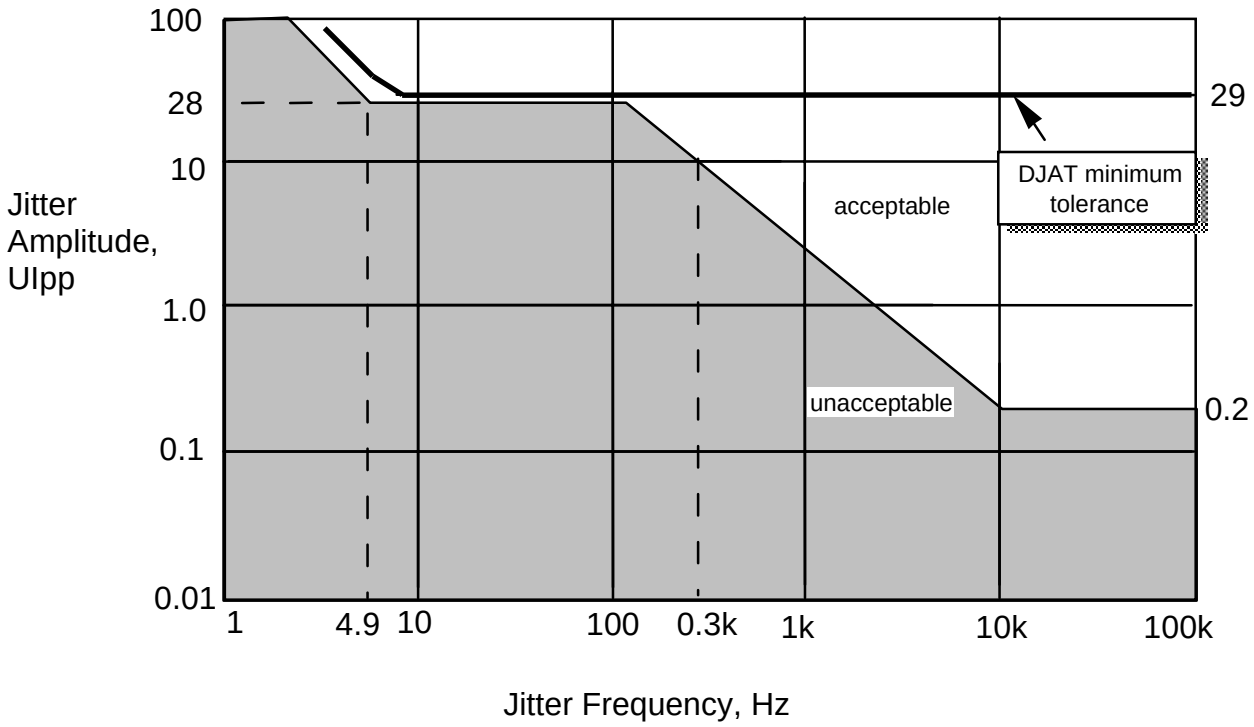
requirements of AT&T TR 62411 and thus allow compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

DJAT exhibits negligible jitter gain for jitter frequencies below 6.6 Hz, and attenuates jitter at frequencies above 6.6 Hz by 20 dB per decade. In most applications the DJAT Blocks will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (37.056 MHz) digital phase locked loop for transmit clock generation. DJAT meets the jitter transfer requirements of AT&T TR 62411. The block allows the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.

Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 29 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 354 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

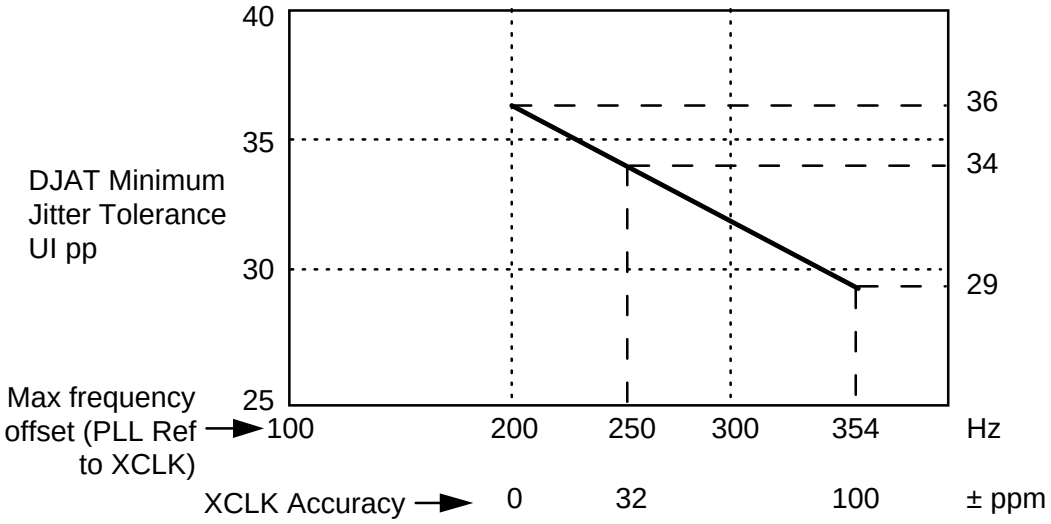
Figure 6 - DJAT Jitter Tolerance



The accuracy of the XCLK frequency and that of the reference clock used to generate the jitter attenuated clock have an effect on the minimum jitter tolerance. Given that the DJAT PLL reference clock accuracy can be ±200 Hz from 1.544 MHz, and that the XCLK input accuracy can be ±100 ppm from 37.056 MHz, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK ÷ 24 are shown in Figure 7.

An XCLK input accuracy of ±100 ppm is only acceptable if an accurate line rate reference is provided. If TJAT is left to free-run without a reference, or referenced to a derivative of XCLK, then XCLK accuracy must be ±32 ppm.

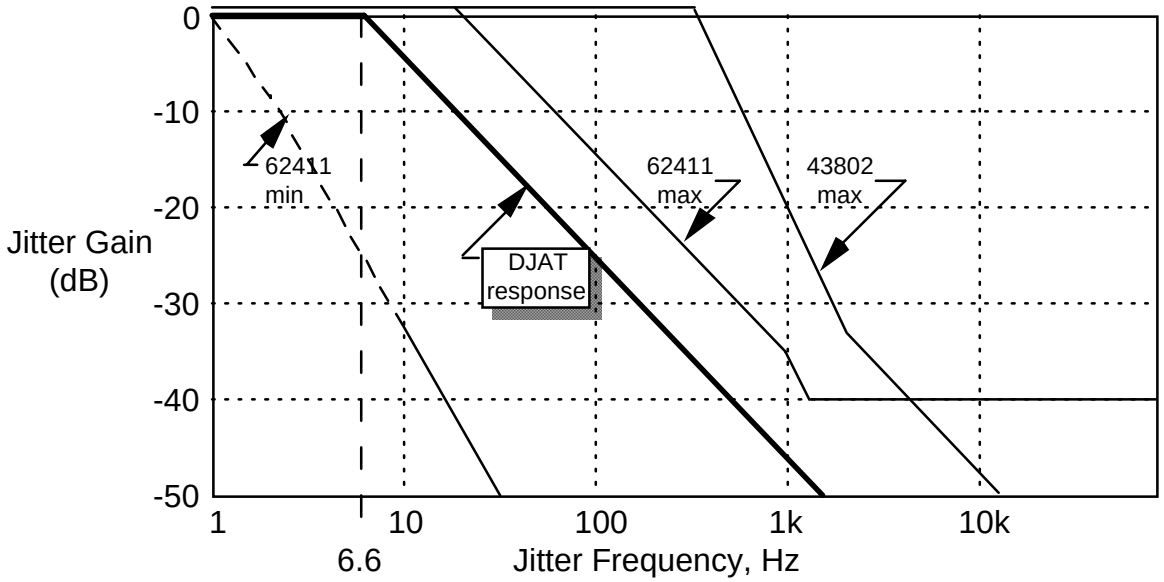
Figure 7 - DJAT Minimum Jitter Tolerance vs. XCLK Accuracy



Jitter Transfer

The output jitter for jitter frequencies from 0 to 6.6 Hz is no more than 0.1 dB greater than the input jitter, excluding the 0.042 UI residual jitter. Jitter frequencies above 6.6 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 8 below:

Figure 8 - DJAT Jitter Transfer



Frequency Range

In the non-attenuating mode, that is, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.48 to 1.608 MHz. The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (29 UIpp) and maximum XCLK frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or XCLK frequency offset.

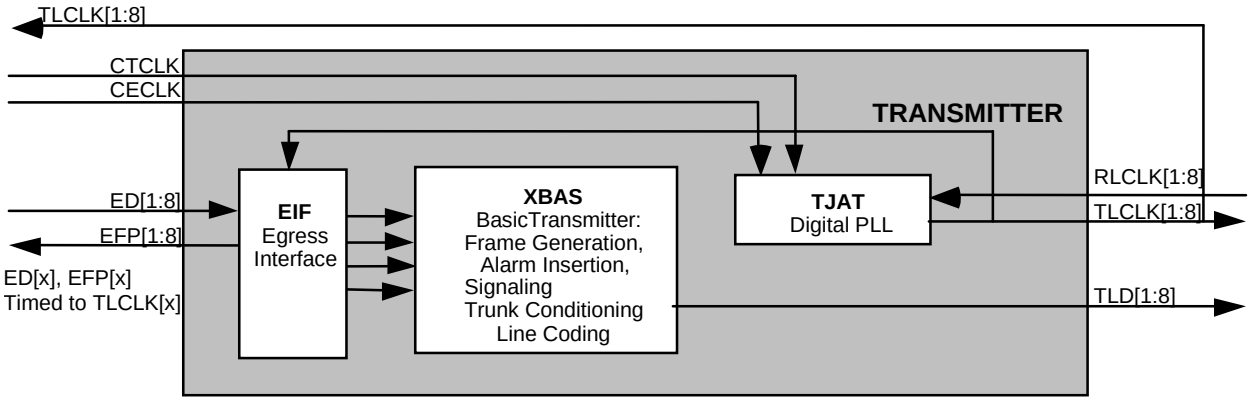
9.20 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the TJAT block, the reference clock for the TJAT digital PLL, and the clock source used to derive the output TLCLK[x] signal.

9.21 Egress Interface (EIF)

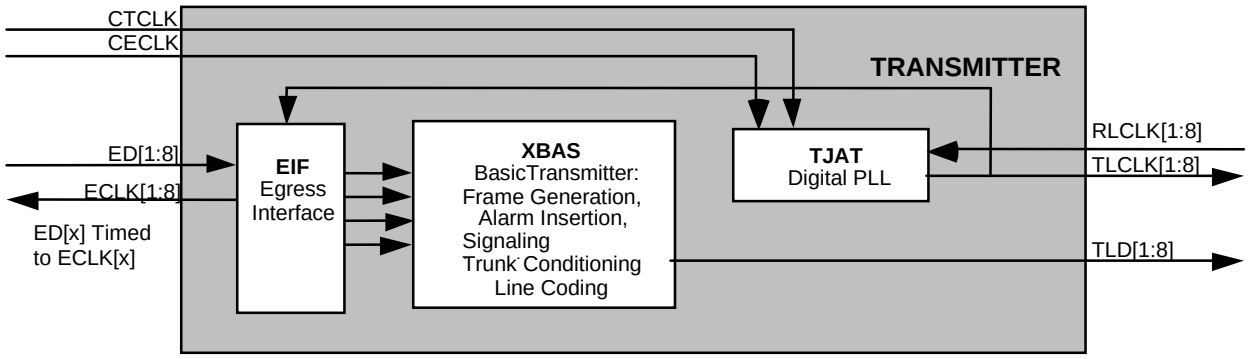
The Egress Interface allows egress data to be inserted into the transmit line using one of four possible modes, as selected by the EMODE[1:0] bits in the Egress Options Register: Clock Master: Full DS1, Clock Master: NxDS0, Clock Slave: EFP Enabled, and Clock Slave: External Signaling.

Figure 9 - Clock Master: Full DS1



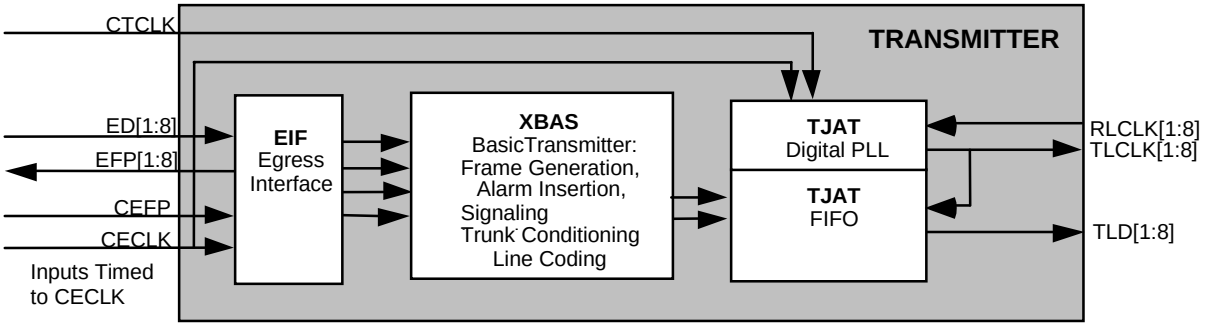
In this mode, the transmit clock output (TLCLK[x]) "pulls" data from an upstream data source. The frame alignment is indicated to the upstream data source using EFP[x]. TLCLK[x] may be generated by the TJAT PLL, referenced to either CECLK, CTCLK, or RLCLK[x]. TLCLK[x] may also be derived directly from CTCLK or XCLK. The CEFP input is unused in this mode, and has no effect.

Figure 10 - Clock Master: NxDS0



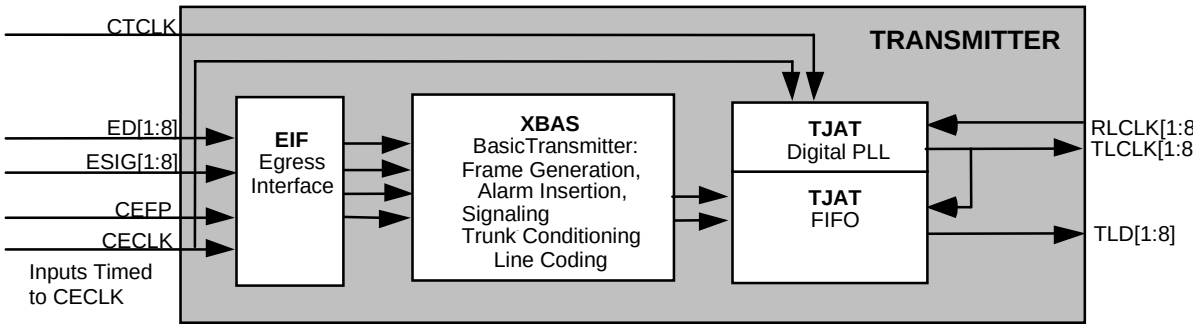
This mode is identical to the full DS1 mode except that the frame alignment is not indicated to the upstream device. Instead, ECLK[x] is gapped on a per DS0 basis so that a subset of the 24 channels in the T1 frame is inserted on ED[x]. Channel insertion is controlled by the IDLE_DS0 bits in the TPSC block's Egress Control Bytes. The framing bit position is always gapped, so the number of ECLK[x] pulses is controllable from 0 to 192 pulses per frame on a per-DS0 basis. The parity functions should not be enabled in NxDS0 mode. The CEFP input is unused in this mode, and has no effect.

Figure 11 - Clock Slave: EFP Enabled



In this mode, the egress interface is clocked by the common egress clock (CECLK). The transmitter is either frame-aligned or superframe-aligned to the common egress frame pulse (CEFP). EFP[x] is configurable to indicate the frame alignment or the superframe alignment of ED[x]. CECLK can be enabled to be a 1.544 MHz clock or a 2.048 MHz clock.

Figure 12 - Clock Slave: External Signaling



In this mode, the egress interface is clocked by the common egress clock (CECLK). The transmitter is either frame-aligned or superframe-aligned to the common egress frame pulse (CEFP). The ESIG[x] contain the robbed-bit signaling data to be inserted into TLD[x], with the four least significant bits of each channel on ESIG[x] representing the signaling state (ABCD or ABAB). EFP[x] is not available in this mode.

9.22 Microprocessor Interface (MPIF)

The Microprocessor Interface allows the TOCTL to be configured, controlled and monitored via internal registers.

10 REGISTER DESCRIPTION

Table 1 - Normal Mode Register Memory Map

Address								Register
#1	#2	#3	#4	#5	#6	#7	#8	
000	080	100	180	200	280	300	380	Receive Line Options
001	081	101	181	201	281	301	381	Ingress Interface Options
002	082	102	182	202	282	302	382	Backplane Parity Configuration and Status
003	083	103	183	203	283	303	383	Receive Interface Configuration
004	084	104	184	204	284	304	384	Transmit Interface Configuration
005	085	105	185	205	285	305	385	Egress Interface Options
006	086	106	186	206	286	306	386	Transmit Framing and Bypass Options
007	087	107	187	207	287	307	387	Transmit Timing Options
008	088	108	188	208	288	308	388	Interrupt Source #1
009	089	109	189	209	289	309	389	Interrupt Source #2
00A	08A	10A	18A	20A	28A	30A	38A	Diagnostics
00B								Master Test
00C								Revision/Chip ID/Global PMON Update
00D	08D	10D	18D	20D	28D	30D	38D	Framer Reset
00E								Interrupt ID
00F	08F	10F	18F	20F	28F	30F	38F	Pattern Generator/Detector Positioning/Control
010	090	110	190	210	290	310	390	RJAT Interrupt Status
011	091	111	191	211	291	311	391	RJAT Reference Clock Divisor (N1) Control
012	092	112	192	212	292	312	392	RJAT Output Clock Divisor (N2) Control
013	093	113	193	213	293	313	393	RJAT Configuration
014-017	094-097	114-117	194-197	214-217	294-297	314-317	394-397	Reserved
018	098	118	198	218	298	318	398	TJAT Interrupt Status
019	099	119	199	219	299	319	399	TJAT Reference Clock Divisor (N1) Control
01A	09A	11A	19A	21A	29A	31A	39A	TJAT Output Clock Divisor (N2) Control
01B	09B	11B	19B	21B	29B	31B	39B	TJAT Configuration
01C	09C	11C	19C	21C	29C	31C	39C	ELST Configuration
01D	09D	11D	19D	21D	29D	31D	39D	ELST Interrupt Enable/Status

01E	09E	11E	19E	21E	29E	31E	39E	ELST Trouble Code
01F	09F	11F	19F	21F	29F	31F	39F	ELST Reserved
020	0A0	120	1A0	220	2A0	320	3A0	FRMR Configuration
021	0A1	121	1A1	221	2A1	321	3A1	FRMR Interrupt Enable
022	0A2	122	1A2	222	2A2	322	3A2	FRMR Interrupt Status
023	0A3	123	1A3	223	2A3	323	3A3	FRMR Reserved
024	0A4	124	1A4	224	2A4	324	3A4	Reserved
025	0A5	125	1A5	225	2A5	325	3A5	Reserved
026	0A6	126	1A6	226	2A6	326	3A6	Reserved
027	0A7	127	1A7	227	2A7	327	3A7	Clock Monitor
028	0A8	128	1A8	228	2A8	328	3A8	Reserved
029	0A9	129	1A9	229	2A9	329	3A9	Reserved
02A	0AA	12A	1AA	22A	2AA	32A	3AA	RBOC Enable
02B	0AB	12B	1AB	22B	2AB	32B	3AB	RBOC Code Status
02C	0AC	12C	1AC	22C	2AC	32C	3AC	ALMI Configuration
02D	0AD	12D	1AD	22D	2AD	32D	3AD	ALMI Interrupt Enable
02E	0AE	12E	1AE	22E	2AE	32E	3AE	ALMI Interrupt Status
02F	0AF	12F	1AF	22F	2AF	32F	3AF	ALMI Alarm Detection Status
030	0B0	130	1B0	230	2B0	330	3B0	TPSC Configuration
031	0B1	131	1B1	231	2B1	331	3B1	TPSC µP Access Status
032	0B2	132	1B2	232	2B2	332	3B2	TPSC Channel Indirect Address/Control
033	0B3	133	1B3	233	2B3	333	3B3	TPSC Channel Indirect Data Buffer
034	0B4	134	1B4	234	2B4	334	3B4	TDPR Configuration
035	0B5	135	1B5	235	2B5	335	3B5	TDPR Upper Transmit Threshold
036	0B6	136	1B6	236	2B6	336	3B6	TDPR Lower Transmit Threshold
037	0B7	137	1B7	237	2B7	337	3B7	TDPR Interrupt Enable
038	0B8	138	1B8	238	2B8	338	3B8	TDPR Interrupt Status/ UDR Clear
039	0B9	139	1B9	239	2B9	339	3B9	TDPR Transmit Data
03A	0BA	13A	1BA	23A	2BA	33A	3BA	TDPR Reserved
03B	0BB	13B	1BB	23B	2BB	33B	3BB	TDPR Reserved
03C	0BC	13C	1BC	23C	2BC	33C	3BC	IBCD Configuration
03D	0BD	13D	1BD	23D	2BD	33D	3BD	IBCD Interrupt Enable/Status
03E	0BE	13E	1BE	23E	2BE	33E	3BE	IBCD Activate Code

03F	0BF	13F	1BF	23F	2BF	33F	3BF	IBCD Deactivate Code
040	0C0	140	1C0	240	2C0	340	3C0	SIGX Configuration
041	0C1	141	1C1	241	2C1	341	3C1	SIGX µP Access Status/ Signaling State Change Channels 17-24
042	0C2	142	1C2	242	2C2	342	3C2	SIGX Channel Indirect Address/Control/ Signaling State Change Channels 9-16
043	0C3	143	1C3	243	2C3	343	3C3	SIGX Channel Indirect Data Buffer/ Signaling State Change Channels 1-8
044	0C4	144	1C4	244	2C4	344	3C4	XBAS Configuration
045	0C5	145	1C5	245	2C5	345	3C5	XBAS Alarm Transmit
046	0C6	146	1C6	246	2C6	346	3C6	XIBC Control
047	0C7	147	1C7	247	2C7	347	3C7	XIBC Loopback Code
048	0C8	148	1C8	248	2C8	348	3C8	PMON Reserved
049	0C9	149	1C9	249	2C9	349	3C9	PMON Interrupt Enable/Status
04A	0CA	14A	1CA	24A	2CA	34A	3CA	PMON BEE Count (LSB)
04B	0CB	14B	1CB	24B	2CB	34B	3CB	PMON BEE Count (MSB)
04C	0CC	14C	1CC	24C	2CC	34C	3CC	PMON FER Count (LSB)
04D	0CD	14D	1CD	24D	2CD	34D	3CD	PMON FER Count (MSB)
04E	0CE	14E	1CE	24E	2CE	34E	3CE	PMON OOF Count
04F	0CF	14F	1CF	24F	2CF	34F	3CF	PMON COFA Count
050	0D0	150	1D0	250	2D0	350	3D0	RPSC Configuration
051	0D1	151	1D1	251	2D1	351	3D1	RPSC µP Access Status
052	0D2	152	1D2	252	2D2	352	3D2	RPSC Channel Indirect Address/Control
053	0D3	153	1D3	253	2D3	353	3D3	RPSC Channel Indirect Data Buffer
054	0D4	154	1D4	254	2D4	354	3D4	RDLC Configuration
055	0D5	155	1D5	255	2D5	355	3D5	RDLC Interrupt Control
056	0D6	156	1D6	256	2D6	356	3D6	RDLC Status
057	0D7	157	1D7	257	2D7	357	3D7	RDLC Data
058	0D8	158	1D8	258	2D8	358	3D8	RDLC Primary Address Match
059	0D9	159	1D9	259	2D9	359	3D9	RDLC Secondary Address Match
05A	0DA	15A	1DA	25A	2DA	35A	3DA	RDLC Reserved
05B	0DB	15B	1DB	25B	2DB	35B	3DB	RDLC Reserved
05C	0DC	15C	1DC	25C	2DC	35C	3DC	XBOC Reserved
05D	0DD	15D	1DD	25D	2DD	35D	3DD	XBOC Code

05E	0DE	15E	1DE	25E	2DE	35E	3DE	Reserved
05F	0DF	15F	1DF	25F	2DF	35F	3DF	Reserved
060	0E0	160	1E0	260	2E0	360	3E0	PRGD Control
061	0E1	161	1E1	261	2E1	361	3E1	PRGD Interrupt Enable/Status
062	0E2	162	1E2	262	2E2	362	3E2	PRGD Length
063	0E3	163	1E3	263	2E3	363	3E3	PRGD Tap
064	0E4	164	1E4	264	2E4	364	3E4	PRGD Error Insertion
065-067	0E5-0E7	165-167	1E5-1E7	265-267	2E5-2E7	365-367	3E5-3E7	PRGD Reserved
068	0E8	168	1E8	268	2E8	368	3E8	PRGD Pattern Insertion #1
069	0E9	169	1E9	269	2E9	369	3E9	PRGD Pattern Insertion #2
06A	0EA	16A	1EA	26A	2EA	36A	3EA	PRGD Pattern Insertion #3
06B	0EB	16B	1EB	26B	2EB	36B	3EB	PRGD Pattern Insertion #4
06C	0EC	16C	1EC	26C	2EC	36C	3EC	PRGD Pattern Detector #1
06D	0ED	16D	1ED	26D	2ED	36D	3ED	PRGD Pattern Detector #2
06E	0EE	16E	1EE	26E	2EE	36E	3EE	PRGD Pattern Detector #3
06F	0EF	16F	1EF	26F	2EF	36F	3EF	PRGD Pattern Detector #4
070-07F	0F0-0FF	170-17F	1F0-1FF	270-27F	2F0-2FF	370-37F	3F0-3FF	Reserved
400-7FF								Reserved for Test

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TOCTL. Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

Notes on Normal Mode Register Bits:

1. Although the register bit descriptions for the eight framers have been combined, each framer is completely independent of the others.

2. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

3. All configuration bits that can be written into can also be read back. This allows the processor controlling the TOCTL to determine the programming state of the chip.

4. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

5. Writing into read-only normal mode register bit locations does not affect TOCTL operation unless otherwise noted.

Registers 000H, 080H, 100H, 180H, 200H, 280H, 300H, 380H: Receive Line Options

Bit	Type	Function	Default
Bit 7	R/W	FIFOBYP	0
Bit 6	R/W	UNF	0
Bit 5	R/W	IBCD_IDLE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	AUTOYELLOW	0
Bit 2	R/W	AUTORED	0
Bit 1	R/W	AUTOOOF	0
Bit 0	R/W	AUTOUPDATE	0

These registers allow software to configure the receive functions of each framer.

FIFOBYP:

The FIFOBYP bit enables the receive line data to be bypassed around the RJAT FIFO to the ingress outputs. When jitter attenuation is not being used, the RJAT FIFO can be bypassed to reduce the delay through the receiver section by typically 24 bits. When FIFOBYP is set to logic 1, the RJAT FIFO is bypassed. When FIFOBYP is set to logic 0, the receive line data passes through the RJAT FIFO.

UNF:

The UNF bit allows the framer to operate with unframed DS-1 data. When UNF is set to logic 1, the FRMR is disabled and the recovered data passes through the receiver section of the framer without frame or channel alignment. While UNF is held at logic 1, the Alarm Integrator continues to operate and detects and integrates AIS alarm, the SIGX holds its signaling frozen, and the AUTO_OOF function, if enabled, will consider OOF to be declared. When UNF is set to logic 0, the framer operates normally, searching for frame alignment on the incoming data.

IBCD_IDLE:

Setting the IBCD_IDLE bit gaps the data to the IBCD block during the framing bit. This allows the IBCD to be used to detect the idle code in the receive

DS1 stream. The IBCD must still be programmed to detect the desired pattern, and otherwise operates unchanged.

Reserved

Reserved for future use.

AUTOYELLOW:

When the AUTOYELLOW bit is set to logic 1, then whenever ALMI declares a Red alarm in the ingress direction, XBAS will transmit a Yellow alarm in the egress direction. When AUTOYELLOW is set to logic 0, XBAS will only transmit a Yellow alarm when the XYEL bit is set in the XBAS Alarm Transmit Register (reg. 045H, 0C5H, 145H, 1C5H, 245H, 2C5H, 345H, 3C5H). Note that the Red alarm from ALMI is not deasserted on detection of AIS.

AUTORED:

The AUTORED bit allows global trunk conditioning to be applied to the ingress data stream, ID[x], immediately upon declaration of Red carrier failure alarm. When AUTORED is set to logic 1, the data on ID[x] for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC while Red CFA is declared. When AUTORED is set to logic 0, the ingress data is not automatically conditioned when Red CFA is declared.

AUTOOOF:

The AUTOOOF bit allows global trunk conditioning to be applied to the ingress data stream, ID[x], immediately upon declaration of out of frame (OOF). When AUTOOOF is set to logic 1, then while OOF is declared, the data on ID[x] for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC. When AUTOOOF is set to logic 0, the ingress data is not automatically conditioned by RPSC when OOF is declared. However, if the ELST is not bypassed, then the ELST trouble code will still be inserted in channel data while OOF is declared. RPSC data and signaling trunk conditioning overwrites the ELST trouble code.

AUTOUPDATE

When AUTOUPDATE is logic 1, the PMON and PRGD registers in the appropriate framer are automatically updated once every 8000 receive frame periods, i.e. once a second, timed to the receive line. If the INTE bit is set in the PMON Interrupt/Enable register, then the PMON will interrupt the microprocessor as soon as the results are available in the PMON registers. The results will then be available for reading for the next second, until they are overwritten by the next update. The OVR bit in the PMON Interrupt/Enable register indicates such an overwrite by going to logic 1.

When AUTOUPDATE is logic 1, the microprocessor can still initiate additional updates by writing to any of the PMON counter registers or to the Revision/Chip ID/Global PMON Update register (register 00CH), but care should be taken not to initiate a second update in a given PMON before the first is completed, which can lead to unpredictable results.

Similarly, the XFERE bit in the PRGD Interrupt Enable/Status Register may be set, allowing the PRGD to interrupt the microprocessor when a PRGD update has been completed. PRGD and PMON perform updates in the same number of clock cycles, so only one of the two interrupts need be enabled. The OVR bit in the same register indicates that data has been overwritten without being read. As is the case for the PMON, additional updates of the PRGD may be initiated by the microprocessor via the Revision/Chip ID/Global PMON Update register, and care must be taken to avoid initiating an update while another update is in progress.

Registers 001H, 081H, 101H, 181H, 201H, 281H, 301H, 381H: Ingress Interface Options

Bit	Type	Function	Default
Bit 7	R/W	IMODE[1]	1
Bit 6	R/W	IMODE[0]	1
Bit 5	R/W	ICLKSEL	0
Bit 4	R/W	CICLK2M	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ISFP	0
Bit 1	R/W	ALTIFP	0
Bit 0	R/W	IMTKC	0

These registers allow software to configure the ingress interface format of each framer.

IMODE[1:0]:

These bits configure the ingress interface as shown below:

IMODE[1:0]	Mode
00	Clock Master: NxDS0
01	Clock Master: Full DS1
10	Clock Slave: ICLK Reference
11	Clock Slave: External Signaling

ICLKSEL:

The ICLKSEL bit is active when the Clock Slave: ICLK Reference mode is enabled, and the ICLK[x] pin is used as a timing reference When ICLKSEL is a logic 1, ICLK[x] is a jitter attenuated version of the 1.544 MHz receive line clock, RLCLK[x]. When ICLKSEL is a logic 0, ICLK[x] is an 8 kHz timing reference that is generated by dividing the jitter attenuated version of RLCLK[x] by 193.

CICLK2M:

The CICLK2M bit selects the 2.048 MHz backplane data rate. When CICLK2M is set to logic 1, the clock rate on the CICLK input is expected to be 2.048MHz and the data stream on ID[x] is output as 1 byte of "filler" followed by 3 bytes of channel data, repeated 8 times. When CICLK2M is set to logic 0, the backplane data rate and format is identical to T1 (i.e. 1.544MHz rate with 24 contiguous channel bytes followed by 1 framing bit). The 2.048 MHz backplane function is not available when the Clock Master modes are active, and CICLK2M MUST BE SET TO LOGIC 0 when these modes are enabled. The HSBPSEL bit in the Timing Options Register (007H, 087H, 107H, 187H, 207H, 287H, 307H, 387H) must be set to logic 1 whenever CICLK2M is set to logic 1.

Reserved

Reserved for future use.

ISFP:

The ISFP bit selects the output signal seen on IFP[x]. When set to logic 1, the IFP[x] output pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF. When ISFP is set to logic 0, the IFP[x] output pulses high during each framing bit (i.e. every 193 bits).

ALTIFP:

The ALTIFP bit suppresses every second output pulse on the backplane output IFP[x]. When ALTIFP is set to logic 1, the output signal on IFP[x] pulses every 386 bits, indicating every second framing bit (if the ISFP bit is logic 0); or the output signal on IFP[x] pulses every 24 or 48 frames (if the ISFP bit is logic 1). This latter setting (i.e. both ALTIFP and ISFP set to logic 1) is useful for converting SF formatted data to ESF formatted data between two TOCTL devices. When ALTIFP is set to logic 0, the output signal on IFP[x] pulses in accordance to the ISFP bit setting.

IMTKC:

The IMTKC bit allows global trunk conditioning to be applied to the received data and signaling streams, ID[x] and ISIG[x]. When IMTKC is set to logic 1, the data on ID[x] for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC; similarly, the signaling data on ISIG[x] for each channel is replaced with the data contained in the signaling trunk conditioning registers. When IMTKC is set to logic 0, the data and signaling signals are modified on a per-DS0 basis in accordance with the control bits contained in the per-DS0 control registers within the RPSC.

Registers 002H, 082H, 102H, 182H, 202H, 282H, 302H, 382H: Backplane Parity Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	EPTYP	0
Bit 6	R/W	EPRTYE	0
Bit 5	R	EDI	X
Bit 4	R	ESIGI	X
Bit 3	R/W	PTY_EXTD	0
Bit 2		Unused	X
Bit 1	R/W	IPTYP	0
Bit 0	R/W	IPRTYE	0

These registers provide control and status reporting of data integrity checking on the ingress and egress interfaces. A single parity bit in the F-bit position represents parity over the previous frame (including the undefined bit positions). If a 2.048 Mbit/s backplane rate is selected, the parity calculation is performed over all bit positions, including the undefined positions. Signaling parity is similarly calculated over all bit positions. Parity checking and generation is not supported when the NxDS0 mode is active.

EPTYP:

The egress parity type (EPTYP) bit sets even or odd parity in the egress streams. If EPTYP is a logic zero, then the expected parity value in the F-bit position of ED[x] and ESIG[x] is even, thus it is a one if the number of ones in the previous frame is odd. If EPTYP is a logic one, then the expected parity value in the F-bit position of ED[x] and ESIG[x] is odd, thus it is a one if the number of ones in the previous frame is even.

EPRTYE:

The EPRTYE bit enables transmit parity interrupts. When set a logic one, parity errors on inputs ED[x] and ESIG[x] are indicated by the EDI and ESIGI bits, respectively, and by the INTB output. When set to logic zero, parity errors are indicated by the EDI and ESIGI status bits but are not indicated on the INTB output.

EDI:

The EDI bit indicates if a parity error has been detected on the ED[x] input. This bit is cleared when this register is read. Odd or even parity is selected by the EPTYP bit.

ESIGI:

The ESIGI bit indicates if a parity error has been detected on the ESIG[x] input. This bit is cleared when this register is read. Odd or even parity is selected by the EPTYP bit. This bit is invalid when the external signaling mode is inactive.

PTY_EXTD:

The Parity Extend bit (PTY_EXTD) causes both ingress and egress parity to be calculated over the previous frame plus the previous parity bit, instead of only the previous frame. The intended use of this bit is when 1.544 MHz ingress/egress interfaces are selected, when the parity is ordinarily calculated over the previous 192 bits. Setting PTY_EXTD causes parity to be calculated over the previous 193 bits, including the previous parity bit, so that odd parity (if chosen) will be calculated over an odd number of bits, and thus may detect either stuck-at-one or stuck-at-zero conditions on the ID[x], ED[x], ISIG[x] and ESIG[x] connections.

IPTYP:

The ingress parity type (IPTYP) bit sets even or odd parity in the ingress streams. If IPTYP is a logic zero, then the parity value in the F-bit position of ID[x] and ISIG[x] is even, thus it is a one if the number of ones in the previous frame is odd. If IPTYP is a logic one, then the parity value in the F-bit position of ID[x] and ISIG[x] is odd, thus it is a one if the number of ones in the previous frame is even. IPTYP only has effect if IPRTYE is a logic one.

IPRTYE:

The IPRTYE bit enables ingress parity insertion. When set a logic one, parity is inserted into the F-bit position of the ID[x] and ISIG[x] streams. When set to logic zero, the F-bit passes through transparently.

Registers 003H, 083H, 103H, 183H, 203H, 283H, 303H, 383H: Receive Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	ICLKRISE	0
Bit 2	R/W	RLCLKFALL	0
Bit 1	R/W	CIFPFALL	0
Bit 0	R/W	CICLKRISE	0

These registers select the active clock edges of the receive line and ingress interfaces.

ICLKRISE:

The ICLKRISE bit enables the ingress interface to be updated on the rising ICLK[x] edge. When ICLKRISE is set to logic 1, ID[x] and IFP[x] are updated on the rising ICLK[x] edge. When ICLKRISE is set to logic 0, ID[x] and IFP[x] are updated on the falling ICLK[x] edge. This register bit has no effect when the Clock Slave ingress modes are enabled.

RLCLKFALL:

The RLCLKFALL bit enables the receive line interface to be sampled on the falling RLCLK[x] edge. When RLCLKFALL is set to logic 1, RLD[x] is sampled on the falling RLCLK[x] edge. When RLCLKFALL is set to logic 0, RLD[x] is sampled on the rising RLCLK[x] edge.

CIFPFALL:

The CIFPFALL bit enables the common ingress frame pulse to be sampled on the falling CICLK edge. When CIFPFALL is set to logic 1, CIFP is sampled on the falling CICLK edge. When CIFPFALL is set to logic 0, CIFP is sampled on the rising CICLK edge. This bit must be set to the same value in all eight registers for proper operation.

CICLKRISE:

The CICLKRISE bit enables the ingress interface to be updated on the rising CICLK edge. When CICLKRISE is set to logic 1, ID[x], ISIG[x] and IFP[x] are updated on the rising CICLK edge. When CICLKRISE is set to logic 0, ID[x], ISIG[x] and IFP[x] are updated on the falling CICLK edge. This register bit has no effect when the Clock Master ingress modes are enabled.

Registers 004H, 084H, 104H, 184H, 204H, 284H, 304H. 384H: Transmit Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	FIFOBYP	0
Bit 6	R/W	TAISEN	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	CECLKFALL	0
Bit 2	R/W	EFPRISE	0
Bit 1	R/W	ECLKFALL	0
Bit 0	R/W	TLCLKRISE	0

These registers select the active clock edges of the transmit line and egress interfaces.

FIFOBYP:

The FIFOBYP bit enables the egress data to be bypassed around the TJAT FIFO to the transmit line outputs. When jitter attenuation is not being used, the TJAT FIFO can be bypassed to reduce the delay through the transmitter section by typically 24 bits. When FIFOBYP is set to logic 1, the TJAT FIFO is bypassed. When FIFOBYP is set to logic 0, the egress data passes through the TJAT FIFO. The TJAT FIFO is always bypassed when the Clock Master egress modes are active, so the FIFOBYP bit should not be set while EMODE[1] is logic 0.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TLD[x] pin. When TAISEN is set to logic 1, the unipolar TLD[x] output is forced to all-ones. When TAISEN is set to logic 0, the TLD[x] output operates normally.

CECLKFALL :

The CECLKFALL bit enables the egress interface to be sampled on the falling CECLK edge. When CECLKFALL is set to logic 1, ED[x], ESIG[x] and CEFP are sampled on the falling CECLK edge. When CECLKFALL is set to logic 0,

ED[x], ESIG[x] and CEFP are sampled on the rising CECLK edge. This register bit has no effect when the Clock Master egress modes are selected.

EFPRISE :

The EFPRISE bit enables the egress frame pulse to be updated on the rising CECLK edge. When EFPRISE is set to logic 1, EFP[x] is updated on the rising CECLK edge. When EFPRISE is set to logic 0, EFP[x] is updated on the falling CECLK edge. This register bit is only active when Clock Slave: EFP Enabled mode is selected.

ECLKFALL:

The ECLKFALL bit enables the egress data to be sampled on the falling ECLK[x] edge. When ECLKFALL is set to logic 1, ED[x] is sampled on the falling ECLK[x] edge. When ECLKFALL is set to logic 0, ED[x] is sampled on the rising ECLK[x] edge. This register bit only active when Clock Master: NxDS0 mode is selected.

TLCLKRISE:

The TLCLKRISE bit enables the transmit line interface to be updated on the rising TLCLK[x] edge. When TLCLKRISE is set to logic 1, TLD[x] is updated on the rising TLCLK[x] edge. When TLCLKRISE is set to logic 0, TLD[x] is updated on the falling TLCLK[x] edge.

Registers 005H, 085H, 105H, 185H, 205H, 285H, 305H, 385H: Egress Options

Bit	Type	Function	Default
Bit 7	R/W	EMODE[1]	1
Bit 6	R/W	EMODE[0]	1
Bit 5		Unused	X
Bit 4	R/W	ABXXEN	0
Bit 3		Unused	X
Bit 2	R/W	CECLK2M	0
Bit 1	R/W	CESFP	0
Bit 0	R/W	ESFP	0

These registers allow software to configure the egress interface format of each framer.

EMODE[1:0]:

These bits configure the egress interface as shown below:

EMODE[1:0]	Mode
00	Clock Master: NxDS0
01	Clock Master: Full DS1
10	Clock Slave: EFP Enabled
11	Clock Slave: External Signaling

When EMODE[1:0] = 0X, then the SYNC bit in the TJAT Configuration Register must be set to logic 0.

ABXXEN:

The ABXXEN bit selects the format of the ESIG[x] transmit signaling input signal. When ABXXEN is set to logic 1, ESIG[x] is expected to contain only the A and B signaling bits in the upper two bit positions of the lower nibble of each channel (i.e. ABXX), with the lower two bit positions being "Don't Cares". When ABXXEN is set to logic 0, ESIG[x] is expected to contain all four signaling bit in the lower nibble of each channel (i.e. ABCD), or it is expected to contain the A and B bits duplicated in the lower nibble (i.e. ABAB).

CECLK2M:

The CECLK2M bit selects the 2.048 MHz data rate and format of the egress data. When CECLK2M is set to logic 1, the clock rate on the CECLK input is expected to be 2.048 MHz and the data stream on ED[x] and ESIG[x] is expected to be formatted as 1 byte of "filler" followed by 3 bytes of channel data, repeated 8 times. The format is precisely laid out in the Functional Timing Diagrams section. When CECLK2M is set to logic 0, the egress data rate and format is identical to T1 (i.e. 1.544MHz rate with 24 contiguous channel bytes followed by 1 framing bit). When CECLK2M is set to logic 1, then the SYNC bit must be set to logic 0 in the TJAT Configuration register (Registers 01BH, 09BH, 11BH, 19BH, 21BH, 29BH, 31BH, 39BH.) and the HSBPSEL bit in the Timing Options Register (007H, 087H, 107H, 187H, 207H, 287H, 307H, 387H) must be set to logic 1. PLLREF[1:0] should not be set to 01 in the Timing Options Register unless the TJAT divisors are specifically set to divide the 2048 kHz clock down to the line rate. CECLK2M MUST BE SET TO LOGIC 0 WHEN THE CLOCK MASTER MODES ARE SELECTED.

CESFP:

The CESFP bit selects the type of egress frame alignment signal, CEFP. When CESFP is set to logic 1, a pulse on CEFP indicates the **LAST** F-bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the XBAS). When CESFP is set to logic 0, a pulse on CEFP indicates each framing bit. CESFP should be set to logic 1 when the external signaling mode is active to ensure that the egress superframe is aligned to the transmit line superframe.

ESFP:

The ESFP bit selects the output signal seen on EFP[x]. When set to logic 1, the EFP[x] output pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF. When ESFP is set to logic 0, the EFP[x] output pulses high during each framing bit (i.e. every 193 bits).

Registers 006H, 086H, 106H, 186H, 206H, 286H, 306H, 386H: Transmit Framing and Bypass Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SIGAEN	0
Bit 4	R/W	TXSIGA	0
Bit 3	R/W	FDIS	0
Bit 2	R/W	FBITBYP	0
Bit 1	R/W	CRCBYP	0
Bit 0	R/W	FDLBYP	0

These registers allow software to configure the bypass options of the transmitter.

SIGAEN:

When set to logic 1, the SIGA is inserted into the signaling bit data path before the XBAS. In this position, it will take a snapshot of the ESIG[x] stream during frame 1 of each superframe, and use those signaling values for the remainder of the superframe. This ensures signaling bit integrity in systems which do not specify or track the superframe alignment of XBAS. When SIGAEN is set to logic 1, the TXSIGA bit should also be set to logic 1. When SIGAEN is set to logic 0, the SIGA is removed from the circuit.

TXSIGA:

The TXSIGA bit is reserved, and should be set to logic 1 whenever SIGAEN is set to logic 1.

FDIS:

The FDIS bit allows the framing generation through the XBAS to be disabled and the egress data to pass through the XBAS unchanged. When FDIS is set to logic 1, XBAS is disabled from generating framing. When FDIS is set to logic 0, XBAS is enabled to generate and insert the framing into the transmit data.

FBITBYP:

The FBITBYP bit allows the frame synchronization bit in the egress stream, ED[x], to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FBITBYP is set to logic 1, the input frame synchronization bit is re-inserted into the output data stream. When FBITBYP is set to logic 0, the XBAS is allowed to generate the output frame synchronization bits.

CRCBYP:

The CRCBYP bit allows the framing bit corresponding to the CRC-6 bit position in the egress stream, ED[x], to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When CRCBYP is set to logic 1, the input CRC-6 bit is re-inserted into the output data stream. When CRCBYP is set to logic 0, the XBAS is allowed to generate the output CRC-6 bits.

FDLBYP:

The FDLBYP bit allows the framing bit corresponding to the facility data link bit position in the egress data stream, ED[x], to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FDLBYP is set to logic 1, the input FDL bit is re-inserted into the output data stream. When FDLBYP is set to logic 0, the XBAS is allowed to generate the output FDL bit.

Registers 007H, 087H, 107H, 187H, 207H, 287H, 307H, 387H: Transmit Timing Options

Bit	Type	Function	Default
Bit 7	R/W	HSBPSEL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	OCLKSEL	0
Bit 3	R/W	PLLREF1	0
Bit 2	R/W	PLLREF0	1
Bit 1	R/W	CTCLKSEL	0
Bit 0	R/W	SMCLKO	0

These registers allow software to configure the options of the transmit timing section.

HSBPSEL:

The HSBPSEL bit selects the source of the high-speed clock used in the ELST, SIGX, TPSC, and RPSC blocks. This allows the TOCTL to interface to higher rate backplanes (>2.048MHz, externally gapped, or 2.048MHz, internally gapped). Note, however, that the externally gapped instantaneous backplane clock frequency must not exceed 3.0MHz. When HSBPSEL is set to logic 1, the 37.056MHz XCLK input signal is divided by 2 and used as the high-speed clock to these blocks. XCLK must be driven with 37.056MHz. When HSBPSEL is set to logic 0, XCLK input signal is divided by 3 and used as the high-speed clock to these blocks.

OCLKSEL:

The OCLKSEL bit selects the source of the Transmit Digital Jitter Attenuator FIFO output clock signal. When OCLKSEL is set to logic 1, the TJAT FIFO output clock is driven with the CTCLK input clock, and the SYNC bit must be set to logic 0 in the TJAT Configuration Register (Registers 01BH, 09BH, 11BH, 19BH, 21BH, 29BH, 31BH, 39BH.) When OCLKSEL is set to logic 0, the TJAT FIFO output clock is driven with the internal smooth 1.544MHz clock selected by the CTCLKSEL and SMCLKO bits.

PLLREF1, PLLREF0:

The PLLREF[1:0] bits select the source of the Transmit Digital Jitter Attenuator phase locked loop reference signal as follows:

PLLREF1	PLLREF0	Source of PLL Reference
0	0	Transmit clock used by XBAS when the Clock Slave egress modes are active. (either the 1.544MHz CECLK or the gapped clock derived from the 2.048MHz CECLK as selected by CECLK2M)
0	1	CECLK input
1	0	RLCLK[x] input
1	1	CTCLK input

PLLREF[1:0] = 00 when the Clock Master egress modes are active is a reserved setting, and should not be used.

CTCLKSEL,SMCLKO:

The CTCLKSEL and SMCLKO bits select the source of the internal smooth 1.544MHz output clock signals. When CTCLKSEL and SMCLKO are set to logic 0, the internal 1.544MHz clock signal is driven by the smooth 1.544MHz clock source generated by TJAT. When CTCLKSEL is set to logic 0 and SMCLKO is set to logic 1, the internal 1.544MHz clock signal is driven by the CTCLK input signal divided by 8. When CTCLKSEL and SMCLKO are set to logic 1, the internal 1.544MHz clock signal is driven by the XCLK input signal divided by 24. The combination of CTCLKSEL set to logic 1 and SMCLKO set to logic 0 should not be used.

The following table provides examples of the most common combinations of settings:

Table 2 - Typical Transmit Timing Configurations

Mode Description	Bit Settings	Transmit Line Clock Options
Default Setting Clock Slave: External Signaling Egress data timed to CECLK TJAT FIFO decouples the Egress interface (timed to CECLK) from the Transmit Line side (timed to jitter-attenuated TLCLK[x]). The TJAT PLL is used to generate TLCLK[x] from a reference clock.	EMODE[1:0] = 11 HSBPSEL =0 OCLKSEL =0 CTCLKSEL =0 SMCLKO =0 CECLK2M =0	When PLLREF[1:0]=0X, TLCLK[x] is a jitter-attenuated clock referenced to CECLK. This is the default. When PLLREF[1:0]=10, TLCLK[x] is a jitter-attenuated clock referenced to RLCLK[x] When PLLREF[1:0]=11, TLCLK[x] is a jitter-attenuated clock referenced to CTCLK[x]
Clock Slave: EFP Enabled Egress data timed to CECLK TJAT FIFO decouples the Egress interface (timed to CECLK) from the Transmit Line side (timed to jitter-attenuated TLCLK[x]). The TJAT PLL is used to generate TLCLK[x] from a reference clock.	EMODE[1:0] = 10 HSBPSEL =0 OCLKSEL =0 CTCLKSEL =0 SMCLKO =0 CECLK2M =0	When PLLREF[1:0]=0X, TLCLK[x] is a jitter-attenuated clock referenced to CECLK. When PLLREF[1:0]=10, TLCLK[x] is a jitter-attenuated clock referenced to RLCLK[x] When PLLREF[1:0]=11, TLCLK[x] is a jitter-attenuated clock referenced to CTCLK

Mode Description	Bit Settings	Transmit Line Clock Options
Clock Slave with 2.048 MHz CECLK. Egress data timed to internally-gapped CECLK. TJAT FIFO decouples the Egress interface (timed to gapped CECLK) from the Transmit Line side (timed to jitter-attenuated TLCLK[x]). The TJAT PLL is used to generate TLCLK[x] from a reference clock.	EMODE[1:0] = 1X HSBPSEL =1 OCLKSEL =0 CTCLKSEL =0 SMCLKO =0 CECLK2M =1	When PLLREF[1:0]=00, TLCLK[x] is a jitter-attenuated clock referenced to the internally gapped CECLK. See note 1. When PLLREF[1:0]=01, TLCLK[x] is a jitter-attenuated clock referenced to CECLK. See note 2. When PLLREF[1:0]=10, TLCLK[x] is a jitter-attenuated clock referenced to RLCLK[x] When PLLREF[1:0]=11, TLCLK[x] is a jitter-attenuated clock referenced to CTCLK
Clock Slave with Egress data timed to an **externally gapped CECLK**. TJAT FIFO decouples the Egress interface (timed to CECLK) from the Transmit Line side (timed to jitter-attenuated TLCLK[x]). The TJAT PLL is used to generate TLCLK[x] from a reference clock.	EMODE[1:0] = 1X HSBPSEL =1 OCLKSEL =0 CTCLKSEL =0 SMCLKO =0 CECLK2M =0	When PLLREF[1:0]=0X, TLCLK[x] is a jitter-attenuated clock referenced to CECLK. See note 2. When PLLREF[1:0]=10, TLCLK[x] is a jitter-attenuated clock referenced to RLCLK[x] When PLLREF[1:0]=11, TLCLK[x] is a jitter-attenuated clock referenced to CTCLK

Mode Description	Bit Settings	Transmit Line Clock Options
Clock Slave with Egress data timed to CECLK. CECLK may be a normal, internally gapped, or externally gapped clock as shown in previous examples. TJAT FIFO decouples the Egress interface (timed to CECLK) from the Transmit Line side (timed to TLCLK[x]). **The TJAT PLL is unused**. The SYNC, CENT, and LIMIT in the TJAT configuration must be set to logic 0.	EMODE[1:0] = 1X HSBPSEL =* PLLREF[1:0] =XX CECLK2M =* * See note 3	When OCLKSEL = 1, TLCLK[x] = CTCLK. When OCLKSEL = 0, SMCLKO = 1, and CTCLKSEL =0, then TLCLK[x] = CTCLK÷8. When OCLKSEL = 0, SMCLKO = 1, and CTCLKSEL =1, then TLCLK[x] = XCLK÷24.
Clock Slave with Egress data timed to 1.544 MHz CECLK. **TJAT FIFO is bypassed**, so that TLCLK[x] is directly driven by CECLK.	EMODE[1:0] = 1X HSBPSEL =0 FIFOBYP =1 OCLKSEL =X PLLREF[1:0] =XX CTCLKSEL =0 SMCLKO =0 CECLK2M =0	

Mode Description	Bit Settings	Transmit Line Clock Options
Clock Master: Full DS1 or NxDS0. Egress data is clocked by TLCLK[x], and TJAT FIFO is automatically bypassed. In NxDS0 mode, a gapped version of TLCLK[x] is provided on ECLK[x], which only clocks during the desired channels. The TJAT PLL is used to generate TLCLK[x] from a reference clock.	EMODE[1:0] = 0X HSBPSEL =0 FIFOBYP =0 OCLKSEL =0 CTCLKSEL =0 SMCLKO =0 CECLK2M =0	The setting PLLREF[1:0]=00 is reserved and should not be used. When PLLREF[1:0]=01, TLCLK[x] is a jitter-attenuated clock referenced to CECLK. When PLLREF[1:0]=10, TLCLK[x] is a jitter-attenuated clock referenced to RLCLK[x] When PLLREF[1:0]=11, TLCLK[x] is a jitter-attenuated clock referenced to CTCLK
Clock Master: Full DS1 or NxDS0 Egress data is clocked by TLCLK[x], and TJAT FIFO is automatically bypassed. In NxDS0 mode, a gapped version of TLCLK[x] is provided on ECLK[x], which only clocks during the desired channels. The **TJAT PLL is unused**.	EMODE[1:0] = 0X HSBPSEL =0 FIFOBYP =0 CECLK2M =0 PLLREF[1:0] =XX	When OCLKSEL = 1, TLCLK[x] = CTCLK. When OCLKSEL = 0, SMCLKO = 1, and CTCLKSEL =0, then TLCLK[x] = CTCLK÷8. When OCLKSEL = 0, SMCLKO = 1, and CTCLKSEL =1, then TLCLK[x] = XCLK÷24.

Notes:

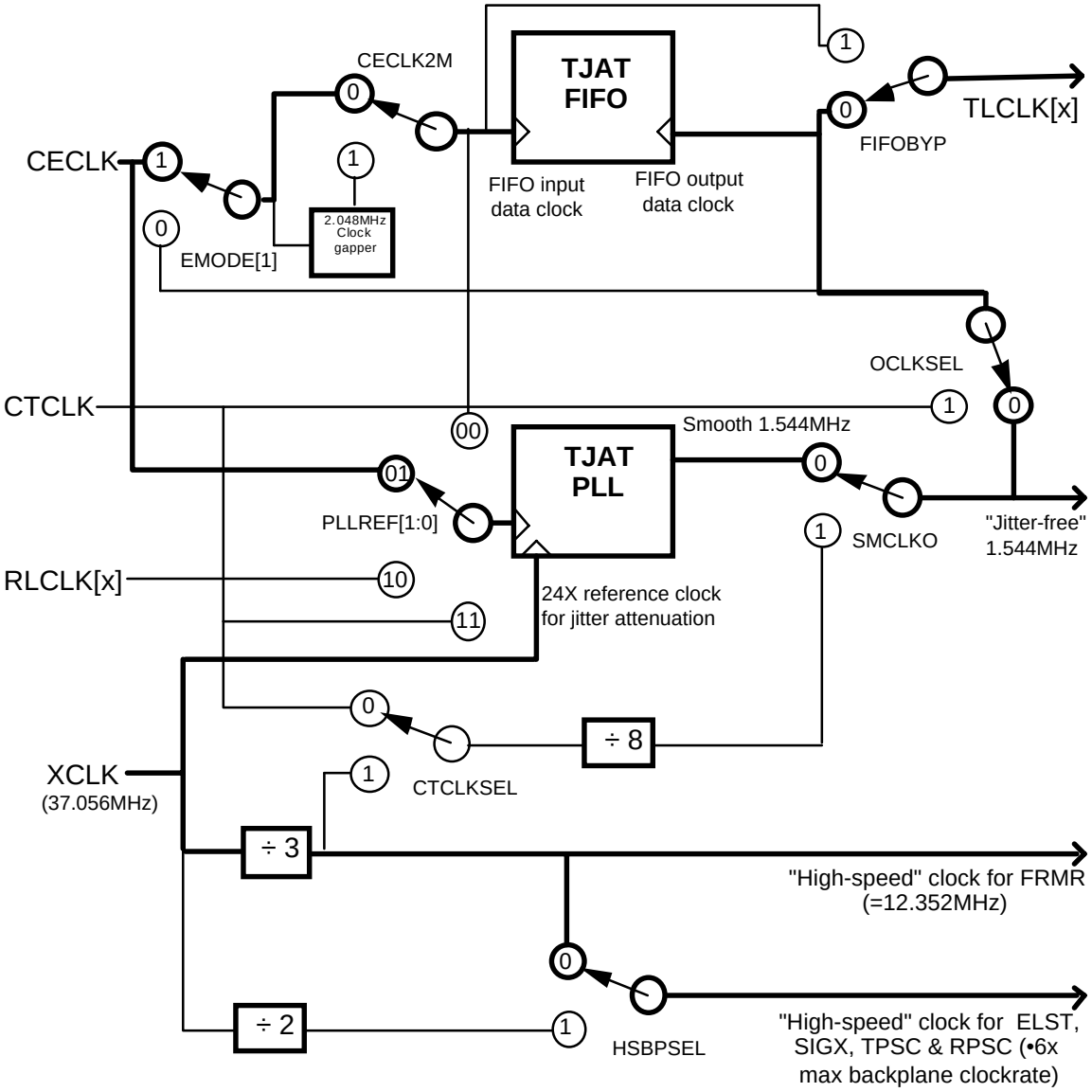
1. When the internally gapped clock is used as the TJAT PLL reference, the TJAT divisors N1 and N2 should both be set to C0H.

2. When an externally gapped clock is used as the TJAT PLL reference, the TJAT divisors N1 and N2 should be set so that the gapping vanishes. If the gapping introduces no 8kHz jitter, then a setting of C0H (representing division by 193) will be acceptable.

3. Whenever CECLK is used and is not a regular 1.544 MHz clock, HSBPSEL must be set to logic 1. If internal gapping of CECLK is desired, CECLK2M must be set as well.

Figure 13 illustrates the various bit setting options, with the reset condition highlighted.

Figure 13 - Transmit Timing Options



Registers 008H, 088H, 108H, 188H, 208H, 288H, 308H, 388H: Interrupt Source #1

Bit	Type	Function	Default
Bit 7	R	PMON	0
Bit 6	R	IBCD	0
Bit 5	R	FRMR	0
Bit 4	R	PRGD	0
Bit 3	R	ELST	0
Bit 2	R	RDLC	0
Bit 1	R	RBOC	0
Bit 0	R	ALMI	0

These registers allow software to determine the block which produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Registers 009H, 089H, 109H, 189H, 209H, 289H, 309H, 389H: Interrupt Source #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PRTY	0
Bit 5	R	TJAT	0
Bit 4	R	RJAT	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	TDPR	0
Bit 0	R	SIGX	0

These registers allow software to determine the block which produced the interrupt on the INTB output pin.

The PRTY bit indicates a pending parity error indication needs servicing in the Backplane Parity Configuration and Status register.

Reading these registers does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Registers 00AH, 08AH, 10AH, 18AH, 20AH, 28AH, 30AH, 38AH: Master Diagnostics

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	LINELB	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	DDLB	0
Bit 1	R/W	TXMFP	0
Bit 0	R/W	TXDIS	0

These registers allow software to enable the diagnostic mode of each framer.

LINELB:

The LINELB bit selects the line loopback mode, where the receive line clock and data, RLCLK[x] and RLD[x] (with or without jitter attenuation by the RJAT block) are internally connected to the transmit line interface, TLCLK[x] and TLD[x]. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. DDLB and LINELB are mutually incompatible and should not be simultaneously enabled.

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the transmit line interface, TLCLK[x] and TD[x] are internally connected to the receive line interface, RLCLK[x] and RD[x]. When DDLB is set to logic 1, the diagnostic digital loopback mode is enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled. DDLB and LINELB are mutually incompatible and should not be simultaneously enabled.

TXMFP:

The TXMFP bit introduces a mimic framing pattern in the digital output of the basic transmitter by forcing a copy of the current framing bit into bit location 1 of the frame, thereby creating a mimic pattern in the bit position immediately following the correct framing bit. When TXMFP is set to logic 1, the mimic

framing pattern is generated. When TXMFP is set to logic 0, no mimic pattern is generated.

TXDIS:

The TXDIS bit provides a method of suppressing the output of the basic transmitter. When TXDIS is set to logic 1, the digital output of XBAS is disabled by forcing it to logic 0. When TXDIS is set to logic 0, the digital output of XBAS is not suppressed.

Register 00BH: TOCTL Master Test

Bit	Type	Function	Default
Bit 7	R/W	A_TM[9]	X
Bit 6	R/W	A_TM[8]	X
Bit 5	R/W	A_TM[7]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select TOCTL test features. All bits, except for PMCTST and A_TM[9:7] are reset to zero by a hardware reset of the TOCTL; a software reset of the TOCTL does not affect the state of the bits in this register. Refer to the Test Features Description section for more information.

A_TM[9]:

The state of the A_TM[9] bit internally replaces the input address line A[9] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[8]:

The state of the A_TM[8] bit internally replaces the input address line A[8] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[7]:

The state of the A_TM[7] bit internally replaces the input address line A[7] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the TOCTL for PMC's manufacturing tests. When PMCTST is set to logic 1, the TOCTL microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high (IOTST must be set to logic 1 since CSB high resets PMCTST) causes the TOCTL to drive the data bus and holding the CSB pin low tristates the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the TOCTL for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tristate modes of the TOCTL . While the HIZIO bit is a logic 1, all output pins of the TOCTL except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Register 00CH: TOCTL Revision/Chip ID/Global PMON Update

Bit	Type	Function	Default
Bit 7	R	TYPE[2]	0
Bit 6	R	TYPE[1]	1
Bit 5	R	TYPE[0]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

The version identification bits, ID[4:0], are set to a fixed value representing the version number of the TOCTL. ID = 0H indicates Revision C. ID = 1H indicates Revision E.

The chip identification bits, TYPE[2:0], are set to binary 010 representing the TOCTL.

Writing to this register causes all performance monitor and pattern generator/detector counters to be updated simultaneously.

Registers 00DH, 08DH, 10DH, 18DH, 20DH, 28DH, 30DH, 38DH: Framer Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

The RESET bit implements a software reset. If the RESET bit is a logic 1, the individual framer is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the framer out of reset. Holding the framer in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Register 00EH: Interrupt ID

Bit	Type	Function	Default
Bit 7	R	INT8	0
Bit 6	R	INT7	0
Bit 5	R	INT6	0
Bit 4	R	INT5	0
Bit 3	R	INT4	0
Bit 2	R	INT3	0
Bit 1	R	INT2	0
Bit 0	R	INT1	0

These registers provide interrupt identification. The T1 framer(s) which caused the INTB output to transition low can be identified by reading this register. The INTx bit is high if the xth framer caused the interrupt. A procedure for identifying the source of an interrupt can be found in the Operations section.

INT8, INT7, INT6, INT5, INT4, INT3, INT2, INT1:

The INTx bit will be high if the xth T1 framer (the T1 framer corresponding to the input pin RLCLK[x]) causes the INTB pin to transition low.

Registers 00FH, 08FH, 10FH, 18FH, 20FH, 28FH, 30FH, 38FH: Pattern Generator/Detector Positioning/Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Nx56k_GEN	0
Bit 3	R/W	Nx56k_DET	0
Bit 2	R/W	RXPATGEN	0
Bit 1	R/W	UNF_GEN	0
Bit 0	R/W	UNF_DET	0

This register modifies the way in which the PRGD is used by the TPSC and RPSC. More information on using PRGD is available in the Operations section.

Nx56k_GEN:

The Nx56k_GEN bit is active when the RPSC or TPSC is used to insert PRBS into selected DS0 channels of the transmit or receive stream. When the Nx56kbps generation bit is set to logic 1, the pattern is only inserted in the first 7 bits of the selected DS0 channels, and gapped on the eighth bit. This is particularly useful when using the jammed-bit-8 zero code suppression in the transmit direction, for instance when sending a Nx56kbps fractional T1 loopback sequence. This bit has no effect when UNF_GEN is set to logic 1.

Nx56k_DET:

The Nx56k_DET bit is active when the RPSC or TPSC is used to detect PRBS in selected DS0 channels of the transmit or receive stream. When the Nx56kbps detection bit is set to logic 1, the pattern generator only looks at the first 7 bits of the selected DS0 channels, and gaps out the eighth bit. This is particularly useful when searching for fractional T1 loopback codes in an Nx56kbps fractional T1 signal. This bit has no effect when UNF_DET is set to logic 1.

RXPATGEN:

The Receive Pattern Generate (RXPATGEN) bit controls the location of the pattern generator/detector. When RXPATGEN is set to logic 1, the pattern generator is inserted in the receive path and the pattern detector is inserted in the transmit path. DS0 channels from the receive line may be overwritten with generated patterns before appearing on the ingress interface, and DS0 channels from the egress interface may be checked for the generated pattern before appearing on the transmit line. When RXPATGEN is set to logic 0, the pattern detector is inserted in the receive path and the pattern generator is inserted in the transmit path. DS0 channels from the egress interface may be overwritten with generated patterns before appearing on the transmit line, and DS0 channels from the receive line may be checked for the generated pattern before appearing on the ingress interface.

UNF_GEN

When the Unframed Pattern Generation bit (UNF_GEN) is set to logic 1 while RXPATGEN = 0, then the PRGD will overwrite all 193 bits in every frame in the transmit direction. Unless signaling and/or framing is disabled, the XBAS will still overwrite the signaling bit positions and/or the framing bit position. The UNF_GEN bit overrides any per-DS0 pattern generation specified in the TPSC. UNF_GEN also overrides idle code insertion and data inversion in the transmit direction, just like the TEST bit in the TPSC. UNF_GEN=1 while RXPATGEN=1 is a reserved setting and should not be used.

UNF_DET

When the Unframed Pattern Detection bit (UNF_DET) is set to logic 1, then the PRGD will search for the pattern in all 193 bits of the egress or receive stream, depending on the setting of RXPATGEN. The UNF_DET bit overrides any per-DS0 pattern detection specified in the TPSC or RPSC.

Registers 010H, 090H, 110H, 190H, 210H, 290H, 310H, 390H: RJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	0
Bit 0	R	UNDI	0

These registers contain the indication of the RJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. The OVRI bit is cleared after this register is read.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. The UNDI bit is cleared after this register is read.

Register 011H, 091H, 111H, 191H, 211H, 291H, 311H, 391H: RJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

These registers define an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the RJAT PLL reference clock input. The REF divisor magnitude, (N1+1), is the ratio between the frequency of REF input and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit in the RJAT Configuration register is high, will also reset the FIFO.

Upon reset of the TOCTL, the default value of N1 is set to decimal 47 (2FH).

Registers 012H, 092H, 112H, 192H, 212H, 292H, 312H, 392H: RJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

These registers define an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the RJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Upon reset of the TOCTL, the default value of N2 is set to decimal 47 (2FH).

Registers 013H, 093H, 113H, 193H, 213H, 293H, 313H, 393H: RJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

These registers control the operation of the RJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

Reserved:

The Reserved bit should be programmed to logic 1 for future compatibility.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. The CENT bit can only be set to logic 1 if the SYNC bit is set to logic 0.

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI. When SYNC is set to logic 1, then the RJAT divisors (N1 and N2) must be set so that N1+1 is a multiple of 48 decimal, and N2+1 is a multiple of 48 decimal.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Registers 018H, 098H, 118H, 198H, 218H, 298H, 318H, 398H: TJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	0
Bit 0	R	UNDI	0

These registers contain the indication of the TJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. The OVRI bit is cleared after this register is read.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. The UNDI bit is cleared after this register is read.

Register 019H, 099H, 119H, 199H, 219H, 299H, 319H, 399H: TJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

These registers define an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the TJAT PLL reference clock input. The REF divisor magnitude, (N1+1), is the ratio between the frequency of REF input and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit in the TJAT Configuration register is high, will also reset the FIFO.

Upon reset of the TOCTL, the default value of N1 is set to decimal 47 (2FH).

Registers 01AH, 09AH, 11AH, 19AH, 21AH, 29AH, 31AH, 39AH: TJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

These registers define an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the TJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Upon reset of the TOCTL, the default value of N2 is set to decimal 47 (2FH).

Registers 01BH, 09BH, 11BH, 19BH, 21BH, 29BH, 31BH, 39BH: TJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

These registers control the operation of the TJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

Reserved:

The Reserved bit should be programmed to logic 1 for future compatibility.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. The CENT bit can only be set to logic 1 if the SYNC bit is set to logic 0.

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI. When using the 2Mbit/s transmit backplane option, the SYNC bit must be set to logic 0. When SYNC is set to logic 1, then the TJAT divisors (N1 and N2) must be set so that N1+1 is a multiple of 48 decimal, and N2+1 is a multiple of 48 decimal. SYNC should only be set to logic 1 when PLLREF[1:0] = 00, the Egress Interface is in a Clock Slave mode, and CECLK2M is logic 0 the Egress Options Register.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Registers 01CH, 09CH, 11CH, 19CH, 21CH, 29CH, 31CH, 39CH: ELST Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	0
Bit 0	R/W	OR	0

These registers control the format of the expected input frame to the ELST and the format of the generated output frame from the ELST.

Reserved:

The Reserved bit must be programmed to logic 0 for proper operation.

IR:

The IR bit selects the input frame format. The IR bit must be cleared to logic 0 to properly handle the T1 frame format being input into the ELST. SETTING IR TO LOGIC 1 IS A RESERVED SETTING AND SHOULD NOT BE USED.

OR:

The OR bit selects the output frame format. The OR bit must be cleared to properly generate the T1 frame format output from the ELST. SETTING OR TO LOGIC 1 IS A RESERVED SETTING AND SHOULD NOT BE USED.

Registers 01DH, 09DH, 11DH, 19DH, 21DH, 29DH, 31DH, 39DH: ELST Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	0
Bit 0	R	SLIPI	0

SLIPE:

The SLIPE bit position enables generation of an interrupt on the microprocessor INTB pin when a slip event occurs.

SLIPI:

The SLIPI bit indicates whether a slip event has occurred since the last read of the Enable/Status register. SLIPI is a logic 1 if a slip has occurred; SLIPI is a logic 0 is no slip has occurred. The SLIPI bit is cleared after the register is read.

SLIPD:

The SLIPD bit indicates the direction of the last slip when SLIPI is a logic 1. If a slip has occurred and the SLIPD bit is a logic 1 then the slip was due to the frame buffer becoming full. If a slip has occurred and the SLIPD bit is a logic 0 then the slip was due to the frame buffer becoming empty.

Registers 01EH, 09EH, 11EH, 19EH, 21EH, 29EH, 31EH, 39EH: ELST Trouble Code

Bit	Type	Function	Default
Bit 7	R/W	D7	1
Bit 6	R/W	D6	1
Bit 5	R/W	D5	1
Bit 4	R/W	D4	1
Bit 3	R/W	D3	1
Bit 2	R/W	D2	1
Bit 1	R/W	D1	1
Bit 0	R/W	D0	1

These registers allow the Trouble Code, transmitted in place of channel data when the framer is out of frame, to be programmed to any 8-bit value. The code is transmitted from MSB (D7) to LSB (D0).

The writing of the trouble code pattern into the register is asynchronous with respect to the clocks within the framer. One channel of trouble code data will always be corrupted if the register is written while the receiver is out of frame.

Registers 020H, 0A0H, 120H, 1A0H, 220H, 2A0H, 320H, 3A0H: FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	M2O[1]	0
Bit 6	R/W	M2O[0]	0
Bit 5	R/W	ESFFA	0
Bit 4	R/W	ESF	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1		Unused	X
Bit 0		Unused	X

These registers select the framing format and the frame loss criteria used by the FRMR.

M2O[1:0]:

The M2O[1:0] bits select the ratio of errored to total framing bits before declaring out of frame in SF, and ESF framing formats. A logic 00 selects 2 of 4 framing bits in error; a logic 01 selects 2 of 5 bits in error; a logic 10 selects 2 of 6 bits in error. A logic 11 in the M2O[1:0] bits is reserved and should not be used.

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the FRMR does not declare inframe while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

ESF:

The ESF bit selects either extended superframe format or standard superframe format. A logic 1 in the ESF bit position selects ESF; a logic 0 selects SF.

Reserved:

The reserved bits must be written with logic 0 for proper operation..

Registers 021H, 0A1H, 121H, 1A1H, 221H, 2A1H, 321H, 3A1H: FRMR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	ACCEL	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	FERE	0
Bit 3	R/W	BEEE	0
Bit 2	R/W	SFEE	0
Bit 1	R/W	MFPE	0
Bit 0	R/W	INFRE	0

These registers select which of the MFP, COFA, FER, BEE, SFE, or INFR events generates an interrupt on the microprocessor INTB pin when their state changes or their event condition is detected.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

COFAE:

The COFAE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the new alignment differs from the previous alignment. When COFAE is set to logic 1, the declaration of a change of frame alignment is allowed to generate an interrupt. When COFAE is set to logic 0, a change in the frame alignment does not generate an interrupt.

FERE:

The FERE bit enables the generation of an interrupt when a framing bit error has been detected. When FERE is set to logic 1, the detection of a framing bit error is allowed to generate an interrupt. When FERE is set to logic 0, any error in the framing bits does not generate an interrupt.

BEEE:

The BEEE bit enables the generation of an interrupt when a bit error event has been detected. A bit error event is defined as a framing bit errors for SF formatted data, and a CRC-6 error for ESF formatted data. When BEEE is set to logic 1, the detection of a bit error event is allowed to generate an interrupt. When BEEE is set to logic 0, bit error events are disabled from generating an interrupt.

SFEE:

The SFEE bit enables the generation of an interrupt when a severely errored framing event has been detected. A severely errored framing event is defined as 2 or more framing bit errors during the current superframe for SF or ESF formatted data. When SFEE is set to logic 1, the detection of a severely errored framing event is allowed to generate an interrupt. When SFEE is set to logic 0, severely errored framing events are disabled from generating an interrupt.

MFPE:

The MFPE bit enables the generation of an interrupt when the frame find circuitry detects the presence of framing bit mimics. The occurrence of a mimic is defined as more than one framing bit candidate following the frame alignment pattern. When MFPE is set to logic 1, the assertion or deassertion of the detection of a mimic is allowed to generate an interrupt. When MFPE is set to logic 0, the detection of a mimic framing pattern is disabled from generating an interrupt.

INFRE:

The INFRE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the framer is now "inframe". When INFRE is set to logic 1, the assertion or deassertion of the "inframe" state is allowed to generate an interrupt. When INFRE is set to logic 0, a change in the "inframe" state is disabled from generating an interrupt.

Registers 022H, 0A2H, 122H, 1A2H, 222H, 2A2H, 322H, 3A2H: FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	0
Bit 6	R	FERI	0
Bit 5	R	BEEI	0
Bit 4	R	SFEI	0
Bit 3	R	MFPI	0
Bit 2	R	INFRI	0
Bit 1	R	MFP	0
Bit 0	R	INFR	0

These registers indicate whether a change of frame alignment, a framing bit error, a bit error event, or a severely errored framing event generated an interrupt. These registers also indicate whether a mimic framing pattern was detected or whether there was a change in the "inframe" state of the frame circuitry.

COFAI,FERI,BEEI,SFEI:

A logic 1 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the occurrence of the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the corresponding event did not generate an interrupt.

MFPI:

A logic 1 in the MFPI status bit position indicates that the assertion or deassertion of the mimic detection indication has generated an interrupt; a logic 0 in the MFPI bit position indicates that no change in the state of the mimic detection indication occurred.

INFRI:

A logic 1 in the INFRI status bit position indicates that a change in the "inframe" state of the frame alignment circuitry generated an interrupt; a logic 0 in the INFRI status bit position indicates that no state change occurred.

MFP,INFR:

The bit position MFP and INFR indicate the current state of the mimic detection and of the frame alignment circuitry.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SFEI, MFPI, and INFRI) are cleared to logic 0 when this register is read.

Registers 027H, 0A7H, 127H, 1A7H, 227H, 2A7H, 327H, 3A7H: Clock Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	XCLKA	0
Bit 3	R	CECLKA	0
Bit 2	R	CTCLKA	0
Bit 1	R	CICLKA	0
Bit 0	R	RLCLKA	0

These registers provide activity monitoring on TOCTL clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. These registers should be read at periodic intervals to detect clock failures.

XCLKA:

The XCLK active bit monitors for low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read.

RLCLKA:

The RLCLK active bit monitors for low to high transitions on the RLCLK[x] input. RLCLKA is set high on a rising edge of RLCLK[x], and is set low when this register is read.

CICLKA:

The CICLK active bit monitors for low to high transitions on the CICLK input. CICLKA is set high on a rising edge of CICLK, and is set low when this register is read.

CTCLKA:

The CTCLK active bit monitors for low to high transitions on the CTCLK input. CTCLKA is set high on a rising edge of CTCLK, and is set low when this register is read.

CECLKA:

The CECLK active bit monitors for low to high transitions on the CECLK input. CECLKA is set high on a rising edge of CECLK, and is set low when this register is read.

Registers 02AH, 0AAH, 12AH, 1AAH, 22AH, 2AAH, 32AH, 3AAH: RBOC Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	BOCE	0

These registers select the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt on a change in code status.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects the "alternate" validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt on the microprocessor INTB pin when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

Registers 02BH, 0ABH, 12BH, 1ABH, 22BH, 2ABH, 32BH, 3ABH: RBOC Code Status

Bit	Type	Function	Default
Bit 7	R	IDLEI	0
Bit 6	R	BOCI	0
Bit 5	R	BOC[5]	1
Bit 4	R	BOC[4]	1
Bit 3	R	BOC[3]	1
Bit 2	R	BOC[2]	1
Bit 1	R	BOC[1]	1
Bit 0	R	BOC[0]	1

These registers indicate the current state value of the BOC[5:0] bits and indicates whether an interrupt was generated by a change in the code value.

IDLEI:

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

BOCI:

The BOCI bit position indicates whether an interrupt was generated by the detection of a valid BOC. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. BOCI is cleared to logic 0 when the register is read.

BOC[5:0]

BOC[5:0] contain the validated 6-bit BOC. BOC[5] corresponds to the MSB of the code; BOC[0] corresponds to the LSB. An all-ones setting indicates that no valid BOC has been received.

Registers 02CH, 0ACH, 12CH, 1ACH, 22CH, 2ACH, 32CH, 3ACH: ALMI Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ESF	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1		Unused	X
Bit 0		Unused	X

These registers allow selection of the framing format to allow operation of the CFA detection algorithms.

ESF:

The ESF bit selects either extended superframe format or standard superframe format. A logic 1 in the ESF bit position selects ESF; a logic 0 bit selects SF.

Reserved:

The reserved bits must be written with logic 0 for proper operation..

Registers 02DH, 0ADH, 12DH, 1ADH, 22DH, 2ADH, 32DH, 3ADH: ALMI Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	FASTD	0
Bit 3	R/W	ACCEL	0
Bit 2	R/W	YELE	0
Bit 1	R/W	REDE	0
Bit 0	R/W	AISE	0

These registers select which of the three CFA's can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

FASTD:

The FASTD bit enables the "fast" deassertion of Red and AIS alarms. When FASTD is set to a logic 1, deassertion of Red alarm occurs within 120 ms of going in frame. Deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in frame. When FASTD is set to a logic 0, Red and AIS alarm deassertion times remain as defined in the ALMI description.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

YELE,REDE,AISE:

A logic 1 in the enable bit positions (YELE, REDE, AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state changes to generate an interrupt. The enable bits are independent; any combination of Yellow, Red, and AIS CFA's can be enabled to generate an interrupt.

Registers 02EH, 0AEH, 12EH, 1AEH 22EH, 2AEH, 32EH, 3AEH: ALMI Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	YELI	0
Bit 4	R	REDI	0
Bit 3	R	AISI	0
Bit 2	R	YEL	0
Bit 1	R	RED	0
Bit 0	R	AIS	0

These registers indicate which of the three CFA's generated an interrupt when their logic state changed in bit positions 5 through 3; and indicate the current state of each CFA in bit positions 2 through 0. A logic 1 in the status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has generated an interrupt; a logic 0 in the status positions indicates that no state change has occurred. Both the status bit positions (bits 5 through 3) and the interrupt generated because of the change in CFA state are cleared to logic 0 when this register is read.

Registers 02FH, 0AFH, 12FH, 1AFH, 22FH, 2AFH, 32FH, 3AFH: ALMI Alarm Detection Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	REDD	X
Bit 1	R	YELD	X
Bit 0	R	AISD	X

These registers indicate the presence or absence of one or more OOF occurrences within the last 40 ms; the presence or absence of the Yellow ALARM signal over the last 40 ms; and indicate the presence or absence of the AIS ALARM signal over the last 60 ms.

REDD:

When REDD is a logic 1, one or more out of frame events have occurred during the last 40 ms interval. When REDD is a logic 0, no out of frame events have occurred within the last 40 ms interval.

YELD:

When YELD is logic 1, a valid Yellow signal was present during the last 40 ms interval. When YELD is logic 0, the Yellow signal was absent during the last 40 ms interval. For each framing format, a valid Yellow signal is deemed to be present if:

- bit 2 of each channel is not logic 0 for 16 or fewer times during the 40 ms interval for SF framing format;
- the 16-bit Yellow bit oriented code is received error-free 8 or more times during the interval for ESF framing format;

AISD:

When AISD is logic 1, a valid AIS signal was present during the last 60 ms interval. When AISD is logic 0, the AIS signal was absent during the last 60

ms interval. A valid AIS signal is deemed to be present during a 60 ms interval if the out of frame condition has persisted for the entire interval and the received PCM data stream is not logic 0 for 126 or fewer times.

Registers 030H, 0B0H, 130H, 1B0H, 230H, 2B0H, 330H, 3B0H: TPSC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

These registers allow selection of the microprocessor read access type and output enable control for the Transmit Per-DS0 Serial Controller. The per-DS0 Serial Controller allows per-DS0 data and signaling trunk alignment, idle code, zero code suppression, data inversion, DS0 loopback from the ingress stream, channel insertion, and the detection or generation of pseudo-random or repetitive patterns. More information on using the TPSC can be found in the Operations section.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TOCTL is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-DS0 functions. When the PCCE bit is set to a logic 1, each channel's Egress Control byte, IDLE Code byte, and SIGNALING Control byte are enabled. When the PCCE bit is set to logic 0, the per-DS0 functions are disabled.

Registers 031H, 0B1H, 131H, 1B1H, 231H, 2B1H, 331H, 3B1H: TPSC µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 032H, 0B2H, 132H, 1B2H, 232H, 2B2H, 332H, 3B2H: TPSC Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

These registers allow the µP to access the internal TPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal TPSC register is requested; when R/WB is set to a logic 0, a write to the internal TPSC register is requested.

Registers 033H, 0B3H, 133H, 1B3H, 233H, 2B3H, 333H, 3B3H: TPSC Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

These registers contain either the data to be written into the internal TPSC registers when a write request is initiated or the data read from the internal TPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal TPSC registers control the per-DS0 functions on the egress data, provide the per-DS0 transmit idle code, and provide the per-DS0 transmit signaling control and the alternate signaling bits. The functions are allocated within the registers as follows:

Table 3 - TPSC Indirect Memory Map

01H	Egress Control byte for Channel 1
02H	Egress Control byte for Channel 2
• •	• •
17H	Egress Control byte for Channel 23
18H	Egress Control byte for Channel 24

19H	IDLE Code byte for Channel 1
1AH	IDLE Code byte for Channel 2
• •	• •
2FH	IDLE Code byte for Channel 23
30H	IDLE Code byte for Channel 24
31H	SIGNALING Control byte for Channel 1
32H	SIGNALING Control byte for Channel 2
• •	• •
47H	SIGNALING Control byte for Channel 23
48H	SIGNALING Control byte for Channel 24

The bits within each control byte are allocated as follows:

TPSC Internal Registers 01-18H: Egress Control byte

Bit	Type	Function	Default
Bit 7	R/W	INVERT	
Bit 6	R/W	IDLE_DS0	
Bit 5	R/W	DMW	
Bit 4	R/W	SIGNINV	
Bit 3	R/W	TEST	
Bit 2	R/W	LOOP	
Bit 1	R/W	ZCS0	
Bit 0	R/W	ZCS1	

INVERT:

When the INVERT bit is set to a logic 1, data from the ED[x] input is inverted for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit from the ED[x] input is inverted for that channel.

The INVERT and SIGNINV can be used to produce the following types of inversions:

INVERT	SIGNINV	Effect on PCM Channel Data
0	0	PCM Channel data is unchanged
1	0	All 8 bits of the PCM channel data are inverted
0	1	Only the MSB of the PCM channel data is inverted (SIGN bit inversion)
1	1	All bits EXCEPT the MSB of the PCM channel data is inverted (Magnitude inversion)

IDLE_DS0:

When the IDLE_DS0 bit is set to a logic 1, data from the IDLE Code Byte replaces the ED[x] input data for the duration of that channel.

When the NxDS0 mode is active, IDLE_DS0 also controls the generation of ECLK[x]. When IDLE_DS0 is a logic 0, data is inserted from the egress interface during that channel, and eight clock pulses are generated on ECLK[x]. When IDLE_DS0 is a logic 1, an IDLE code byte is inserted, and ECLK[x] is suppressed for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the ED[x] input data for the duration of that channel.

TEST:

When the TEST bit is set to a logic 1, channel data from the ED[x] input is either overwritten with a test pattern from the PRGD block or is routed to the PRGD block and compared against an expected test pattern. The RXPATGEN bit in the Pattern Generator/Detector Positioning/Control register determines whether the egress data is overwritten or compared as shown in the following table:

TEST	RXPATGEN	Description
0	X	Channel data is not included in test pattern
1	1	Channel data is routed to PRGD and compared against expected test pattern
1	0	Channel data is overwritten with PRGD test pattern

All the channels that are routed to the PRGD are concatenated and treated as a continuous stream in which pseudorandom or repetitive sequences are searched for. Similarly, all channels set to be overwritten with PRGD test pattern data are treated such that if the channels are subsequently extracted and concatenated, the PRBS or repetitive sequence appears in the concatenated stream. Pattern generation/detection can be enabled to work on only the first 7 bits of a channel (for Nx56 kbps fractional T1) using the Nx56k_DET and Nx56k_GEN bits in the Pattern Generator/Detector Positioning/Control register (Reg. 00FH, 08FH, 10FH, 18FH, 20FH, 28FH, 30FH, 38FH). THe PRGD can also be enabled to work on the entire DS1, including framing bits, using the UNF_GEN and UNF_DET bits in the Pattern Generator/Detector Positioning/Control register.

LOOP:

The LOOP bit enables the DS0 loopback. When the LOOP bit is set to a logic 1, egress data is overwritten with the corresponding channel data from the

receive line. When the Clock Master ingress modes are enabled, the elastic store is used to align the receive line data to the egress frame. When the Clock Slave ingress modes are enabled, however, the elastic store is unavailable to facilitate per-DS0 loopacks, and loopback functionality is provided only when the Egress Interfaces is also in a Clock Slave mode, and ingress and egress clocks and frame alignment are identical (CICLK=CECLK, CIFP=CEFP).

Data inversion, idle, loopback and test pattern insertion/checking are performed independent of the transmit framing format. DS0 loopback takes precedence over digital milliwatt pattern insertion. Next in priority is test pattern insertion, which, in turn, takes precedence over idle code insertion. Data inversion has the lowest priority. When test pattern checking is enabled, the egress data is compared before DS0 loopback, digital milliwatt pattern insertion, idle code insertion or data inversion is performed. None of this prioritizing has any effect on the gapping of ECLK in NxDS0 mode. That is, if both DS0 loopback and idle code insertion are enabled for a given channel while in NxDS0 mode, the DS0 will be looped-back, will not be overwritten with idle code, and ECLK will be gapped out for the duration of the channel. Similarly, none of the prioritizing has any effect on the generation of test patterns from the PRGD, only on the insertion of that pattern. Thus, if both DMW and TEST are set for a given DS0, and RXPATGEN = 0, then the test pattern from the PRGD will be overwritten with the digital milliwatt code. This same rule also applies to test patterns inserted via the UNF_GEN bit in the Pattern Generator/Detector Positioning/Control register.

ZCS0,ZCS1:

The ZCS0 and ZCS1 bits select the zero code suppression used as follows. With the exception of the “Jammed bit 8” setting, the ZCS[1:0] bits are logically ORed with the ZCS[1:0] bits in the XBAS Configuration register:

ZCS0	ZCS1	Description
0	0	No Zero Code Suppression
0	1	“Jammed bit 8" - Every bit 8 is forced to a one. This may be used for 56kbit/s data service.
1	0	GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.)
1	1	Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.)

TPSC Internal Registers 19-30H: IDLE Code byte

Bit	Type	Function	Default
Bit 7	R/W	IDLE7	
Bit 6	R/W	IDLE6	
Bit 5	R/W	IDLE5	
Bit 4	R/W	IDLE4	
Bit 3	R/W	IDLE3	
Bit 2	R/W	IDLE2	
Bit 1	R/W	IDLE1	
Bit 0	R/W	IDLE0	

The contents of the IDLE Code byte register is substituted for the channel data on ED[x] when the IDLE_DS0 bit in the Egress Control byte is set to a logic 1. The IDLE Code is transmitted from MSB (IDLE7) to LSB (IDLE0).

TPSC Internal Registers 31-48H: SIGNALING Control byte

Bit	Type	Function	Default
Bit 7	R/W	SIGC0	
Bit 6	R/W	SIGC1	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	A'	
Bit 2	R/W	B'	
Bit 1	R/W	C'	
Bit 0	R/W	D'	

Signaling insertion is controlled by the SIGC[1:0] bits. The source of the signaling bits is determined by SIGC0: when SIGC0 is set to a logic 1, signaling data is taken from the A', B', C', and D' bits; when SIGC0 is set to logic 0, signaling data is taken from the A,B,C, and D bit locations on the ESIG[x] input. Signaling insertion is controlled by SIGC1: when SIGC1 is set to a logic 1, insertion of signaling bits is enabled; when SIGC1 is set to logic 0, the insertion of signaling bits is disabled. For SF format, the C' and D' or C and D bits from Signaling Control byte or ESIG[x], respectively, are inserted into the A and B signaling bit positions of every second superframe that is transmitted. It is assumed that C=A and D=B.

Register 034H, 0B4H, 134H, 1B4H, 234H, 2B4H ,334H, 3B4H: TDPR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of XCLK.

EN:

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN bit is set to logic 0, the TDPR is disabled and an all 1's Idle sequence is transmitted on the datalink.

CRC:

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the Transmit Data register is transmitted. The FIFO is then reset. All data in the FIFO will

be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is cleared upon a write to the TDPR Transmit Data register (039H, 0B9H, 139H, 1B9H, 239H, 2B9H, 339H, 3B9H).

Reserved:

This bit should be programmed to logic 0 for proper operation.

FIFOCLR:

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHARE:

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, then separate closing and opening flags are inserted between successive frames.

Register 035H, 0B5H, 135H, 1B5H, 235H, 2B5H ,335H, 3B5H: TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]:

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 036H, 0B6H, 136H, 1B6H, 236H, 2B6H ,336H, 3B6H: TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]:

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], the LFILLI and BLFILL bits will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 037H, 0B7H, 137H, 1B7H, 237H, 2B7H ,337H, 3B7H: TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE:

The LFILLE enables a transition to logic 1 on LFILLI to generate an interrupt on INTB. If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB. If LFILLE is a logic 0, a transition to logic 1 on LFILLI will not generate an interrupt on INTB.

UDRE:

The UDRE enables a transition to logic 1 on UDRI to generate an interrupt on INTB. If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB. If UDRE is a logic 0, a transition to logic 1 on UDRI will not generate an interrupt on INTB.

OVRE:

The OVRE enables a transition to logic 1 on OVRI to generate an interrupt on INTB. If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB. If OVRE is a logic 0, a transition to logic 1 on OVRI will not generate an interrupt on INTB.

FULLE:

The FULLE enables a transition to logic 1 on FULLI to generate an interrupt on INTB. If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB. If FULLE is a logic 0, a transition to logic 1 on FULLI will not generate an interrupt on INTB.

Reserved:

This bit should be set to logic 0 for proper operation.

Register 038H, 0B8H, 138H, 1B8H, 238H, 2B8H ,338H, 3B8H: TDPR Interrupt Status /UDR Clear

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Reserved	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Writing to this register will clear the underrun condition if it has occurred.

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of XCLK.

LFILLI:

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 if LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI:

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 if UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI:

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 if OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI:

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 if FULLE is programmed to logic 1. FULLI is cleared when this register is read.

Reserved:

This bit is not used in TOCTL applications, and should be set to logic 0 for proper operation.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL:

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 039H, 0B9H, 139H, 1B9H, 239H, 2B9H ,339H, 3B9H: TDPR Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of XCLK.

TD[7:0]:

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Registers 03CH, 0BCH, 13CH, 1BCH, 23CH, 2BCH, 33CH, 3BCH: IBCD Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	DSEL1	0
Bit 2	R/W	DSEL0	0
Bit 1	R/W	ASEL1	0
Bit 0	R/W	ASEL0	0

These registers provide the selection of the Activate and De-activate loopback code lengths (from 3 bits to 8 bits) as follows:

DEACTIVATE Code		ACTIVATE Code		CODE LENGTH
DSEL1	DSEL0	ASEL1	ASEL0	
0	0	0	0	5 bits
0	1	0	1	6 (or 3*) bits
1	0	1	0	7 bits
1	1	1	1	8 (or 4*) bits

***Note:**

3 and 4 bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

The Reserved bit must be programmed to logic 0 for normal operation.

Registers 03DH, 0BDH, 13DH, 1BDH, 23DH, 2BDH, 33DH, 3BDH: IBCD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R	LBACP	0
Bit 6	R	LBDCP	0
Bit 5	R/W	LBAE	0
Bit 4	R/W	LBDE	0
Bit 3	R	LBAI	0
Bit 2	R	LBDI	0
Bit 1	R	LBA	0
Bit 0	R	LBD	0

LBACP,LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval.

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the microprocessor INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the microprocessor INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI,LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes generated the interrupt when their state changed. A logic 1 in these bit positions indicate that a state change in that code has generated an interrupt; a logic 0 in these bit positions indicate that no state change has occurred.

LBA,LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicate the presence of that code has been detected; a logic 0 in these bit positions indicate the absence of that code.

Registers 03EH, 0BEH, 13EH, 1BEH, 23EH, 2BEH, 33EH, 3BEH: IBCD Activate Code

Bit	Type	Function	Default
Bit 7	R/W	ACT7	0
Bit 6	R/W	ACT6	0
Bit 5	R/W	ACT5	0
Bit 4	R/W	ACT4	0
Bit 3	R/W	ACT3	0
Bit 2	R/W	ACT2	0
Bit 1	R/W	ACT1	0
Bit 0	R/W	ACT0	0

This 8 bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 00001, then the first 8 bits of two repetitions (0000100001) is programmed into the register, i.e.00001000. Note that bit ACT7 corresponds to the first code bit received.

Registers 03FH, 0BFH, 13FH, 1BFH, 23FH, 2BFH, 33FH, 3BFH: IBCD Deactivate Code

Bit	Type	Function	Default
Bit 7	R/W	DACT7	0
Bit 6	R/W	DACT6	0
Bit 5	R/W	DACT5	0
Bit 4	R/W	DACT4	0
Bit 3	R/W	DACT3	0
Bit 2	R/W	DACT2	0
Bit 1	R/W	DACT1	0
Bit 0	R/W	DACT0	0

This 8 bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 001, then the first 8 bits of three repetitions (001001001) is programmed into the register, i.e.00100100. Note that bit DACT7 corresponds to the first code bit received.

Registers 040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H: SIGX Configuration (COSS=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	COSS	0
Bit 5	R/W	SIGE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESF	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

These registers allow selection of the framing format, the microprocessor access type, and allows enabling of the per-DS0 configuration registers. The bits in this register are valid when the COSS bit is a logic 0. The reserved bits must be set to logic 0 for correct operation.

SIGE:

The SIGE bit enables a change of signaling state in any of the 24 channels to generate an interrupt on the INTB pin. When SIGE is set to logic 1, a change of signaling state in any channel generates an interrupt. When SIGE is set to logic 0, the interrupt is disabled.

COSS:

The COSS bit allows the channels to be polled to determine in which channel(s) the signaling state has changed. When COSS is a logic 1, the SIGX register space is configured to allow the change of signaling state event bits to be read. When COSS is a logic 0, the SIGX register space is configured to allow indirect access to the configuration and signaling data registers for each of the 24 channels.

ESF:

The ESF bit selects either extended superframe format standard superframe formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit selects SF.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TOCTL is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-DS0 functions. When the PCCE bit is set to a logic 1, bit fixing and signaling debouncing are performed on a per-DS0 basis. When the PCCE bit is logic 0, the per-DS0 functions are disabled.

Registers 040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H: SIGX Configuration (COSS=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	COSS	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

COSS:

The COSS bit allows the channels to be polled to determine in which channel(s) the signaling state has changed. When COSS is a logic 1, the SIGX register space is configured to allow the change of signaling state event bits to be read. When COSS is a logic 0, the SIGX register space is configured to allow indirect access to the configuration and signaling data registers for each of the 24 channels.

Registers 041H, 0C1H, 141H, 1C1H, 241H, 2C1H, 341H, 3C1H: SIGX µP Access Status (COSS=0)

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns. The bits in this register are valid when the COSS bit is a logic 0.

Registers 041H, 0C1H, 141H, 1C1H, 241H, 2C1H, 341H, 3C1H: SIGX Signaling State Change Channels 17-24 (COSS=1)

Bit	Type	Function	Default
Bit 7	R	COSS[24]	X
Bit 6	R	COSS[23]	X
Bit 5	R	COSS[22]	X
Bit 4	R	COSS[21]	X
Bit 3	R	COSS[20]	X
Bit 2	R	COSS[19]	X
Bit 1	R	COSS[18]	X
Bit 0	R	COSS[17]	X

The bits in this register are valid when the COSS bit is a logic 1.

COSS[24:17]:

The COSS[24:17] bits indicate a signaling state change in channels 17 - 24. A logic 1 in a bit position indicates a change of signaling state in the corresponding channel since the last time this register was read; a logic 0 in a bit position indicates that no signaling state change has occurred. These bits are cleared when this register is read.

Registers 042H, 0C2H, 142H, 1C2H, 242H, 2C2H, 342H, 3C2H: SIGX Channel Indirect Address/Control (COSS=0)

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

These registers allow the µP to access to internal SIGX registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to one of these registers with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal SIGX register is requested, when R/WB is set to a logic 0, an write to the internal SIGX register is requested. The bits in this register are valid when the COSS bit is a logic 0.

Registers 042H, 0C2H, 142H, 1C2H, 242H, 2C2H, 342H, 3C2H: SIGX Signaling State Change Channels 9-16 (COSS=1)

Bit	Type	Function	Default
Bit 7	R	COSS[16]	X
Bit 6	R	COSS[15]	X
Bit 5	R	COSS[14]	X
Bit 4	R	COSS[13]	X
Bit 3	R	COSS[12]	X
Bit 2	R	COSS[11]	X
Bit 1	R	COSS[10]	X
Bit 0	R	COSS[9]	X

The bits in this register are valid when the COSS bit is a logic 1.

COSS[16:9]:

The COSS[16:9] bits indicate a signaling state change in channels 9 - 16. A logic 1 in a bit position indicates a change of signaling state in the corresponding channel since the last time this register was read; a logic 0 in a bit position indicates that no signaling state change has occurred. These bits are cleared when this register is read.

Registers 043H, 0C3H, 143H, 1C3H, 243H, 2C3H, 343H, 3C3H: SIGX Channel Indirect Data Buffer (COSS = 0)

Bit	Type	Function	Default
Bit 7	R/W	D7	X
Bit 6	R/W	D6	X
Bit 5	R/W	D5	X
Bit 4	R/W	D4	X
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

These registers contain either the data to be written into the internal SIGX registers when a write request is initiated or the data read from the internal SIGX registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data bits.

Registers 043H, 0C3H, 143H, 1C3H, 243H, 2C3H, 343H, 3C3H: SIGX Signaling State Change Channels 1-8 (COSS=1)

Bit	Type	Function	Default
Bit 7	R	COSS[8]	X
Bit 6	R	COSS[7]	X
Bit 5	R	COSS[6]	X
Bit 4	R	COSS[5]	X
Bit 3	R	COSS[4]	X
Bit 2	R	COSS[3]	X
Bit 1	R	COSS[2]	X
Bit 0	R	COSS[1]	X

The bits in this register are valid when the COSS bit is a logic 1.

COSS[8:1]:

The COSS[8:1] bits indicate a signaling state change in channels 1 - 8. A logic 1 in a bit position indicates a change of signaling state in the corresponding channel since the last time this register was read; a logic 0 in a bit position indicates that no signaling state change has occurred. These bits are cleared when this register is read.

The internal registers of the SIGX control the per-DS0 functions on the ingress signaling data and allow the µP to read the channel's current signaling state. The address bit A6 selects whether a channel's configuration data register is to be accessed (A6=1) or whether a channel's signaling data register is to be accessed. The channel registers are allocated within the SIGX as follows:

Table 4 - SIGX Indirect Memory Map

20H	Channel 1 Signaling Data
21H	Channel 2 Signaling Data
•	•
•	•
36H	Channel 23 Signaling Data
37H	Channel 24 Signaling Data
38-3FH	Ignored
40H	Channel 1 Per-DS0 Configuration Data
41H	Channel 2 Per-DS0 Configuration Data
42H	Channel 3 Per-DS0 Configuration Data
•	•
•	•
56H	Channel 23 Per-DS0 Configuration Data
57H	Channel 24 Per-DS0 Configuration Data
58-5FH	Ignored

The bits within each channel register byte are allocated as follows:

SIGX Internal Registers 20-37H: Signaling Data

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	A
Bit 2	R	B
Bit 1	R	C
Bit 0	R	D

When the Signaling Data registers are read, the byte returned contains the 4 signaling bits in the 4 least significant bit positions. If SF framing format is selected then C=A and D=B. The bits read correspond to the signaling state extracted from the third to last superframe received.

When reading the extracted signaling data for a channel with signaling state debounce enabled, the signaling data returned is the debounced version, meaning that the signaling state value for that channel must have been the same for two consecutive superframes before it was allowed to propagate through the signaling buffers and be visible in the signaling data registers. If the state was not the same, the current state (accessible via these registers) is not changed.

Signaling data is not available for one full signaling multi-frame after the COSS[x] indication is available. If the signaling data is needed in the same signaling multi-frame that the COSS indication is available, the following registers can be read.

TimeSlot	SIGX Address	Bit Mask	Timeslot	SIGX Address	Bit Mask
1	10H	F0H	17	10H	0FH
2	11H	F0H	18	11H	0FH
⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	23	16H	0FH
⋮	⋮	⋮	24	17H	0FH
15	1EH	F0H	Reserved		
16	1FH	F0H			

SIGX Internal Registers 40-57H: Per-DS0 Configuration Data

Bit	Type	Function
Bit 7	R/W	Unused
Bit 6	R/W	Unused
Bit 5	R/W	Unused
Bit 4	R/W	Unused
Bit 3	R/W	Unused
Bit 2	R/W	FIX
Bit 1	R/W	POL
Bit 0	R/W	DEB

FIX:

The FIX bit controls whether the signaling bit (the least significant bit of the DS0 channel on ID[x] during each signaling frame) is fixed to the polarity specified by the POL bit. A logic 1 in the FIX position enables bit fixing; a logic 0 in the FIX position disables bit fixing. Note that the RPSC functions (inversion, digital milliwatt code insertion, trunk conditioning, and PRBS detection or insertion) take place after bit fixing.

POL:

The POL bit selects the logic level the signaling bit is fixed to when bit fixing is enabled. When POL is a logic 1, the signaling is fixed to logic 1. When POL is a logic 0, the signaling is fixed to logic 0.

DEB:

The DEB bit controls whether a channel's signaling bits are to be debounced. Debouncing requires that the signaling bits be in the same state for two successive superframes before the signaling bits are changed to that state.

Registers 044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H: XBAS Configuration

Bit	Type	Function	Default
Bit 7	R/W	MTRK	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	ESF	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ZCS1	0
Bit 0	R/W	ZCS0	0

MTRK:

The MTRK bit forces trunk conditioning, idle code substitution and signaling conditioning, on all channels when MTRK is a logic 1. This has the same effect as setting the IDLE_DS0 bit in the Egress Control byte and the SIG0 bit in the Signaling Control byte for all channels, except that the ECLK[x] output is unaffected in NxDS0 mode. Signalling conditioning only occurs if SIGC[1] is logic 1 in the TPSC Internal Signaling Control register for the channel in question.

ESF:

The ESF bit selects either Extended Superframe format or standard superframe format. A logic 1 selects ESF, a logic 0 selects SF.

ZCS[1:0]:

The ZCS[1:0] bits select the Zero Code Suppression format to be used. These bits are logically ORed with the ZCS[1:0] bits in the TPSC per-DS0 Egress Control byte. The bits are encoded as follows:

ZCS1	ZCS0	Zero Code Suppression Format
0	0	None

ZCS1	ZCS0	Zero Code Suppression Format
0	1	GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.)
1	0	Reserved (do not use)
1	1	Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.)

Reserved:

The reserved bits must be set to logic 0 for correct operation.

Registers 045H, 0C5H, 145H, 1C5H, 245H, 2C5H, 345H, 3C5H: XBAS Alarm Transmit

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	XYEL	0
Bit 0	R/W	Reserved	0

These registers control the transmission of Yellow alarm.

XYEL:

The XYEL bit enables the XBAS to generate a Yellow alarm in the appropriate framing format. When XYEL is set to logic 1, framer is enabled to set bit 2 of each channel to logic 0 for SF format, or the framer is enabled to transmit repetitions of 1111111100000000 (the Yellow Alarm BOC) on the FDL for ESF format. When XYEL is set to logic 0, XBAS is disabled from generating the Yellow alarm.

Registers 046H, 0C6H, 146H, 1C6H, 246H, 2C6H, 346H, 3C6H: XIBC Control

Bit	Type	Function	Default
Bit 7	R/W	EN	0
Bit 6	R/W	UF	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	CL1	0
Bit 0	R/W	CL0	0

EN:

The EN bit controls whether the Inband Code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

UF:

The UF bit controls whether the code is transmitted framed or unframed. A logic 1 in the UF bit position selects unframed inband code transmission; a logic 0 in the UF bit position selects framed inband code transmission. Note: the UF register bit controls the XBAS directly and is not qualified by the EN bit. When UF is set to logic 1, the XBAS is disabled and no framing is inserted regardless of the setting of EN. The UF bit should only be written to logic 1 when the EN bit is set, and should be cleared to logic 0 when the EN bit is cleared.

CL1, CL0:

The bit positions CL[1:0] (bits 1 & 0) of this register indicate the length of the inband loopback code sequence, as follows:

CL1	CL0	Code Length
0	0	5
0	1	6
1	0	7
1	1	8

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e. a 3-bit code would use the 6-bit code length setting).

Registers 047H, 0C7H, 147H, 1C7H, 247H, 2C7H, 347H, 3C7H: XIBC Loopback Code

Bit	Type	Function	Default
Bit 7	R/W	IBC7	X
Bit 6	R/W	IBC6	X
Bit 5	R/W	IBC5	X
Bit 4	R/W	IBC4	X
Bit 3	R/W	IBC3	X
Bit 2	R/W	IBC2	X
Bit 1	R/W	IBC1	X
Bit 0	R/W	IBC0	X

These registers contain the inband loopback code pattern to be transmitted. The code is transmitted most significant bit (IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (e.g., a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (i.e., the 3-bit code '011' would be written as the 6-bit code '011011').

When the TOCTL is reset, the contents of this register are not affected.

Registers 049H, 0C9H, 149H, 1C9H, 249H, 2C9H, 349H, 3C9H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	XFER	0
Bit 0	R	OVR	0

These registers contain status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt ; a logic 0 bit in the INTE position disables the generation of an interrupt. If the AUTOUPDATE bit is set in the Receive Line Options register, then INTE should be set, causing the XFER interrupt to occur every second, indicating that the PMON registers have been updated.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations, by writing to the Revision/Chip ID/Global PMON Update register (address 00CH) or via the AUTOUPDATE function, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFER being logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Registers 04A-04FH, 0CA-0CFH, 14A-14FH, 1CA-1CFH, 24A-24FH, 2CA-2CFH, 34A-34FH, 3CA-3CFH: Latching Performance Data

The Performance Data registers for a single framer are updated as a group by writing to any of the PMON count registers. A write to one (and only one) of these locations loads performance data located in the PMON into the internal holding registers. Alternately, the Performance Data registers for all eight framers are updated by writing to the Revision/Chip ID/Global PMON Update register (address 00CH). A third update option is to set the AUTOUPDATE bit in the Receive Line Options register, which causes the PMON to be updated automatically every second (or, more precisely, every 8000 frames). The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed.

The PMON is loaded with new performance data within 3.5 receive line clock, RLCLK[x], periods of the latch performance data register write. With nominal line rates, the PMON registers should not be polled until 2.3 µsec have elapsed from the "latch performance data" register write.

When the TOCTL is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

Registers 04AH, 0CAH, 14AH 1CAH, 24AH, 2CAH, 34AH, AND 3CAH: PMON BEE Count (LSB)

Bit	Type	Function	Default
Bit 7	R	BEE7	X
Bit 6	R	BEE6	X
Bit 5	R	BEE5	X
Bit 4	R	BEE4	X
Bit 3	R	BEE3	X
Bit 2	R	BEE2	X
Bit 1	R	BEE1	X
Bit 0	R	BEE0	X

These registers contain the lower eight bits of the 12-bit Bit Error event counter. A Bit Error event is defined as a CRC-6 error in ESF format, or a framing bit error in SF format.

Registers 04BH, 0CBH, 14BH 1CBH, 24BH, 2CBH, 34BH, AND 3CBH: PMON BEE Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	BEE11	X
Bit 2	R	BEE10	X
Bit 1	R	BEE9	X
Bit 0	R	BEE8	X

These registers contain the upper four bits of the 12-bit Bit Error event counter. A Bit Error event is defined as a CRC-6 error in ESF format, or a framing bit error in SF format.

Registers 04CH, 0CCH, 14CH, 1CCH, 24CH, 2CCH, 34CH, 3CCH: PMON FER Count (LSB)

Bit	Type	Function	Default
Bit 7	R	FER7	X
Bit 6	R	FER6	X
Bit 5	R	FER5	X
Bit 4	R	FER4	X
Bit 3	R	FER3	X
Bit 2	R	FER2	X
Bit 1	R	FER1	X
Bit 0	R	FER0	X

These registers contain the lower eight bits of the 9-bit Framing Bit Error event counter.

Registers 04DH, 0CDH, 14DH, 1CDH, 24DH, 2CDH, 34DH, 3CDH: PMON FER Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	FER8	X

These registers contain the upper bit of the 9-bit Framing Bit Error event counter.

Registers 04EH, 0CEH, 14EH, 1CEH, 24EH, 2CEH, 34EH, 3CEH: PMON OOF Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	OOF4	X
Bit 3	R	OOF3	X
Bit 2	R	OOF2	X
Bit 1	R	OOF1	X
Bit 0	R	OOF0	X

These registers contain the value of the 5 bit Out Of Frame event counter.

Registers 04FH, 0CFH, 14FH, 1CFH, 24FH, 2CFH, 34FH, 3CFH: PMON COFA Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	COFA2	X
Bit 1	R	COFA1	X
Bit 0	R	COFA0	X

These registers contain the value of the 3 bit counter accumulating Change of Frame Alignment events.

Registers 050H, 0D0H, 150H, 1D0H, 250H, 2D0H, 350H, 3D0H: RPSC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

These registers allow selection of the microprocessor read access type and output enable control for the Receive Per-DS0 Serial Controller. The RPSC allows data and signaling trunk conditioning to be applied on the receive DS-1 stream on a per-DS0 basis. It also allows per-DS0 control of data inversion, data extraction (when the NxDS0 interface is enabled), and the detection or generation of pseudo-random or repetitive patterns. More information on using the RPSC is available in the Operations section

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TOCTL is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-DS0 functions. When the PCCE bit is set to a logic 1, the Data Trunk Conditioning Code byte is enabled to modify the ingress data stream, ID[x], under direction of each channel's Ingress Control byte. When the PCCE bit is set to logic 0, the per-DS0 functions are disabled. The RPSC per-channel functions overwrite the data after the ELST, and thus overwrite the ELST trouble code when the framer is OOF.

Registers 051H, 0D1H, 151H, 1D1H, 251H, 2D1H, 351H, 3D1H: RPSC µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 052H, 0D2H, 152H, 1D2H, 252H, 2D2H, 352H, 3D2H: RPSC Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

These registers allow the µP to access the internal RPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal RPSC register is requested; when R/WB is set to a logic 0, a write to the internal RPSC register is requested.

Registers 053H, 0D3H, 153H, 1D3H, 253H, 2D3H, 353H, 3D3H: RPSC Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

These registers contain either the data to be written into the internal RPSC registers when a write request is initiated or the data read from the internal RPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal RPSC registers control the per-DS0 functions on the ingress data, and provide the per-DS0 data trunk conditioning code. The functions are allocated within the registers as follows:

01H	Ingress Control byte for Channel 1
02H	Ingress Control byte for Channel 2
• •	• •
17H	Ingress Control byte for Channel 23
18H	Ingress Control byte for Channel 24
19H	Data Trunk Conditioning byte for Channel 1
1AH	Data Trunk Conditioning byte for Channel 2
• •	• •
2FH	Data Trunk Conditioning byte for Channel 23
30H	Data Trunk Conditioning byte for Channel 24
31H	Signaling Trunk Conditioning byte for Channel 1
32H	Signaling Trunk Conditioning byte for Channel 2
• •	• •
47H	Signaling Trunk Conditioning byte for Channel 23
48H	Signaling Trunk Conditioning byte for Channel 24

The bits within each control byte are allocated as follows:

RPSC Internal Registers 01-18H: Ingress Control byte

Bit	Type	Function	Default
Bit 7	R/W	INVERT	
Bit 6	R/W	DTRKC	
Bit 5	R/W	DMW	
Bit 4	R/W	SIGNINV	
Bit 3	R/W	TEST	
Bit 2	R/W	EXTRACT	
Bit 1		Unused	
Bit 0		Unused	

INVERT:

When the INVERT bit is set to a logic 1, data output on the ID[x] pin is the bit inverse of the received data for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to logic 1, the most significant bit of the data output on the ID[x] pin in the inverse of the received data most significant bit for that channel.

INVERT	SIGNINV	Effect on PCM Channel Data
0	0	PCM Channel data is unchanged
1	0	All 8 bits of the PCM channel data are inverted
0	1	Only the MSB of the PCM channel data is inverted (SIGN bit inversion)
1	1	All bits EXCEPT the MSB of the PCM channel data is inverted (Magnitude inversion)

DTRKC:

When the DTRKC bit is set to a logic 1, data from the Data Trunk Conditioning Code Byte replaces the receive data for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the ID[x] output data for the duration of that channel.

TEST:

When the TEST bit is set to a logic 1, receive data is either overwritten with a test pattern from the PRGD block or is routed to the PRGD block and compared against an expected test pattern. The RXPATGEN bit in the Pattern Generator/Detector Positioning/Control register determines whether the receive data is overwritten or compared as shown in the following table:

TEST	RXPATGEN	Description
0	X	Channel data is not included in test pattern
1	0	Channel data is routed to PRGD and compared against expected test pattern
1	1	Channel data is overwritten with PRGD test pattern

Pattern generation/detection can be enabled to work on only the first 7 bits of a channel (for Nx56 kbps fractional T1) using the Nx56k_DET and Nx56k_GEN bits in the Pattern Generator/Detector Positioning/Control register (Reg. 00FH, 08FH, 10FH, 18FH, 20FH, 28FH, 30FH, 38FH). The PRGD can also be enabled to detect patterns in the entire DS1, including framing bits, using the UNF_DET bit in the Pattern Generator/Detector Positioning/Control register. More information on using the PRGD is available in the Operations section.

EXTRACT:

When the NxDS0 mode is active, EXTRACT controls the generation of ICLK[x]. When EXTRACT is a logic 1, channel data is extracted to the ingress interface and eight clock pulses are generated on ICLK[x]. When EXTRACT is a logic 0, ICLK[x] is suppressed for the duration of that channel.

Data inversion, data trunk conditioning, digital milliwatt pattern insertion, and test pattern insertion are performed independent of the received framing format. Digital milliwatt pattern insertion has the highest priority. Data trunk conditioning takes precedence over the test pattern insertion which, in turn, takes precedence over data inversion. When test pattern checking is enabled, the receive data is compared before data trunk conditioning or data inversion is performed.

RPSC Internal Registers 19-30H: Data Trunk Conditioning Code byte

Bit	Type	Function
Bit 7	R/W	DTRK7
Bit 6	R/W	DTRK6
Bit 5	R/W	DTRK5
Bit 4	R/W	DTRK4
Bit 3	R/W	DTRK3
Bit 2	R/W	DTRK2
Bit 1	R/W	DTRK1
Bit 0	R/W	DTRK0

The contents of the Data Trunk Conditioning Code byte register is substituted for the channel data on ID[x] when the DTRKC bit in the Ingress Control Byte is set to a logic 1. The Data Trunk Conditioning Code is transmitted from MSB (DTRK7) to LSB (DTRK0).

RPSC Internal Registers 31-48H: Signaling Trunk Conditioning byte

Bit	Type	Function	Default
Bit 7	R/W	STRKC	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	A'	
Bit 2	R/W	B'	
Bit 1	R/W	C'	
Bit 0	R/W	D'	

The contents of the Signaling Trunk Conditioning Code byte register is substituted for the channel signaling data on ISIG[x] when the STRKC bit is set to a logic 1. The Signaling Trunk Conditioning Code is placed in least significant nibble of the channel byte.

Registers 054H, 0D4H, 154H, 1D4H, 254H, 2D4H, 354H, 3D4H: RDLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

The RDLC is a microprocessor peripheral used to receive HDLC frames on the 4kHz ESF facility data link. More information on using the RDLC can be found in the Operations section.

EN:

The EN bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled.

TR:

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic 0.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC FIFO of only those packets whose first data byte

matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the RDLC FIFO.

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when performing the address comparison.

Reserved:

This register bit should be set to logic 0 for proper operation.

Register 055H, 0D5H, 155H, 1D5H, 255H, 2D5H, 355H, 3D5H: RDLC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC [6:0]:

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. Whenever the number of bytes in the RDLC FIFO exceeds the value of INTC[6:0], INTR is set to logic 1 and, if INTE is set, an interrupt will be generated. This interrupt persists until the RDLC FIFO becomes empty. A value of 0 in INTC[6:0] is interpreted as decimal 128.

INTE:

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC will not assert INTB.

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register 056H, 0D6H, 156H, 1D6H, 256H, 2D6H, 356H, 3D6H: RDLC Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

The RDLC Status and Data registers should not be accessed at a rate greater than 1/15 of the XCLK rate.

INTR:

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control Register is set to logic 1, a RDLC interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

1. the number of bytes specified in the RDLC Interrupt Control register have been received on the data link and written into the FIFO
2. RDLC FIFO buffer overrun has been detected
3. the last byte of a packet has been written into the RDLC FIFO
4. the last byte of an aborted packet has been written into the RDLC FIFO
5. transition of receiving all ones to receiving flags has been detected.

If INTR is logic 1 due to condition 1, then INTR will be cleared at the start of the next Data Register read that results in an empty FIFO buffer. This is independent of the FIFO buffer fill level for which the interrupt is programmed. If INTR is logic 1 due to conditions 2,3,4, or 5 then INTR is cleared by a read of this register. INTR may always be forced low by setting the EN bit low in the RDLC Configuration register, disabling the RDLC, or by setting the TR bit high in the

RDLC Configuration register, forcing RDLC to terminate reception of the current packet and empty the FIFO.

PBS[2:0]:

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in the following table:

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC Status Register is read.

COLS:

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 057H, 0D7H, 157H, 1D7H, 257H, 2D7H, 357H, 3D7H: RDLC Data

Bit	Type	Function	Default
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

The RDLC Status and Data registers should not be accessed at a rate greater than 1/15 of the XCLK rate.

RD[7:0]:

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the RDLC Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status Register is read.

Register 058H, 0D8H, 158H, 1D8H, 258H, 2D8H, 358H, 3D8H: RDLC Primary Address Match

Bit	Type	Function	Default
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 059H, 0D9H, 159H, 1D9H, 259H, 2D9H, 359H, 3D9H: RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Registers 05DH, 0DDH, 15DH, 1DDH, 25DH, 2DDH, 35DH, 3DDH: XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BC[5]	1
Bit 4	R/W	BC[4]	1
Bit 3	R/W	BC[3]	1
Bit 2	R/W	BC[2]	1
Bit 1	R/W	BC[1]	1
Bit 0	R/W	BC[0]	1

These registers enables the XBOC to generate a bit oriented code and selects the 6-bit code to be transmitted.

When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the ESF Facility Data Link with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0, overwriting any HDLC packets currently being transmitted. When the register is written with 111111, the XBOC is disabled.

Register 060H, 0E0H, 160H, 1E0H, 260H, 2E0H, 360H, 3E0H: PRGD Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

The PRGD provides test pattern generation, detection, and monitoring. More information on using PRGD can be found in the Operations section.

PDR[1:0]:

The PDR[1:0] bits select the contents of the four pattern detector registers (at addresses 6CH to 6FH in each octant) to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

QRSS:

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDAT stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PS:

The PS bit selects the pattern type. When PS is a logic 1, a repetitive pattern is generated/detected. When PS is a logic 0, a pseudo-random pattern is generated/detected.

The PS Bit must be programmed to the desired setting before programming any other PRGD registers, otherwise the transmitted pattern may be corrupted. Any time the setting of the PS bit is changed, the PRGD Pattern Insertion Registers should be reprogrammed.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted

RINV:

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. When AUTOSYNC is logic 1, then the PRGD will search in the receive data stream until it finds 48 consecutive bits in which the pattern is present and error-free. The PRGD will then declare SYNCV = 1. Thereafter, the PRGD will automatically initiate a resynchronization when 10 or more bit errors are detected in a fixed 48 bit window. When AUTOSYNC is a logic 0, then the PRGD will search in the data stream in the same way. However, once SYNCV=1 has been declared, resynchronization will only be initiated by a 0 to 1 transition on MANSYNC. SYNCV will still be asserted and deasserted in the usual way, but the PRGD will not initiate a search for the new pattern alignment.

MANSYNC:

The MANSYNC bit is used to manually initiate a resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 061H, 0E1H, 161H, 1E1H, 261H, 2E1H, 361H, 3E1H: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. Bit errors are not flagged unless the pattern detector is synchronized. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled. PMON and PRGD transfer values in the same number of clock cycles, so as long as both are being updated at once, only one interrupt need be used.

SYNCV:

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 48 consecutive error free bit periods). When

SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 10 or more bit errors in a fixed 48 bit window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, then the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. Bit errors are not flagged unless the pattern detector is synchronized. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the Revision/Chip ID/Global PMON Update register (00CH), or via the AUTOUPDATE feature in the Receive Line Options Register (000H, 080H, 100H, 180H, 200H, 280H, 300H, 480H). XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 062H, 0E2H, 162H, 1E2H, 262H, 2E2H, 362H, 3E2H: PRGD Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]:

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 063H, 0E3H, 163H, 1E3H, 263H, 2E3H, 363H, 3E3H: PRGD Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]:

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 064H, 0E4H, 164H, 1E4H, 264H, 2E4H, 364H, 3E4H: PRGD Error Insertion Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT:

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]:

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in the following table:

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

In order to prevent single error insertion from interfering with error rate generation, writes to EIR[2:0] do not take effect immediately. Instead, they take effect when the next generated bit error occurs. When using very low error rates and using PRGD in only a few channels, this delay can be significant, since a 10^{-7} error rate at 64kbps is one error every 156 seconds.

Register 068H, 0E8H, 168H, 1E8H, 268H, 2E8H, 368H, 3E8H: PRGD Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 069H, 0E9H, 169H, 1E9H, 269H, 2E9H, 369H, 3E9H: PRGD Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 06AH, 0EAH, 16AH, 1EAH, 26AH, 2EAH, 36AH, 3EAH: PRGD Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 06BH, 0EBH, 16BH, 1EBH, 26BH, 2EBH, 36BH, 3EBH: PRGD Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]:

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to FFFFFFFFH. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written. When a repetitive pattern is transmitted, PI[31] is transmitted first, followed by the remaining bits in sequence down to PI[0]. Subsequently, PI [pattern_length-1] down to PI[0] will be repetitively transmitted, where pattern_length is the decimal value stored in the PRGD length register.

Register 06CH, 0ECH, 16CH, 1ECH, 26CH, 2ECH, 36CH, 3ECH: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 06DH, 0EDH, 16DH, 1EDH, 26DH, 2EDH, 36DH, 3EDH: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 06EH, 0EEH, 16EH, 1EEH, 26EH, 2EEH, 36EH, 3EEH: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 06FH, 0EFH, 16FH, 1EFH, 26FH, 2EFH, 36FH, 3EFH: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]:

Reading PD[31:0] returns the contents of the pattern detector data register selected by the PDR[1:0] bits in the control register. All three detector data registers are updated during an accumulation interval.

When PDR[1:0] is set to 00 or 01, reading PD[31:0] returns the contents of pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0]. PD[0] contains the bit received immediately prior to the last accumulation. The pattern receive register is particularly useful for identifying received repetitive patterns.

When PDR[1:0] is set to 10, reading PD[31:0] returns the contents of the error counter holding register. The value in this register represents the number of bit errors that were accumulated during the last accumulation interval, up to a maximum (saturation) of 2^{32}-1. Note that bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, reading PD[31:0] returns the contents of the bit counter holding register. The value in this register represents the total number of bits that were received during the last accumulation interval, up to a maximum (saturation) of 2^{32}-1.

Writing to any of these registers causes them to be updated, and the internal counters reset. The XFERI bit in PRGD Enable/Status register will go high once the update is complete, and an interrupt will be generated if enabled.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TOCTL. Test mode registers (as opposed to normal mode registers) are mapped into addresses 400H-7FFH.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the TOCTL are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 00BH: TOCTL Master Test

Bit	Type	Function	Default
Bit 7	R/W	A_TM[9]	X
Bit 6	R/W	A_TM[8]	X
Bit 5	R/W	A_TM[7]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select TOCTL test features. All bits, except for PMCTST and A_TM[9:7] are reset to zero by a hardware reset of the TOCTL; a software reset of the TOCTL does not affect the state of the bits in this register. Refer to the Test Features Description section for more information.

A_TM[9]:

The state of the A_TM[9] bit internally replaces the input address line A[9] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[8]:

The state of the A_TM[8] bit internally replaces the input address line A[8] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[7]:

The state of the A_TM[7] bit internally replaces the input address line A[7] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the TOCTL for PMC's manufacturing tests. When PMCTST is set to logic 1, the TOCTL microprocessor port becomes the test access port used to run the PMC manufacturing test

vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the TOCTL to drive the data bus and holding the CSB pin low tristates the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the TOCTL for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tristate modes of the TOCTL . While the HIZIO bit is a logic 1, all output pins of the TOCTL except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

12.1 Test Mode 0

In test mode 0, the TOCTL allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Master Test Register is set to logic 1 and the following addresses must be written with 00H: 411H, 419H, 41DH, 421H, 42BH, 42DH, 431H, 435H, 43DH, 441H, 445H, 449H, 451H, 455H, 45DH, and 461H. Repeat these writes to 491H, 499H, ... , 4E1H, then 511H .. 561H, and so on until all 8 octants have been set up.

Reading the following address locations returns the values for the indicated inputs :

Table 5 - Accessing Inputs in Test Mode 0

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
410H					XCLK	RLCLK[1]		RLD[1]
418H					XCLK	CTCLK		
41CH	CIFP	CICLK						
444H	CECLK		CEFP		ESIG[1]			ED[1]
490H					XCLK	RLCLK[2]		RLD[2]
498H					XCLK	CTCLK		
49CH	CIFP	CICLK						
4C4H	CECLK		CEFP		ESIG[2]			ED[2]
510H					XCLK	RLCLK[3]		RLD[3]
518H					XCLK	CTCLK		
51CH	CIFP	CICLK						
544H	CECLK		CEFP		ESIG[3]			ED[3]
590H					XCLK	RLCLK[4]		RLD[4]
598H					XCLK	CTCLK		
59CH	CIFP	CICLK						
5C4H	CECLK		CEFP		ESIG[4]			ED[4]
610H					XCLK	RLCLK[5]		RLD[5]
618H					XCLK	CTCLK		
61CH	CIFP	CICLK						
644H	CECLK		CEFP		ESIG[5]			ED[5]
690H					XCLK	RLCLK[6]		RLD[6]
698H					XCLK	CTCLK		
69CH	CIFP	CICLK						
6C4H	CECLK		CEFP		ESIG[6]			ED[6]
710H					XCLK	RLCLK[7]		RLD[7]
718H					XCLK	CTCLK		
71CH	CIFP	CICLK						
744H	CECLK		CEFP		ESIG[7]			ED[7]
790H					XCLK	RLCLK[8]		RLD[8]
798H					XCLK	CTCLK		
79CH	CIFP	CICLK						
7C4H	CECLK		CEFP		ESIG[8]			ED[8]

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Table 6 - Controlling Outputs in Test Mode 0

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
418H	INT[1]					TLCLK[1]		TLD[1]
41CH		INT[1]					IFP[1]	
440H						ID[1][2]	ISIG[1]	
498H	INT[1]					TLCLK[2]		TLD[2]
49CH		INT[1]					IFP[2]	
4C0H						ID[2][2]	ISIG[2]	
518H	INT[1]					TLCLK[3]		TLD[3]
51CH		INT[1]					IFP[3]	
540H						ID[3][2]	ISIG[3]	
598H	INT[1]					TLCLK[4]		TLD[4]
59CH		INT[1]					IFP[4]	
5C0H						ID[4][2]	ISIG[4]	
618H	INT[1]					TLCLK[5]		TLD[5]
61CH		INT[1]					IFP[5]	
640H						ID[5][2]	ISIG[5]	
698H	INT[1]					TLCLK[6]		TLD[6]
69CH		INT[1]					IFP[6]	
6C0H						ID[6][2]	ISIG[6]	
718H	INT[1]					TLCLK[7]		TLD[7]
71CH		INT[1]					IFP[7]	
740H						ID[7][2]	ISIG[7]	
798H	INT[1]					TLCLK[8]		TLD[8]
79CH		INT[1]					IFP[8]	
7C0H						ID[8][2]	ISIG[8]	

Notes:

1. Writing a logic 1 to any of the block interrupt signals asserts the INTB output low. In order to force INT high-impedance, registers 410 .. 461 in each octant must initially be cleared.

2. In order for bit 2 of this register to control ID[x], bit 3 of this register must be written logic 0.

The bidirectional pins ESIG[x]/ECLK[x]/EFP[x] are inputs while IOTST is set.

12.2 JTAG Test Port

The TOCTL JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 1H for Rev. E, 0H for Rev. C.

Part Number - 4388H

Manufacturer's identification code - 0CDH

Device identification - 143880CDH for Rev. E (043880CDH for Rev. C.)

Table 7 - Boundary Scan Register

Length - 120 bits

Pin/ Enable	Scan Register Bit	Pin/ Enable	Scan Register Bit	Pin/ Enable	Scan Register Bit
HIZ [2,3]	120	D3	79	ISIG3	38
RLD1	119	D3_OEB [1]	78	ID3	37
RLCLK1	118	D4	77	IFP2	36
RLD2	117	D4_OEB [1]	76	ISIG2	35
RLCLK2	116	D5	75	ID2	34
RLD3	115	D5_OEB [1]	74	IFP1	33
RLCLK3	114	D6	73	ISIG1	32
RLD4	113	D6_OEB [1]	72	ID1	31
RLCLK4	112	D7	71	ESIG8	30
TLD1	111	D7_OEB [1]	70	ESIG_OEB8[1]	29
TLCLK1	110	ALE	69	ED8	28
TLD2	109	A0	68	ESIG7	27
TLCLK2	108	A1	67	ESIG_OEB7[1]	26
TLD3	107	A2	66	ED7	25
TLCLK3	106	A3	65	ESIG6	24
TLD4	105	A4	64	ESIG_OEB6[1]	23
TLCLK4	104	A5	63	ED6	22
TLD5	103	A6	62	ESIG5	21
TLCLK5	102	A7	61	ESIG_OEB5[1]	20
TLD6	101	A8	60	ED5	19
TLCLK6	100	A9	59	ESIG4	18
TLD7	99	A10	58	ESIG_OEB4[1]	17
TLCLK7	98	CSB	57	ED4	16
TLD8	97	WRB	56	ESIG3	15

Pin/ Enable	Scan Register Bit	Pin/ Enable	Scan Register Bit	Pin/ Enable	Scan Register Bit
TLCLK8	96	RDB	55	ESIG_OEB3[1]	14
RLD5	95	IFP8	54	ED3	13
RLCLK5	94	ISIG8	53	ESIG2	12
RLD6	93	ID8	52	ESIG_OEB2[1]	11
RLCLK6	92	IFP7	51	ED2	10
RLD7	91	ISIG7	50	ESIG1	9
RLCLK7	90	ID7	49	ESIG_OEB1[1]	8
RLD8	89	IFP6	48	ED1	7
RLCLK8	88	ISIG6	47	XCLK	6
RSTB	87	ID5	46	CIFP	5
INTB	86	IFP5	45	CICLK	4
D0	85	ISIG5	44	CEFP	3
D0_OEB [1]	84	ID5	43	CECLK	2
D1	83	IFP4	42	CTCLK	1
D1_OEB [1]	82	ISIG4	41		
D2	81	ID4	40		
D2_OEB [1]	80	IFP3	39		

Notes:

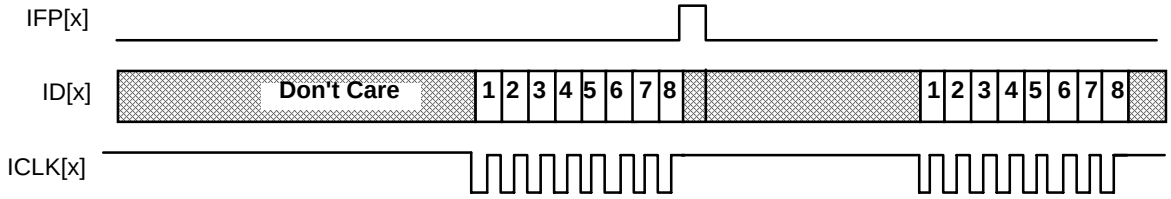
1. All OEB signals will set the corresponding bidirectional signal to an output when set low.

2. When set high, TLD[8:1], TLCLK[8:1], ID[8:1], ISIG[8:1], IFP[8:1], and INTB will be set to high impedance.

3. HIZ is the first bit in the boundary scan chain.

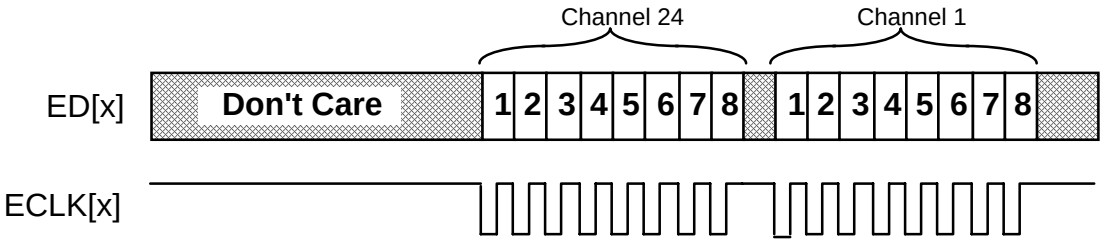
13 FUNCTIONAL TIMING DIAGRAMS

Figure 14 - Ingress Interface Clock Master: NxDS0 Mode



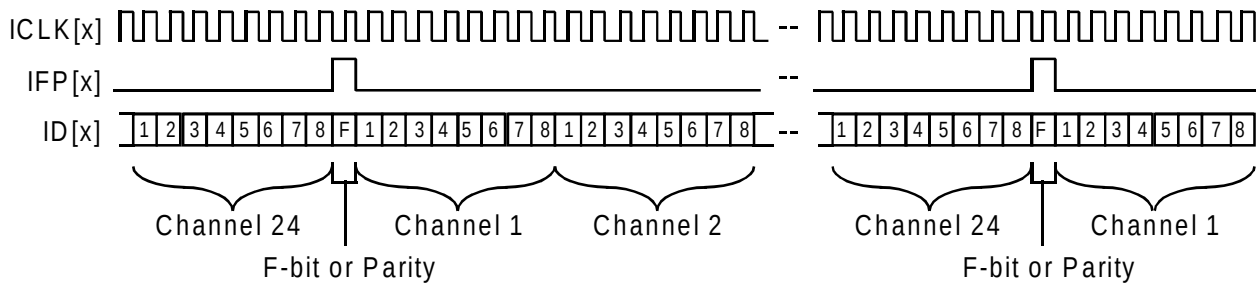
The Ingress Interface Options register is programmed to select NxDS0 mode. The RPSC ingress control bytes are programmed to extract the desired channels. In this example, the ingress control bytes for channels 2 and 24 are configured to extract these channels. ICLK[x] is gapped so that it is only active for those channels with the associated EXTRACT bit set. If either ISFP or ALTIFP is set, then IFP[x] will pulse only during the appropriate frames. When the ICLKRISE register bit is set, then ID[x] is updated on the rising edge of ICLK[x] and the functional timing is described by Figure 14 with ICLK inverted.

Figure 15 - Egress Interface Clock Master: NxDS0 Mode



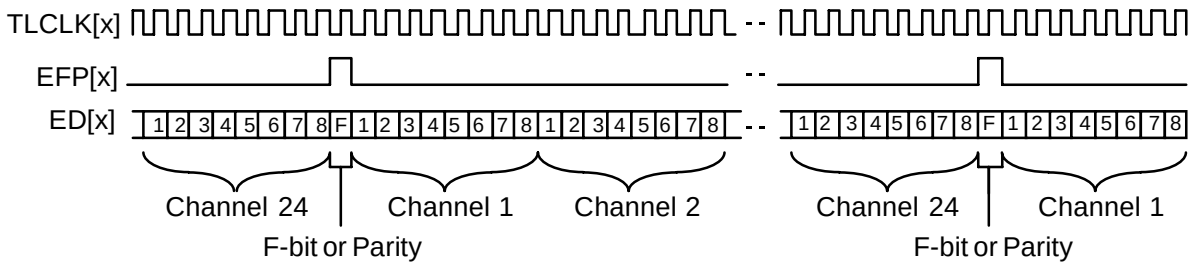
The Egress Interface Options register is programmed to select NxDS0 mode. The TPSC egress control bytes are programmed to insert the desired channels. In this example, the egress control bytes for channels 1 and 24 are configured to insert these channels. ECLK[x] is gapped so that it is only active for those channels with the associated IDLE_DS0 bit cleared (logic 0). The remaining channels (with IDLE_DS0 set) contain the per-DS0 idle code as defined in the associated Idle Code byte. When the ECLKFALL bit is set to logic 1, then ED[x] is sampled on the falling edge of ECLK, and the functional timing is described by Figure 15 with the ECLK signal inverted.

Figure 16 - Ingress Interface Clock Master : Full DS1 Mode



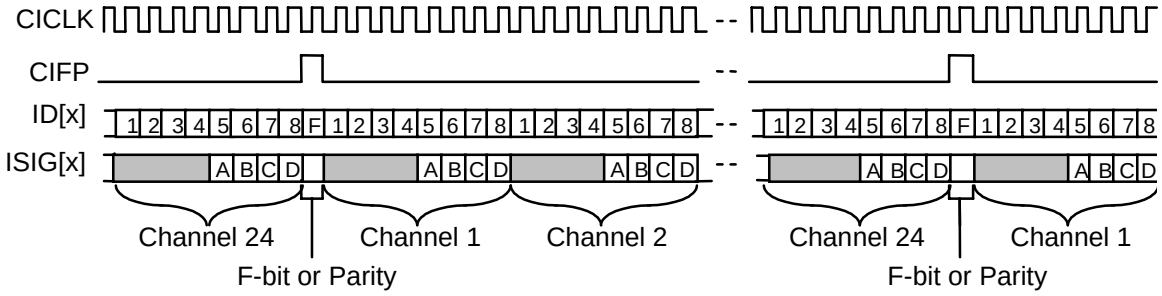
The Ingress Interface Options register is programmed to select the Clock Master: Full DS1 mode. IFP[x] is set high for one ICLK[x] period every frame. If ISFP=1, IFP[x] pulses on the superframe frame boundaries (i.e. once every 12 or 24 frame periods). If ALTRFP=1, IFP[x] pulses on every second indication of either the frame or the superframe boundary.

Figure 17 - Egress Interface : 1.544 MHz Clock Master: Full DS1 Mode



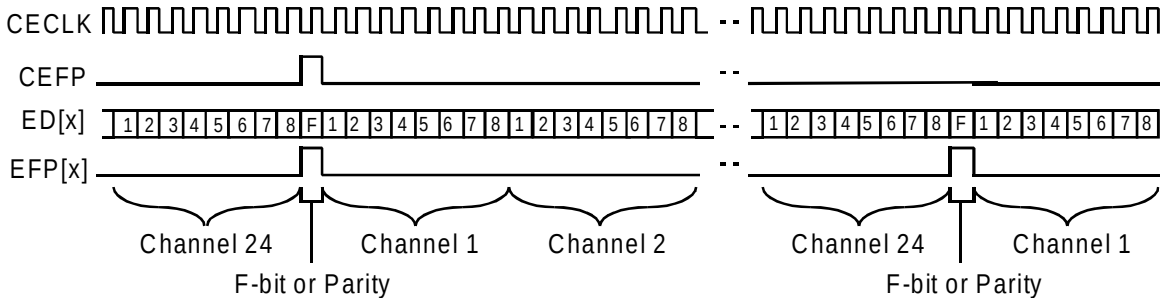
The Egress Interface is configured for the Clock Master: Full DS1 mode by writing 01 binary to EMODE[1:0] in the Egress Options register. ED[x] is clocked in on the rising edge of the TLCLK[x] output. Frame alignment is indicated to an upstream source by EFP[x], which may be configured to indicate frame or superframe alignment via the ESFP bit in the Egress Options Register.

Figure 18 - Ingress Interface: 1.544MHz Clock Slave Modes



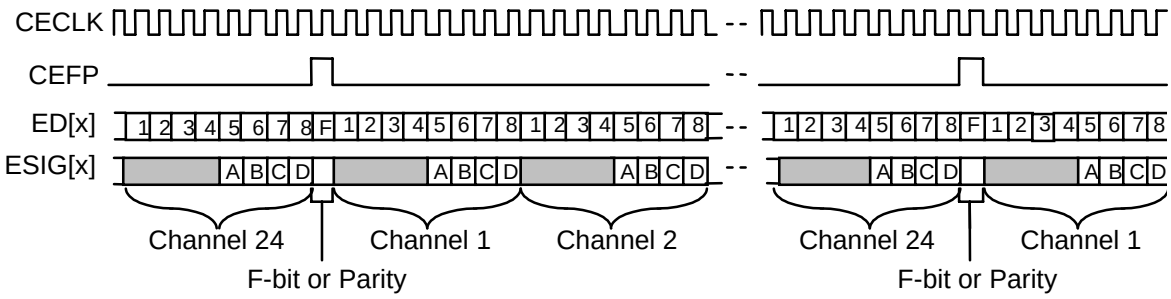
The Ingress Interface is programmed for Clock Slave mode by setting the IMODE[1:0] bits to 10 (ICLK Reference) or 11 (external signaling) in the Ingress Interface Options register. ID[x] is timed to the active edge of CICLK, and is frame-aligned to CIFP; CIFP need not be provided every frame. ID[x] and ISIG[x] may be configured to carry a parity bit during the first bit of each frame. In External Signaling Mode, ISIG[x] is active and is aligned as shown. In ICLK Reference mode, ICLK[x] is active in place of ISIG[x]; ICLK is either a jitter-attenuated line-rate clock referenced to RLCLK, or an 8 kHz clock generated by dividing the smoothed RLCLK by 193.

Figure 19 - Egress Interface : 1.544 MHz Clock Slave: EFP Enabled mode



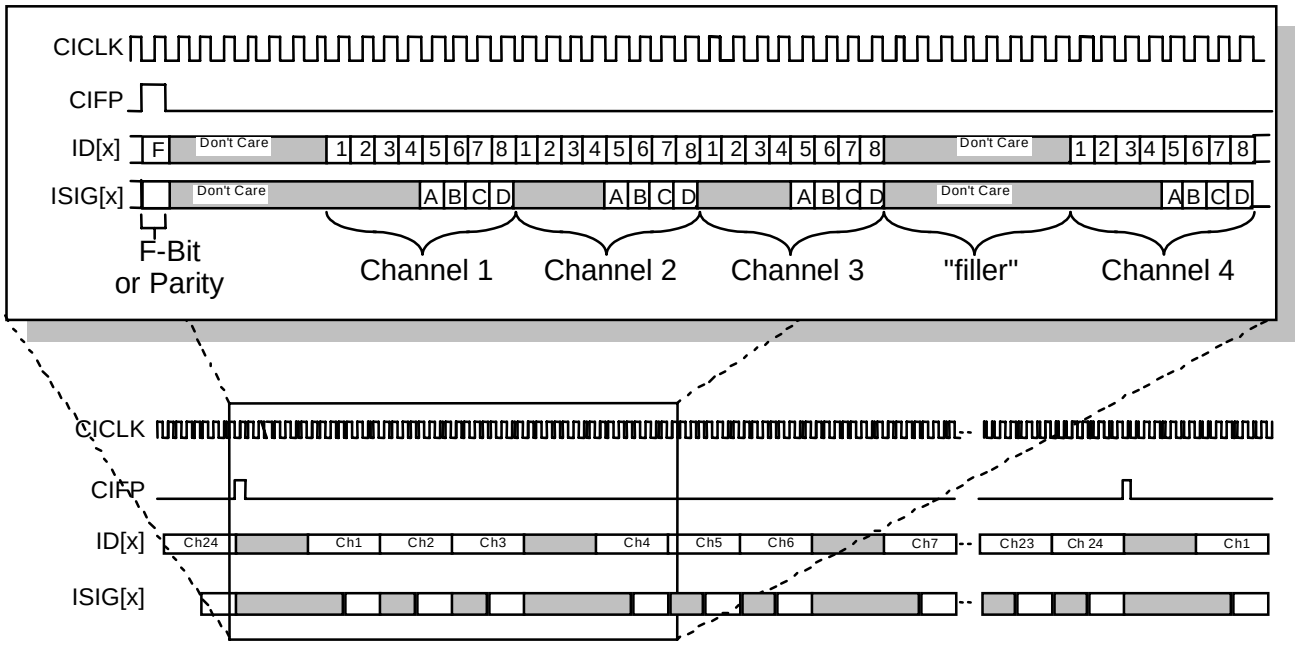
The Egress Interface is configured for the Clock Slave: EFP Enabled mode by writing 10 binary to EMODE[1:0] in the Egress Options register. ED[x] is clocked in on the active edge of CECLK. In the illustrated case, the CESFP bit is written to logic 1 in the Egress Options Register, so that CEFP must pulse once every 12 or 24 frames (for SF and ESF, respectively) on the *last* frame bit of the multiframe. If parity checking is enabled, a parity bit should be inserted on ED[x] in the first bit of each frame. The EFP[x] output will pulse high to mark the F-bit of each frame in order to indicate frame alignment to an upstream device; EFP may be configured to mark superframe alignment instead via the ESFP bit in the Egress Options Register.

Figure 20 - Egress Interface : 1.544 MHz Clock Slave: External Signaling mode



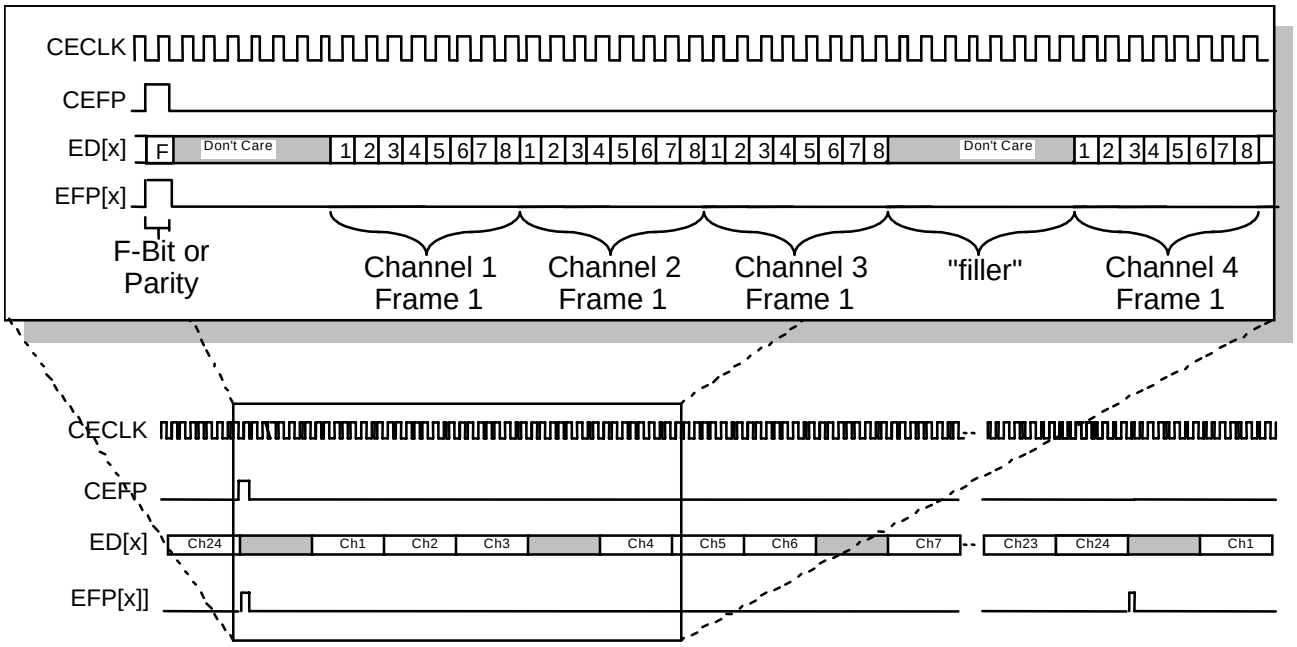
The Egress Interface is configured for the Clock slave: External Signaling Mode by writing 11 binary to EMODE[1:0] in the Egress Options register. ED[x] is clocked in on the active edge of CECLK. Frame alignment is specified by pulses on CEFP. ESIG[x] should carry the signaling bits for each channel in bits 5,6,7 and 8; the signaling bits will be inserted into the data stream by the transmitter. If the ABXXEN bit is set to logic 1 in the Egress Options register, then the A and B bits will be internally forced onto the C and D positions. If parity checking is enabled, a parity bit should be inserted on ED[x] and ESIG[x] in the first bit of each frame. The parity operates on all bits in the ED[x] and ESIG[x] streams, including the unused bits on ESIG. ABXXEN has no effect on ESIG[x] parity.

Figure 21 - Ingress Interface: 2.048 MHz Clock Slave Mode



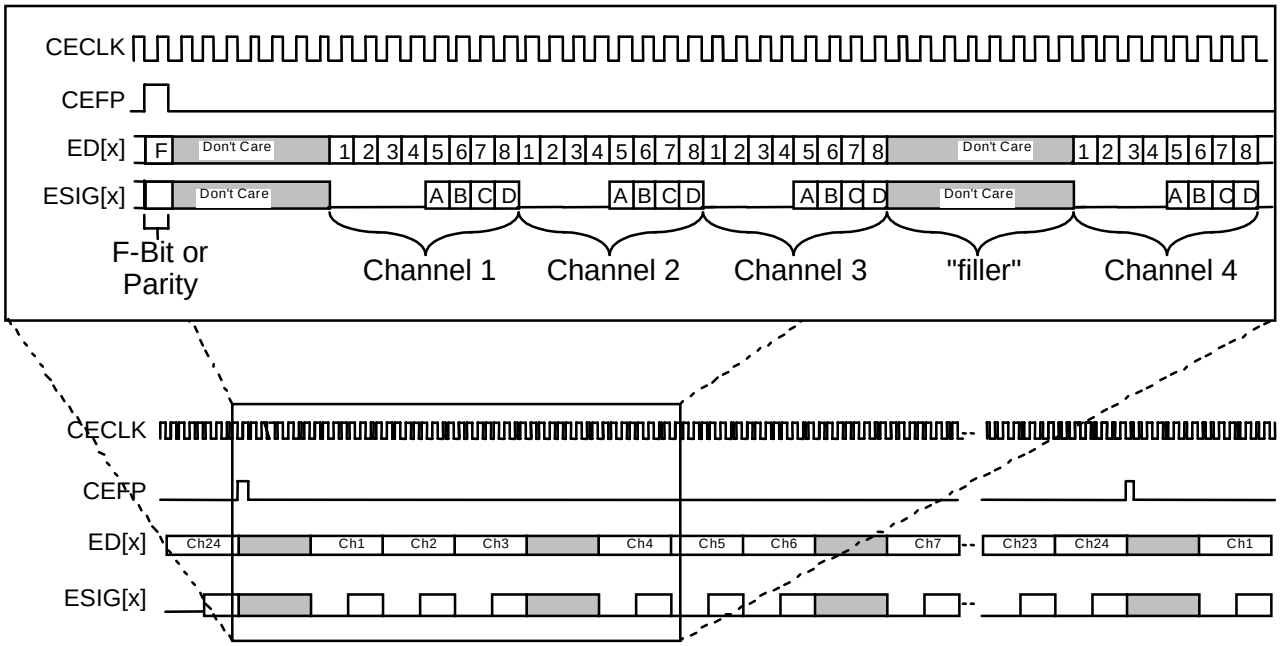
The Ingress Interface is programmed for Clock Slave mode by stetting the IMODE[1:0] bits to 10 (ICLK Reference) or 11 (external signaling) in the Ingress Interface Options register. The 2.048 MHz internally-gapped clock mode is selected by setting the CICLK2M bit to logic 1 in the Ingress Interface Options. ID[x] is timed to the active edge of CICLK, and is frame-aligned to CIFP; CIFP need not be provided every frame. ID[x] and ISIG[x] may be configured to carry a parity bit during the first bit of each frame. In External Signaling Mode, ISIG[x] is active and is aligned as shown. In ICLK Reference mode, ICLK[x] is active in place of ISIG[x]; ICLK is either a jitter-attenuated line-rate clock referenced to RLCLK, or an 8 kHz clock generated by dividing RLCLK by 193. The values of the filler bits will depend on the exact configuration of the TOCTL, and they will be included in the parity calculation

Figure 22 - Egress Interface: 2.048 MHz Clock Slave: EFP Enabled Mode



The Egress Interface is configured for the Clock Slave: EFP Enabled Mode by writing 10 binary to EMODE[1:0] in the Egress Options register. The 2.048 MHz internally gapped clock mode is selected by writing CECLK2M to logic 1 in the Egress Options Register. In the illustrated case, CEFP is configured for superframe alignment by writing CESFP to logic 1 in the Egress Options Register, so that the CEFP input must pulse once every 12 or 24 frames (for SF and ESF, respectively) on the *last* F-bit of the multiframe to specify superframe alignment, instead of once every frame to specify frame alignment. If parity checking is enabled, a parity bit should be inserted on ED[x] in the first bit of each frame. The EFP[x] output will pulse high to mark the F-bit of each frame in order to indicate frame alignment to an upstream device; EFP may be configured to mark superframe alignment instead. The values of the don't-care bits are not important, except that they will be used in the backplane parity check if it is enabled.

Figure 23 - Egress Interface: 2.048 MHz Clock Slave: External Signaling Mode



The Egress Interface is configured for the 2.048 MHz Clock Slave: External Signaling Mode by writing 11 binary to EMODE[1:0] in the Egress Options register. The 2.048 MHz internally gapped clock mode is selected by writing CECLK2M to logic 1 in the Egress Options register. In the illustrated case, CEFP specifies frame alignment and is required to pulse high for one cycle every frame. ESIG[x] should carry the signaling bits for each channel in bits 5,6,7 and 8; the signaling bits will be inserted into the data stream by the transmitter. If the ABXXEN bit is set to logic 1 in the Egress Options register, then the A and B bits will be repeated in the C and D positions. If parity checking is enabled, a parity bit should be inserted on ED[x] and ESIG[x] in the first bit of each frame. The values of the don't-care bits are not important, except that they will be used in the backplane parity check if it is enabled.

14 OPERATIONS

14.1 Configuring the TOCTL from Reset

After a system reset (either via the RSTB pin or via the RESET register bit), the TOCTL will default to the following settings:

Table 8 - Default Settings

Setting	Receiver Section	Transmitter Section
Framing Format	SF	SF
DS-1 interface	• RLD[x] inputs NRZ data sampled on rising RLCLK[x] edge.	• TLD[x] outputs NRZ data updated on falling TLCLK[x] edge
Ingress/Egress Interfaces	• Clock Slave: External Signaling Mode • ID[x], ISIG[x] updated on falling CICLK edge • Elastic Store enabled, CIFP indicates frame alignment	• Clock Slave: External Signaling Mode • ED[x] and ESIG[x] sampled on rising CECLK edge • CEFP indicates frame alignment
Data Link	• internal RDLC disabled	• internal TDPR disabled
Options	• Signaling alignment disabled • Automatic trunk conditioning disabled • PRGD configured to monitor test patterns	• PRGD configured to insert test patterns • F, CRC, FDL bit bypass disabled
Timing Options	Not applicable	• Digital jitter attenuation enabled, with TLCLK[x] referenced to CECLK
Diagnostics	• All diagnostic modes disabled	• All diagnostic modes disabled

In the following tables the "Addr Offset" is the address relative to 000H, 080H, 100H, 180H, 200H, 280H, 300H, or 380H depending on which framer is being configured.

To configure the TOCTL for ESF framing format, after a reset, the following registers should be written with the indicated values:

Table 9 - ESF Frame Format

Action	Addr Offset	Data	Effect
Write XBAS Configuration Register	44H	10H	Select ESF transmitter
Write FRMR Configuration Register	20H	10H or 50H or 90H	Select ESF, 2 of 4 OOF threshold Select ESF, 2 of 5 OOF threshold Select ESF, 2 of 6 OOF threshold
Write RBOC Enable Register	2AH	00H or 02H	Enable 8 out of 10 validation Enable 4 out of 5 validation
Write ALMI Configuration Register	2CH	10H	Select ESF
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	04H	Select ESF

To configure the TOCTL for SF framing format, after a reset, the following registers should be written with the indicated values:

Table 10 - SF Frame Format

Action	Addr Offset	Data	Effect
Write XBAS Configuration Register	44H	00H	Enable for SF in transmitter
Write FRMR Configuration Register	20H	00H or 40H or 80H	Select SF, 2 of 4 OOF threshold Select SF, 2 of 5 OOF threshold Select SF, 2 of 6 OOF threshold
Write ALMI Configuration Register	2CH	00H	Select SF
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	00H	Select SF

To access the Performance Monitor Registers, the following polling sequence should be used:

Table 11 - PMON Polling Sequence

Action	Addr Offset	Data	Effect
Write PMON BEE Count (LSB) Register (To transfer the PMON registers for all eight framers, write the Revision/Chip ID/Global PMON Update register.)	4CH	00H	Latch performance data into PMON registers
Read BEE Count (LSB) Register	4AH		Read least significant byte of bit error event count

Action	Addr Offset	Data	Effect
Read BEE Count (MSB) Register	4BH		Read most significant byte of bit error event count
Read FER Count (LSB) Register	4CH		Read least significant byte of Framing bit error event count
Read FER Count (MSB) Register	4DH		Read most significant byte of Framing bit error event count
Read OOF Count Register	4EH		Read out-of-frame event count
Read COFA Count Register	4FH		Read change of frame alignment event count

14.2 Using the Internal FDL Transmitter

The access rate to the TDPR registers is limited by the rate of the high-speed system clock (XCLK). The TDPR registers should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the 37.056 MHz XCLK. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status.

Upon reset of the TOCTL, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value).An HDLC all-ones Idle signal will be sent while in this state. The TDPR should then be enabled by setting EN to logic 1. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until the current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC

packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the TOCTL Interrupt ID register, and the TOCTL Interrupt Source registers to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

Interrupt Driven Mode:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for data to be transmitted. Once data is available to be transmitted, then go to step 2.

2. Write the data byte to the TDPR Transmit Data register.

3. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

4. If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold

limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

TDPR Interrupt Routine:

Upon assertion of INTB, the source of the interrupt must first be identified by reading the Interrupt ID register and Interrupt Source registers. Once the source of the interrupt has been identified as TDPR, then the following procedure should be carried out:

1. Read the TDPR Interrupt Status register.

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To reenable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

3. If OVRI=1, then the FIFO has overflowed. The packet which the last byte written into the FIFO belongs to has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit. The next write to the TDPR Transmit Data register should contain the first byte of the next packet to be transmitted.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), the OVRI bit is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

4. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

   If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

Polling Mode:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

3. If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

4. If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step 6.

5. If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step 6.

6. If more data bytes are to be transmitted in the packet, then go to step 2.

7. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

14.3 Using the Internal FDL Receiver

The RDLC requires 15 XCLK cycles to process the results of accesses to the RDLC Status and RDLC Data registers. Thus, accesses to these registers should not occur at a rate greater than 1/15 of the 37.056 MHz XCLK.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default state). The RDLC Interrupt Control register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register to determine when to read the RDLC Data register. In the interrupt driven mode, the processor controlling the RDLC

must identify the interrupt source to determine when to read the RDLC Data register.

When the RDLC is identified as the interrupt source, the RDLC should be serviced as follows:

1. RDLC Status register read. The INTR bit should be logic 1 if the RDLC is the interrupt source.

2. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3. If COLS = 1, then set the EMPTY FIFO software flag.

4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

5. Read the RDLC Data register.

6. Read the RDLC Status register.

7. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8. If COLS = 1, then set the EMPTY FIFO software flag.

9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    10.1) If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

    10.2) If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

    10.3) If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

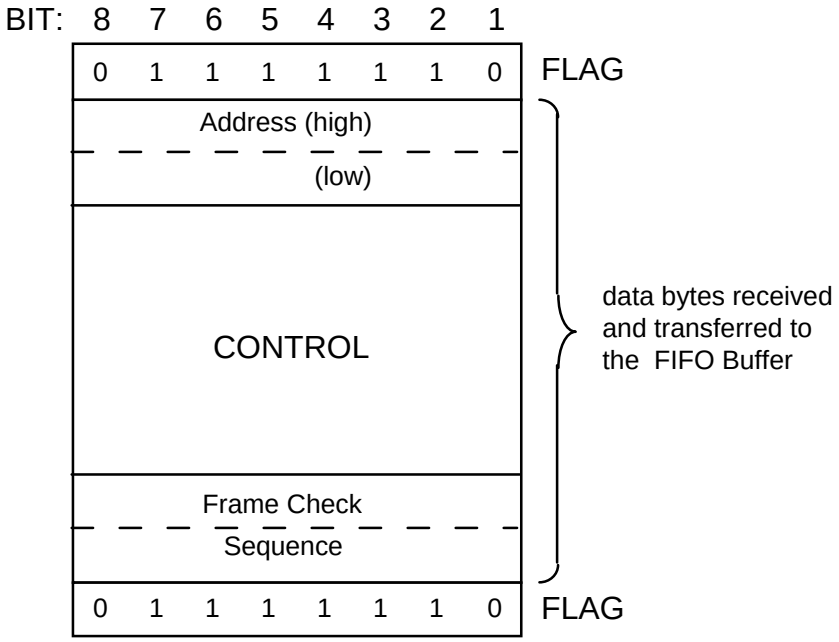
10.4) If PBS[2:0] = 000, store the packet data.

11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

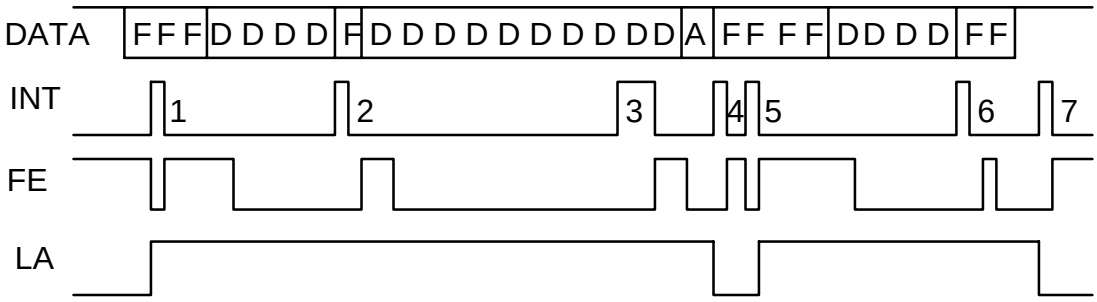
If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 24 - Typical Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 25 - Example Multi-Packet Operational Sequence



F - flag sequence (01111110)

A - abort sequence (01111111)

D - packet data bytes

INT - active high interrupt output

FE - internal FIFO empty status

LA - state of the LINK ACTIVE software flag

Figure 25 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

At points 1 and 5 the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

14.4 Using the PRGD Pattern Generator/Detector

The pattern generator/detector block provides a valuable diagnostic tool, capable of generating and detecting an enormous variety of pseudo-random and repetitive patterns. Controlling the PRGD is accomplished by programming four register sets: the Pattern Generator/Detector Positioning/Control Register (00FH, 08FH, 10FH, 18FH, 20FH, 28FH, 30FH, 38FH), the TPSC Internal Registers 01-18H, the RPSC Internal Registers 01-18H, and the PRGD registers.

Using PRGD to test T1 link integrity

For example, suppose it is desired to monitor the error rate on a T1 link without taking the entire T1 offline. A subset of channels should be chosen (say channels 1,3,5 and 7) to carry PRBS instead of data. The TPSC Egress Control Bytes for channels 1,3,5 and 7 must have their TEST bits set to logic 1, and PCCE must be set in the TPSC Configuration register to enable the per-DS0 functions. Register 00F should be written to its default of all-zeroes. The PRGD should be configured to generate the desired PRBS sequence. The selected channels will then be treated as a single, concatenated data stream in which the selected PRBS will appear. If the device at the far end of the line can be set to loop back at least the selected channels, then the PRGD can be used to monitor the return error rate. The RPSC Ingress Control Bytes for channels 1,3,5, and 7 must have their TEST bits set to logic 1, and the PCCE bit set in the RPSC Configuration register to enable the per-DS0 functions. The PRGD will then synchronize to the returning pattern, and begin counting errors. To determine the BER, an periodic accumulation of the PRGD detection registers may be forced by writing to one of the PRGD Pattern Detector registers, by writing to the Revision/Chip ID/Global PMON Update register (00CH), or via the AUTOUPDATE feature. The bit error count, bits received count, and previous 32 bits received are then available via the Pattern Detector registers.

In this scenario, any desired combination of channels may be selected. If it is desired to insert the test pattern in the entire T1, including the framing bits, then UNF_GEN must be set in the Pattern Generator/Detector Positioning/Control

Register, and framing bit insertion must be disabled by setting FDIS to logic 1 in the Transmit Framing and Bypass Options Register. To detect such an unframed sequence, UNF_DET must also be set.

Using PRGD to test backplane integrity

If, instead, it is desired to test the backplane side of the system, RXPATGEN may be set to logic 1 in the Pattern Generator/Detector Positioning/Control Register. This will cause the pattern to replace the data received in the selected channels of RLD[x], and will cause the PRGD to search for the desired PRBS on the ED[x] stream.

Inserting PRBS in the 7 MSB of each channel

In cases where the least-significant bit of the channel may be overwritten by signaling, excess zeroes suppression, SIGX signaling bit fixing, or other factors, the Nx56k_GEN and/or Nx56k_DET bits may be set in the Pattern Generator/Detector Positioning/Control Register. This will cause the PRGD to only insert patterns into, or detect patterns in, the seven most-significant bits of selected channels. This feature is particularly useful when generating or monitoring for fractional T1 loopback codes when handling Nx56kbps fractional T1.

Generating and detecting repetitive patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers. The repetitive pattern will then be continuously generated. The generated pattern will be inserted in data stream formed from the selected channels, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the selected channels. It does so by loading the first N bits from the selected channels, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences. Note that the PRGD does NOT

look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers (which will then contain the 32 bits detected immediately prior to the strobe).

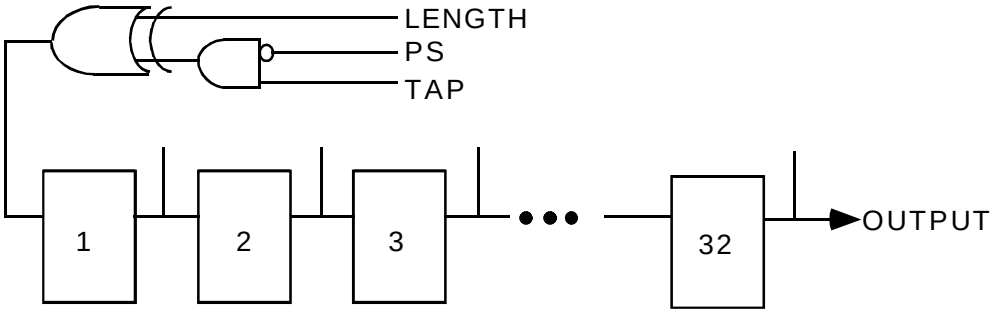
Using PRGD with ELST Enabled

If the elastic store is enabled (Ingress interface is in a Clock Slave mode) then the PRGD will operate on the data output from the ELST. This has two effects: first, when the framer is out-of-frame, the ELST Trouble Code overwrites the received data, and so patterns cannot be detected in the receive direction until the FRMR finds frame. If patterns must be detected while the FRMR is out-of-frame, then the UNF bit must be set in the Receive Line options Register (Reg. 00H in each octant), disabling the FRMR from finding frame but allowing the data to pass through ELST untouched. The second effect is that if slips occur in the ELST, then the PRGD will be forced to re-synchronize to the incoming pattern.

Note that the default ELST trouble code, which is all-ones, is a repetitive pattern of every length, so the PRGD will synchronize to it automatically if repetitive patterns are being detected.

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in the Figure 26 below:

Figure 26 - PRGD Pattern Generator



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0]), when the PS bit is low. When PS is high, the pattern

detector functions as a recirculating shift register, with length determined by PL[4:0].

Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in the two tables below:

Table 12 - Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	PL	PT	PI#1	PI#2	PI#3	PI#4	TINV	RINV
2^3 -1	02	00	FF	FF	FF	FF	0	0
2^4 -1	03	00	FF	FF	FF	FF	0	0
2^5-1	04	01	FF	FF	FF	FF	0	0
2^6 -1	05	04	FF	FF	FF	FF	0	0
2^7 -1	06	00	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	06	03	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Deactivate)	06	03	FF	FF	FF	FF	1	1
2^9 -1 (O.153)	08	04	FF	FF	FF	FF	0	0
2^{10} -1	09	02	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	0A	08	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0E	0D	FF	FF	FF	FF	1	1
2^{17} -1	10	02	FF	FF	FF	FF	0	0
2^{18} -1	11	06	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	13	02	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	13	10	FF	FF	FF	FF	0	0
2^{21} -1	14	01	FF	FF	FF	FF	0	0

Pattern Type	PL	PT	PI#1	PI#2	PI#3	PI#4	TINV	RINV
2^{22} -1	15	00	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	16	11	FF	FF	FF	FF	1	1
2^{25} -1	18	02	FF	FF	FF	FF	0	0
2^{28} -1	1B	02	FF	FF	FF	FF	0	0
2^{29} -1	1C	01	FF	FF	FF	FF	0	0
2^{31} -1	1E	02	FF	FF	FF	FF	0	0

Table 13 - Repetitive Pattern Generation (PS bit = 1)

Pattern Type	PL	PT	PI#1	PI#2	PI#3	PI#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	01	00	FE	FF	FF	FF	0	0
Double alternating ones/zeros	03	00	FC	FF	FF	FF	0	0
3 in 24	17	00	22	00	20	FF	0	0
1 in 16	0F	00	01	00	FF	FF	0	0
1 in 8	07	00	01	FF	FF	FF	0	0
1 in 4	03	00	F1	FF	FF	FF	0	0
Inband loopback activate	04	00	F0	FF	FF	FF	0	0
Inband loopback deactivate	02	00	FC	FF	FF	FF	0	0

Notes for the Pseudo Random and Repetitive Pattern Generation Tables:

1. The PS bit and the QRSS bit are contained in the PRGD Control register
2. PL = Pattern Length Register
3. PT = Pattern Tap Register
4. PI#1 = Pattern Insertion #1 Register

5. PI#2 = Pattern Insertion #2 Register
6. PI#3 = Pattern Insertion #3 Register
7. PI#4 = Pattern Insertion #4 Register
8. The TINV bit and the RINV bit are contained in the control register

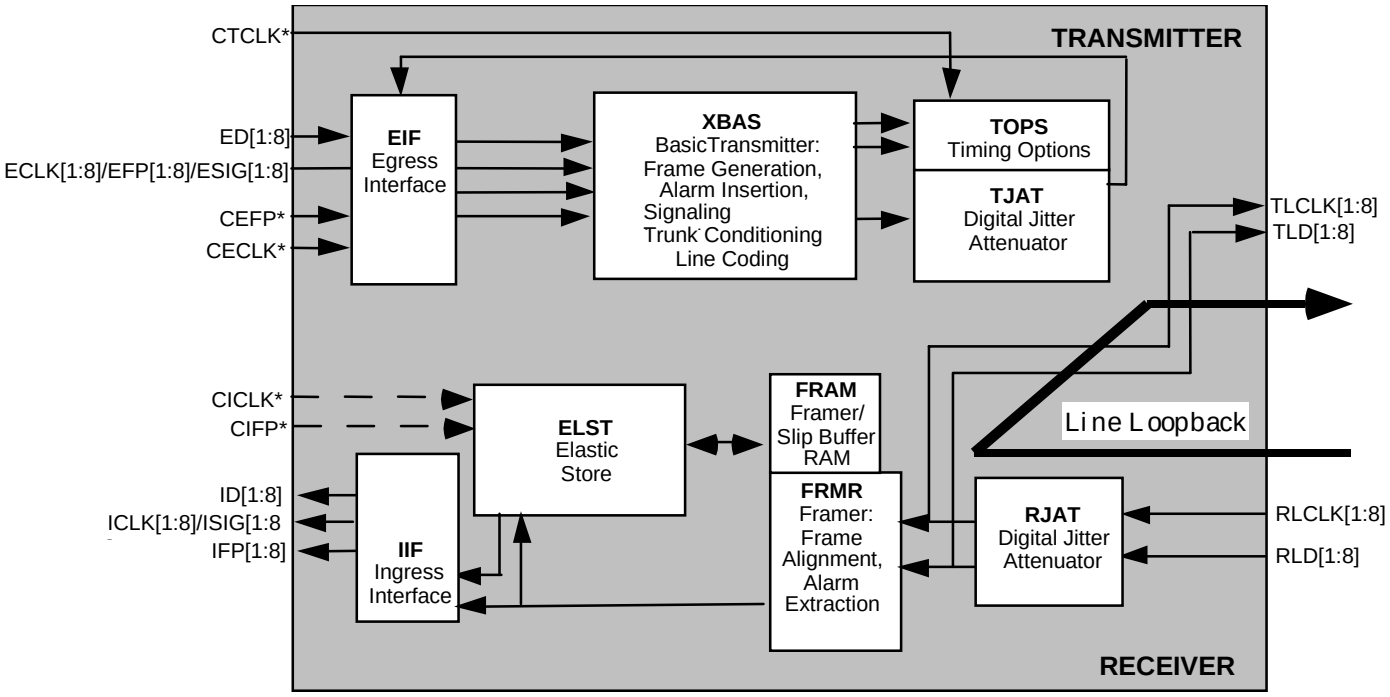
14.5 Using the Loopback Modes

The TOCTL provides three loopback modes to aid in network and system diagnostics. Line loopback can be initiated at any time via the µP interface, but is usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the framer. The payload can also be looped-back on a per-DS0 basis to allow network testing without taking an entire DS1 off-line.

14.5.1 Line Loopback

When LINE loopback (LINELB) is initiated by writing 10H to the Master Diagnostics Register (00AH, 08AH, 10AH, 18AH, 20AH, 28AH, 30AH, and 38AH), the appropriate T1 framer in the TOCTL is configured to internally connect the jitter-attenuated clock and data from the RJAT to the transmit line clock and data, TLD[x] and TLCLK[x]. The RJAT may be bypassed if desired. Conceptually, the data flow through a single T1 framer in this loopback condition is illustrated in Figure 27:

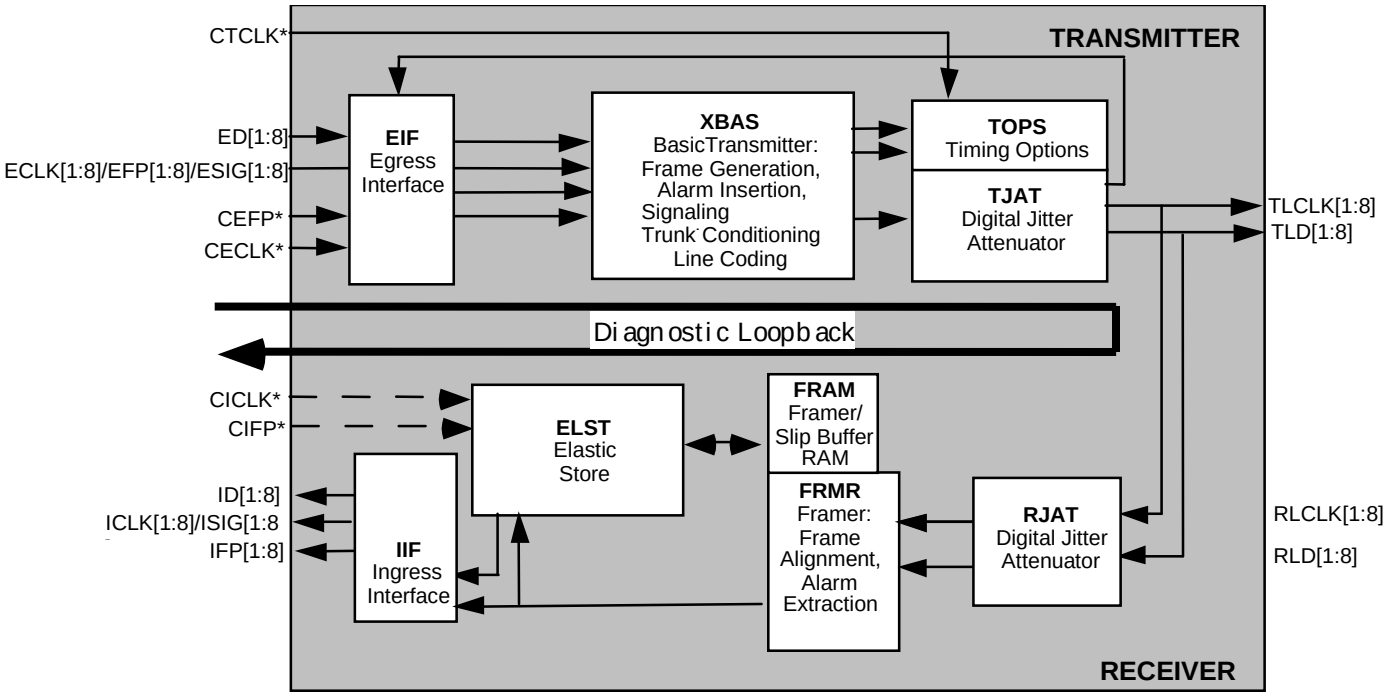
Figure 27 - Line Loopback



14.5.2 Diagnostic Digital Loopback

When Diagnostic Digital loopback (DDLB) is initiated by writing 04H to the Master Diagnostics Register (00AH, 08AH, 10AH, 18AH, 20AH, 28AH, 30AH, and 38AH), the appropriate T1 framer in the TOCTL is configured to internally connect its line clock and data (TLD[x] and TLCLK[x]) to the receive line clock and data (RLD[x] and RLCLK[x]) The data flow through a single T1 framer in this loopback condition is illustrated in Figure 28:

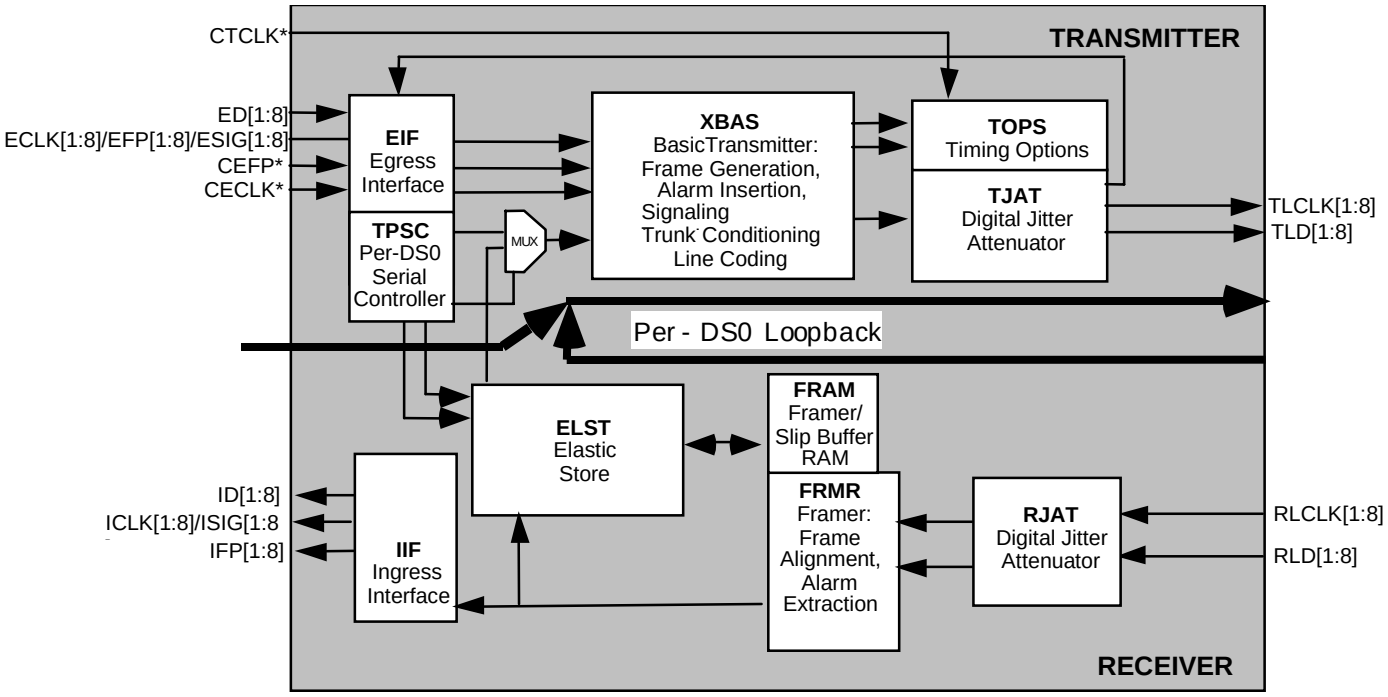
Figure 28 - Diagnostic Digital Loopback



14.5.3 Per-DS0 Loopback

The T1 payload may be looped-back on a per-DS0 basis through the use of the TPSC. If all DS0s are looped-back, the result is very similar to Payload Loopback on the PM4344 TQUAD. In order for per-DS0 loopback to operate correctly, the Ingress Interface must be in Clock Master mode, or else CIFP and CICLK must be connected to CEFP and CECLK, respectively. The LOOP bit must be set to logic 1 in the TPSC Internal Registers for each DS0 desired to be looped back, and the PCCE bit must be set to logic 1 in the TPSC Configuration register. When all these configurations have been made, the ingress DS0 channels selected will overwrite their corresponding egress DS0 channels; the remaining egress DS0 channels will pass through intact. Note that because the egress and ingress streams will not be superframe aligned, that any robbed-bit signaling in the ingress stream may not fall in the correct frame once looped-back, and that egress robbed-bit signaling will overwrite the looped-back channel data if signaling insertion is enabled. The data flow in per-DS0 loopback is illustrated in Figure 29:

Figure 29 - Per-DS0 Loopback



14.6 Using the Per-DS0 Serial Controllers

14.6.1 Initialization

Before the TPSC (RPSC) block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register (registers 030H, 0B0H, 130H, 1B0H, 230H, 2B0H, 330H, 3B0H for TPSC; 050H, 0D0H, 150H, 1D0H, 250H, 2D0H, 350H, 3D0H for RPSC) to logic 0. Then, all 72 locations of the TPSC (RPSC) must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 1.

14.6.2 Direct Access Mode

Direct access mode to the TPSC or RPSC is not used in the TOCTL. However, direct access mode is selected by default whenever the TOCTL is reset. The IND

bit within the TPSC and RPSC Configuration Registers must be set to logic 1 after a reset is applied.

14.6.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC or RPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the TPSC or RPSC is processing an access request; when the BUSY bit is logic 0, the TPSC or RPSC has completed the request.

The indirect write programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write the channel data to the TPSC (RPSC) Channel Indirect Data Buffer register.

3. Write RWB=0 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.

5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write RWB=1 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.

4. Read the requested channel data from the TPSC (RPSC) Channel Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

14.7 Using the Transmit Digital Jitter Attenuator

In using TJAT, it is important to choose the appropriate divisors for the phase comparison between the selected reference clock and the generated smooth TLCLK[x[.

14.7.1 Default Application

Upon reset, the TOCTL default condition provides jitter attenuation with TLCLK[x] referenced to the common egress clock, CECLK. The TJAT SYNC bit is also logic 1 by default. TJAT is configured to divide its input clock rate, CECLK, and its output clock rate, TLCLK[x], both by 48, which is the maximum length of the FIFO. These divided down clock rates are then used by the phase comparator to update the TJAT DPLL. The phase delay between CECLK and TLCLK[x] is synchronized to the physical data delay through the FIFO. For example, if the phase delay between BTCLK[x] and TCLKO[x] is 12UI, the FIFO will be forced to lag its output data 12 bits from its input data.

The default mode works well with the common egress clock running at 1.544MHz.

14.7.2 Data Burst Application

In applications where the 2.048MHz transmit backplane rate (or a higher backplane rate with external gapping) is used, a few factors must be considered to adequately filter the resultant TLCLK[x] into a smooth 1.544MHz clock. The magnitude of the phase shifts in the incoming bursty data are too large to be properly attenuated by the PLL alone. However, the magnitudes, and the frequency components of these phase shifts are known, and are most often multiples of 8 kHz.

When using the 2.048MHz transmit backplane rate, the input clock to TJAT is a gapped version of the 2.048MHz CECLK. The phase shifts of the input clock with respect to the generated TLCLKx] in this case are large, but when viewed over a longer period, such as a frame, there is little net phase shift. Therefore, by choosing the divisors appropriately, the large phase shifts can be filtered out, leaving a stable reference for the DPLL to lock onto. In this application, the N1 and N2 divisors should be changed to C0H (i.e. divisors of 193). Consequently, the frequency of the clock inputs to the phase discriminator in the PLL is 8 kHz. The TJAT SYNC option must be disabled, since the divisor magnitude of 193 is not an integer multiple of the FIFO length, 48.

The self-centering circuitry of the FIFO should be enabled by setting the CENT register bit. This sets up the FIFO read pointer to be at least 4 UI away from the end of the FIFO registers, and then disengages. Should variations in the frequency of input clock or the output clock cause the read pointer to drift to within one unit interval of FIFO overflow or underflow, the pointer will be incrementally pushed away by the LIMIT control without any loss of data.

With SYNC disabled, CENT and LIMIT enabled, the maximum tolerable phase difference between the bursty input clock and the smooth TLCLK[x] is 40UI. Phase wander between the two clock signals is compensated for by the LIMIT control.

14.7.3 Elastic Store Application

In multiplex applications where the jitter attenuation is not required, the TJAT FIFO can be used to provide an elastic store function. For example, in an M12 application, the data is written into the FIFO at 1.544MHz and the data is read out of the FIFO with a gapped DS2 rate clock applied on CTCLK. In this configuration, the Timing Options OCLKSEL bit should be programmed to 1, and the CTCLKSEL bit should be programmed to 1. Also, the TJAT SYNC and LIMIT bits should be disabled and the CENT bit enabled. This provides the maximum phase difference between the input clock and the gapped output clock of 40UI. The maximum jitter and wander between the two clocks is 8UIp-p.

14.7.4 Alternate TLCLK Reference Application

In applications where TLCLK[x] is referenced to an Nx8 kHz clock source applied on CTCLK, TJAT can be configured by programming the output clock divisor, N2, to C0H and the input clock divisor, N1, to the value (N-1). The resultant input clocks to the phase comparator are both 8kHz. The TJAT SYNC and LIMIT bits should be disabled in this configuration.

14.8 Isolating an Interrupt

When the INTB pin goes low, the following procedure may be used to isolate the interrupt source.

1. Read the Interrupt ID register (Register 00EH). The bit corresponding to any framer that has an outstanding interrupt will be logic 1.

2. Read the Interrupt Source Registers (Registers 008H and 009H for each framer) for the framer that caused the interrupt. For instance, if framer 5 caused the interrupt, then registers 288H and 289H would be read. The bit

corresponding to any block with an outstanding interrupt will be set to logic 1 in these registers.

3. Read the register(s) containing the interrupt status bits of the interrupting block in order to determine the event causing the interrupt. A typical block interrupt has two related bits: an enable bit (EVENTE for instance) and an interrupt status bit (EVENTI for instance). EVENTI will go to logic 1 when the triggering event occurs, and goes low when the register containing it is read; the setting of EVENTE has no effect on the value of EVENTI. However, a chip interrupt will only be caused if EVENTE is logic 1 and EVENTI is logic 1. Thus, both the interrupt status bit(s) and their respective enables may need to be read in order to determine which event caused an interrupt. Specific interrupt setups may differ from this model, however.

14.9 Using the Performance Monitor Counter Values

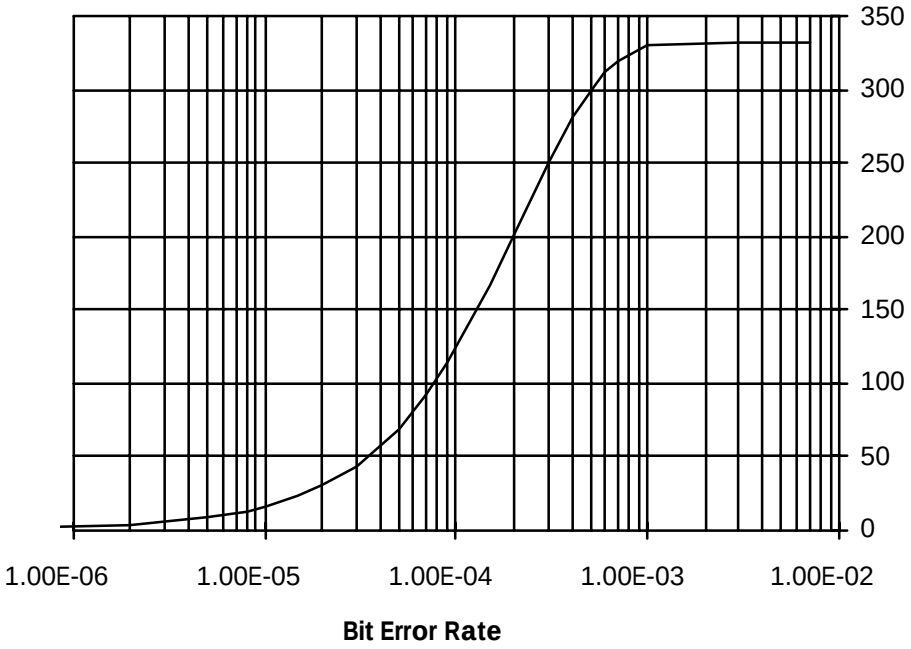
All PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval is very small. For ESF frame format, the FER and BEE error counts are incapable of saturating over a one second interval unless the FRMR is locked in-frame, and even then the likelihood is negligible for BER much less than 10^{-1}. For SF format, the BEE and FER counts are identical, but the FER counter is smaller and should be ignored. The BEE count is incapable of saturating unless the FRMR is locked in-frame, and even then the likelihood of saturating in one second at a $5x10^{-1}$ bit error ratio is less than 2% in SF format; at 10^{-1} or lower BER the odds of saturation are zero for all practical purposes. The relationship between BER and the odds of the OOF and COFA counters saturating is complicated, but at a 10^{-3} BER the probability is less than 0.001% in either format.

In ESF mode, the BEE count (which counts CRC-6 errors) is effective at bit error rates below 10^{-3}. The bit error rate can be calculated from the one-second PMON BEE count by the following equation:

$$\textbf{Bit Error Rate} = 1 - 10^{\left(\frac{\log\left(1 - \frac{24}{8000}\,BEE\right)}{24 * 193}\right)}$$

The following graph illustrates the expected BEE Count for a range of Bit Error Ratios.

Figure 30 - BEE Count Expected vs Bit Error Rate for ESF



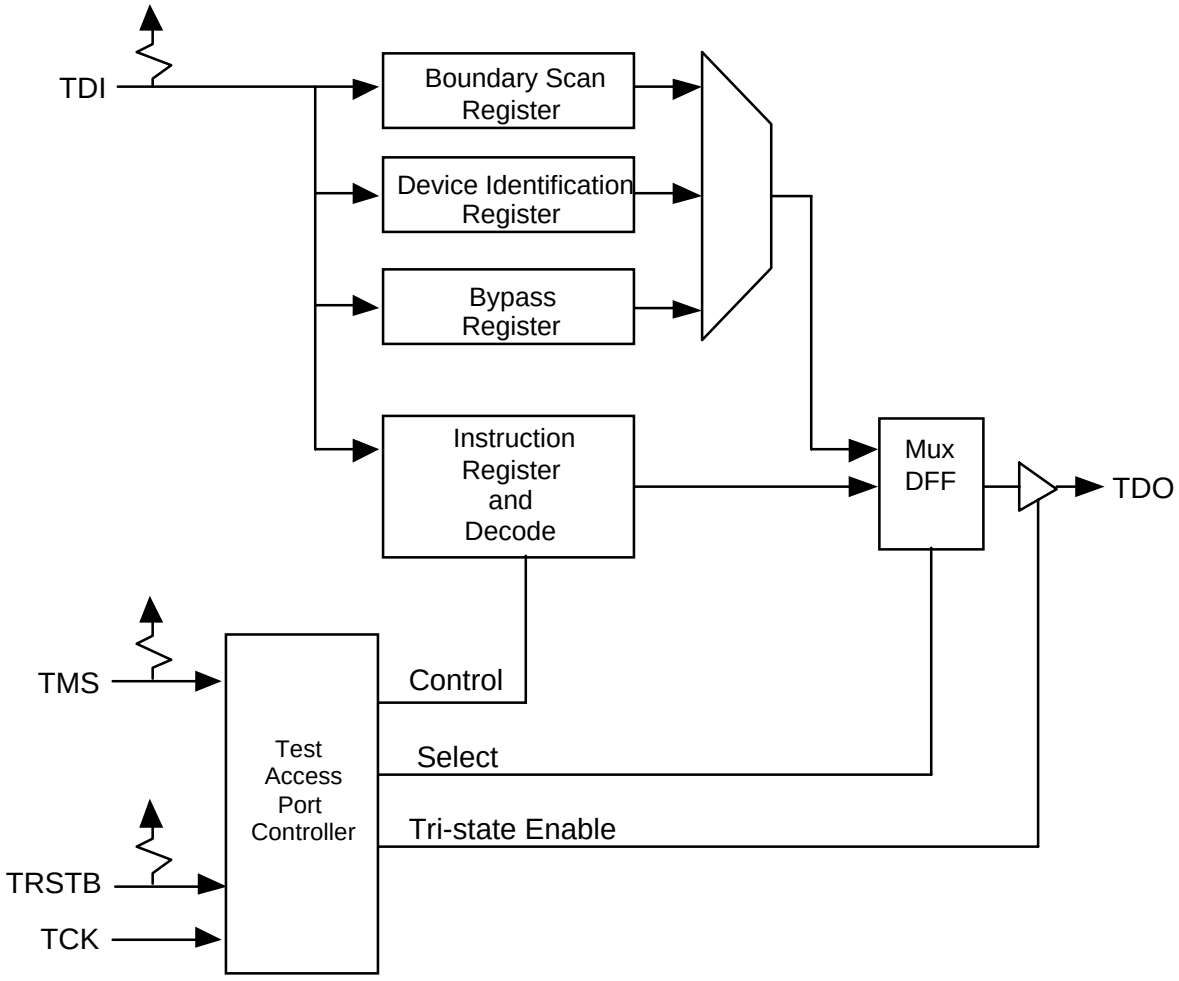
The ESF FER count accumulates framing-pattern errors. There are 2000 framing pattern bits in a second, so the bit error ratio is equal to approximately FER/2000. However, as the bit error rate rises above $5x10^{-3}$, the chance of losing frame at least once a second becomes significant. Because the PMON does not count errors during out-of-frame conditions, this will make the FER count slightly optimistic. Each reframing event will be recorded by the OOF counter, and there is a 99% probability that any given OOF event lasts for less than 15ms.

The SF BEE count also accumulates framing-pattern errors, for which there are 8000 opportunities in a second. Thus, the bit error ratio is equal to approximately BEE/8000. However, as the bit error rate rises above $2x10^{-3}$, OOF events begin to occur infrequently. Because the PMON does not count errors during out-of-frame conditions, this will make the BEE count slightly optimistic. Each reframing event, however, will be recorded by the OOF counter, and there is a 99% probability that any given OOF event lasts for less than 4.4ms.

14.10 JTAG Support

The TOCTL supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 31.

Figure 31 - Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register

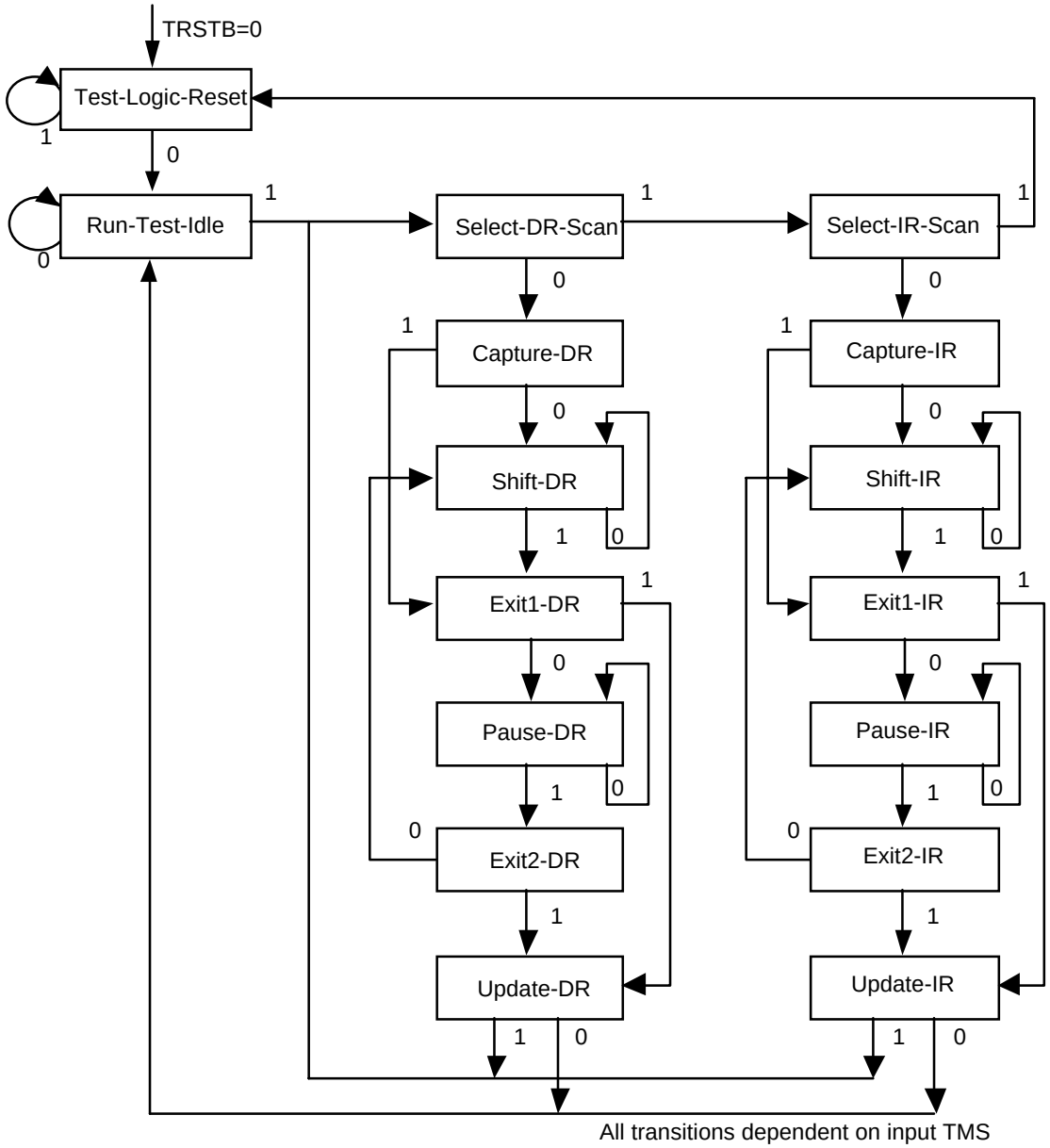
and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input TDI to primary output TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary TMS. The finite state machine is shown in Figure 32.

Figure 32 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP

controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input TDI and output TDO.

BYPASS

The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out TDO using the Shift-DR state.

Boundary Scan Register

The boundary scan register is made up of 120 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the pages which follow. The first 32 cells (120 down to 89) form the ID code register, and carry the code 043880CD. The remaining cells also have values which may be captured during the idcode instruction and shifted out if desired; these are included in brackets for reference. The cells are arranged as follows:

Table 14 - Boundary Scan Register

Pin/ Enable	Register Bit	Cell Type	I.D Bit.	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
HIZ[2,3]	120	OUT_CELL	0	IFP8	54	OUT_CELL	(0)
RLD1	119	IN_CELL	0	ISIG8	53	OUT_CELL	(0)
RLCLK1	118	IN_CELL	0	ID8	52	OUT_CELL	(0)
RLD2	117	IN_CELL	1 / 0 [4]	IFP7	51	OUT_CELL	(0)
RLCLK2	116	IN_CELL	0	ISIG7	50	OUT_CELL	(0)
RLD3	115	IN_CELL	1	ID7	49	OUT_CELL	(0)
RLCLK3	114	IN_CELL	0	IFP6	48	OUT_CELL	(0)
RLD4	113	IN_CELL	0	ISIG6	47	OUT_CELL	(0)
RLCLK4	112	IN_CELL	0	ID6	46	OUT_CELL	(0)
TLD1	111	OUT_CELL	0	IFP5	45	OUT_CELL	(0)
TLCLK1	110	OUT_CELL	1	ISIG5	44	OUT_CELL	(0)

Pin/ Enable	Register Bit	Cell Type	I.D Bit.	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
TLD2	109	OUT_CELL	1	ID5	43	OUT_CELL	(0)
TLCLK2	108	OUT_CELL	1	IFP4	42	OUT_CELL	(0)
TLD3	107	OUT_CELL	0	ISIG4	41	OUT_CELL	(0)
TLCLK3	106	OUT_CELL	0	ID4	40	OUT_CELL	(0)
TLD4	105	OUT_CELL	0	IFP3	39	OUT_CELL	(0)
TLCLK4	104	OUT_CELL	1	ISIG3	38	OUT_CELL	(0)
TLD5	103	OUT_CELL	0	ID3	37	OUT_CELL	(0)
TLCLK5	102	OUT_CELL	0	IFP2	36	OUT_CELL	(0)
TLD6	101	OUT_CELL	0	ISIG2	35	OUT_CELL	(0)
TLCLK6	100	OUT_CELL	0	ID2	34	OUT_CELL	(0)
TLD7	99	OUT_CELL	0	IFP1	33	OUT_CELL	(0)
TLCLK7	98	OUT_CELL	0	ISIG1	32	OUT_CELL	(0)
TLD8	97	OUT_CELL	0	ID1	31	OUT_CELL	(0)
TLCLK8	96	OUT_CELL	1	ESIG8	30	IO_CELL	(0)
RLD5	95	IN_CELL	1	ESIG_OEB8 [1]	29	OUT_CELL	(0)
RLCLK5	94	IN_CELL	0	ED8	28	IN_CELL	(1)
RLD6	93	IN_CELL	0	ESIG7	27	IO_CELL	(0)
RLCLK6	92	IN_CELL	1	ESIG_OEB7 [1]	26	OUT_CELL	(0)
RLD7	91	IN_CELL	1	ED7	25	IN_CELL	(1)
RLCLK7	90	IN_CELL	0	ESIG6	24	IO_CELL	(0)
RLD8	89	IN_CELL	1	ESIG_OEB6 [1]	23	OUT_CELL	(0)
RLCLK8	88	IN_CELL	(0)	ED6	22	IN_CELL	(1)
RSTB	87	IN_CELL	(0)	ESIG5	21	IO_CELL	(0)
INTB	86	OUT_CELL	(0)	ESIG_OEB5 [1]	20	OUT_CELL	(0)
D0	85	IO_CELL	(0)	ED5	19	IN_CELL	(1)
D0_OEB [1]	84	OUT_CELL	(0)	ESIG4	18	IO_CELL	(0)
D1	83	IO_CELL	(0)	ESIG_OEB4 [1]	17	OUT_CELL	(0)
D1_OEB [1]	82	OUT_CELL	(0)	ED4	16	IN_CELL	(1)
D2	81	IO_CELL	(0)	ESIG3	15	IO_CELL	(0)
D2_OEB [1]	80	OUT_CELL	(0)	ESIG_OEB3 [1]	14	OUT_CELL	(0)
D3	79	IO_CELL	(0)	ED3	13	IN_CELL	(1)
D3_OEB [1]	78	OUT_CELL	(0)	ESIG2	12	IO_CELL	(0)

Pin/ Enable	Register Bit	Cell Type	I.D Bit.	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
D4	77	IO_CELL	(0)	ESIG_OEB2 [1]	11	OUT_CELL	(0)
D4_OEB [1]	76	OUT_CELL	(0)	ED2	10	IN_CELL	(1)
D5	75	IO_CELL	(0)	ESIG1	9	IO_CELL	(0)
D5_OEB [1]	74	OUT_CELL	(0)	ESIG_OEB1 [1]	8	OUT_CELL	(0)
D6	73	IO_CELL	(0)	ED1	7	IN_CELL	(1)
D6_OEB [1]	72	OUT_CELL	(0)	XCLK	6	IN_CELL	(1)
D7	71	IO_CELL	(0)	CIFP	5	IN_CELL	(1)
D7_OEB [1]	70	OUT_CELL	(0)	CICLK	4	IN_CELL	(1)
ALE	69	IN_CELL	(0)	CEFP	3	IN_CELL	(1)
A[10:0]	68:58	IN_CELL	(0)	CECLK	2	IN_CELL	(1)
CSB	57	IN_CELL	(1)	CTCLK	1	IN_CELL	(1)
WRB	56	IN_CELL	(1)				
RDB	55	IN_CELL	(1)				

Notes:

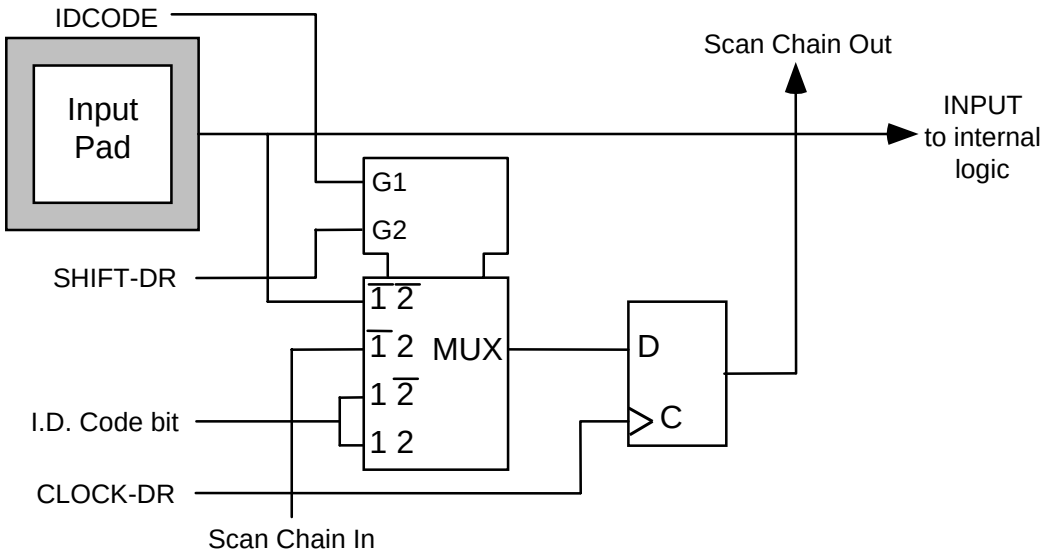
1. All OEB signals will set the corresponding bidirectional signal to an output when set low.

2. When set high, TLD[8:1], TLCLK[8:1], ID[8:1], ISIG[8:1], IFP[8:1], and INTB will be set to high impedance.

3. HIZ is the first bit in the boundary scan chain.

4. Bits 120:117 represent the revision identification code. “0000” indicates revision C. “0001” indicates revision E.

Figure 33 - Input Observation Cell (IN_CELL)



In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Figure 34 - Output Cell (OUT_CELL)

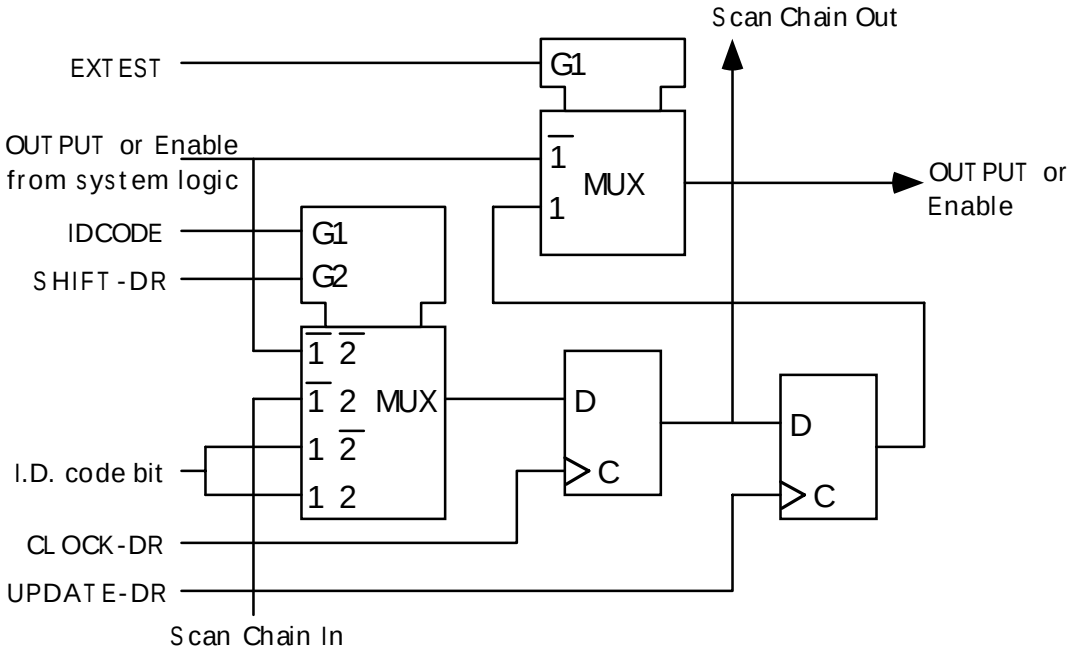


Figure 35 - Bidirectional Cell (IO_CELL)

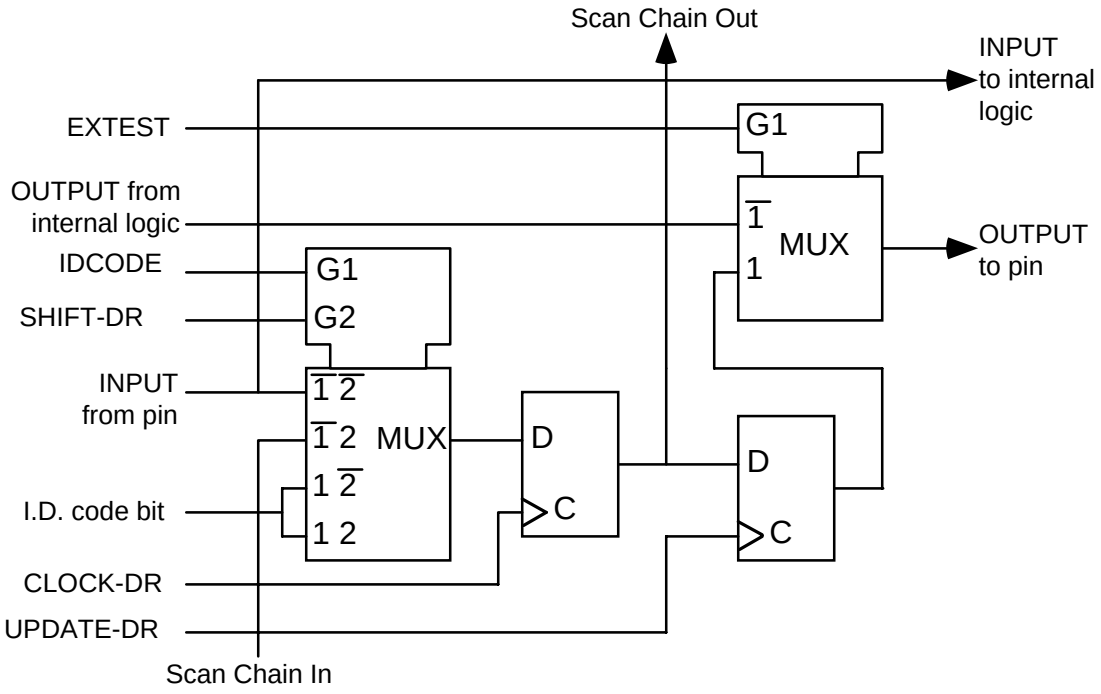
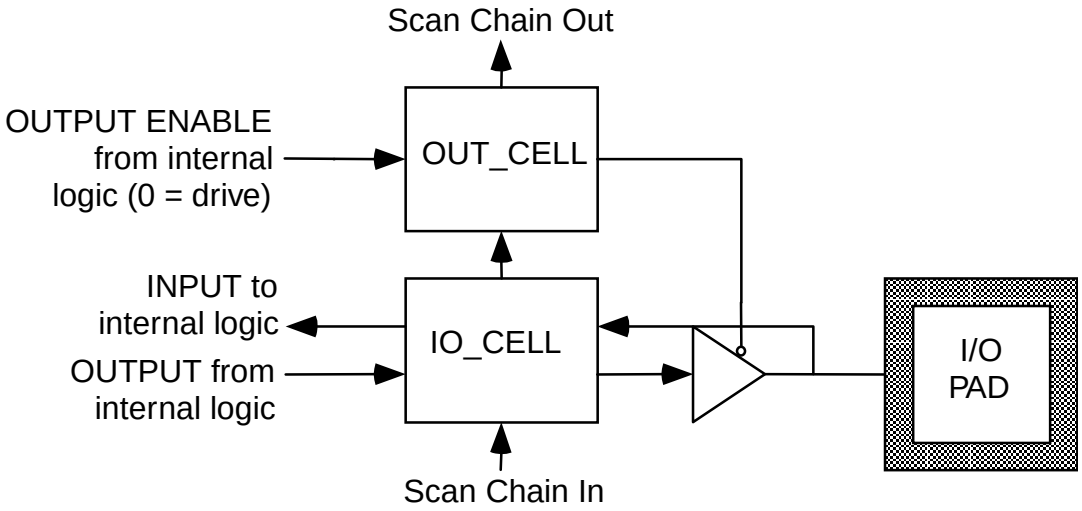


Figure 36 - Layout of Output Enable and Bidirectional Cells



15 ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal operating conditions.

Table 15 - TOCTL Absolute Maximum Ratings

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.3V to 4.6V
Voltage on BIAS with respect to GND	VDD - 0.3V to 5.5V
Voltage on Any Pin	-0.3V to BIAS + 0.3V
Static Discharge Voltage	±1000 V
Latchup current on any pin	±100 mA
Maximum DC current on any pin	±20 mA
Maximum Lead Temperature	+230 °C
Maximum Junction Temperature	+150 °C

16 D .C. CHARACTERISTICS

TA= -40° to +85°C, VDD=3.3V ±10%, VDD ≤ BIAS ≤ 5.5V

Table 16 - TOCTL D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
PHA, PHD	Power Supply	2.97	3.3	3.63	Volts	
BIAS	5V Tolerant Bias	VDD	5.0	5.5	Volts	
I_{BIAS}	Current into 5V Bias		6.0		µA	V_{BIAS} = 5.5V
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		BIAS	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage		0.25	0.4	Volts	V_{DD} = min, I_{OL} = -3 mA for high drive outputs[4] and -2 mA for others[3]
V_{OH}	Output or Bidirectional High Voltage	2.4			Volts	V_{DD} = min, I_{OL} = 3 mA for high drive outputs[4] and 2 mA for others[3]
V_{T+}	Reset Input High Voltage	2.0			Volts	
V_{T-}	Reset Input Low Voltage			0.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	
I_{ILPU}	Input Low Current[1,3]	-100	-60	-10	µA	V_{IL} = GND

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IL}	Input Low Current[2,3]	-10	0	+10	µA	V_{IL} = GND
I_{IH}	Input High Current[2,3]	-10	0	+10	µA	$V_{IH} = V_{BIAS}$
I_{DDOP}	Operating Current		80	150	mA	V_{DD} = 3.63 V, Outputs Unloaded, XCLK = 37.056 MHz
C_{IN}	Input Capacitance		5		pF	Excluding Package -RI Package 2pF Typ. -NI Package 1pF Typ.
C_{OUT}	Output Capacitance		5		pF	Excluding Package -RI Package 2pF Typ. -NI Package 1pF Typ.
C_{IO}	Bi-directional Capacitance		5		pF	Excluding Package -RI Package 2pF Typ. -NI Package 1pF Typ.

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. D[7:0], TLCLK[1:8], ISIG/ICLK[1:8], ESIG/ECLK/EFP[1:8].

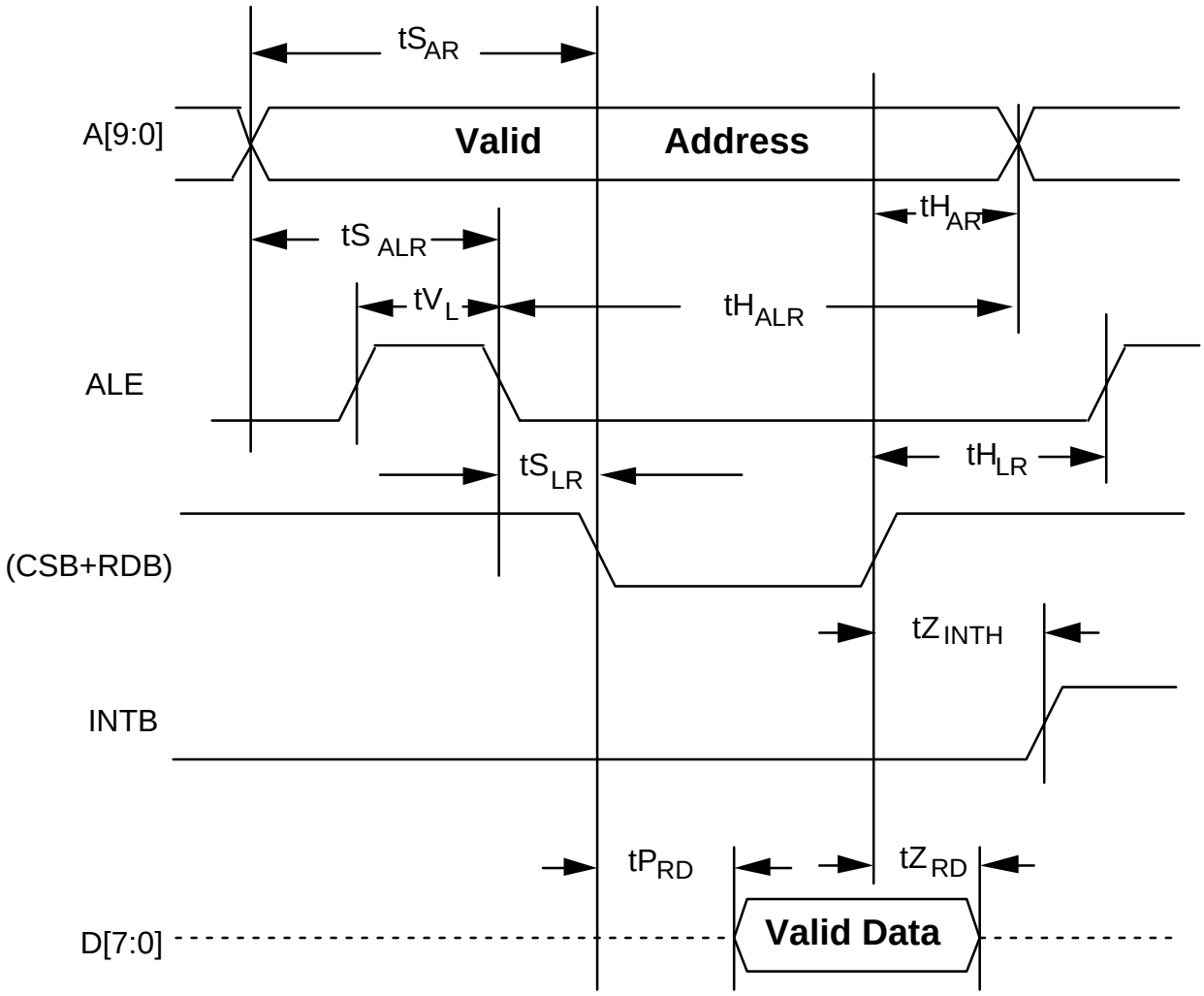
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=3.3V ±10%

Table 17 - Microprocessor Read Access (Figure 37)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB high		50	ns

Figure 37 - Microprocessor Read Access Timing



Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

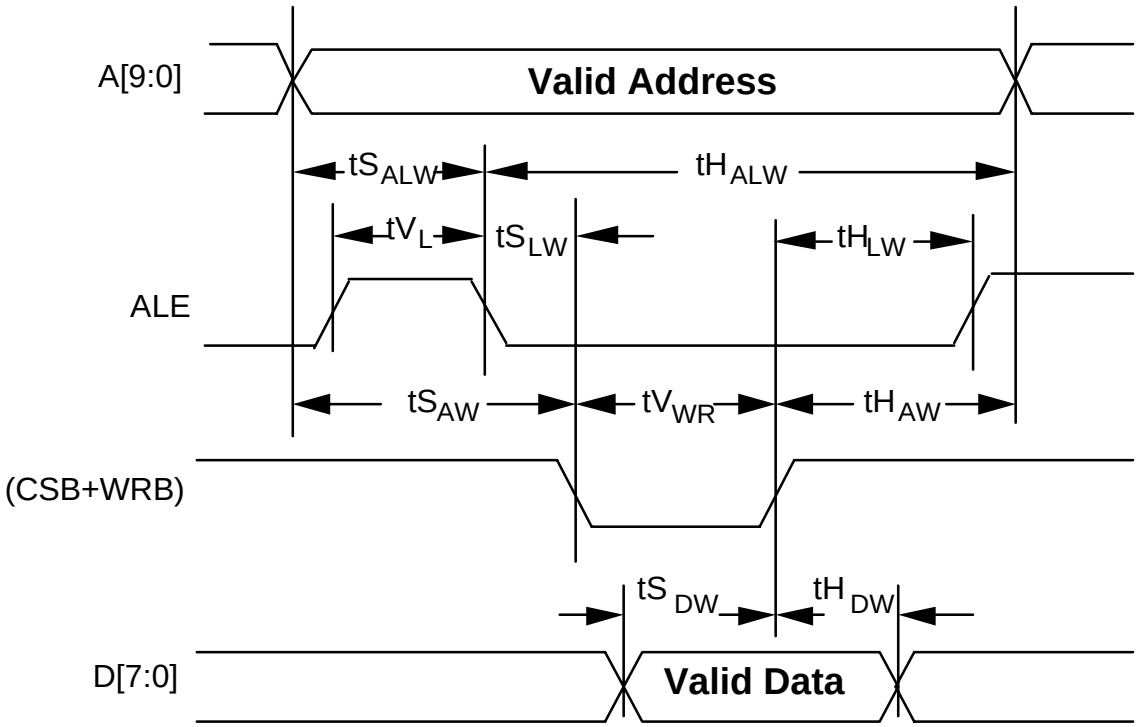
7. In non-multiplexed address/data bus architectures ALE can be held high; parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR}, tH_{LR} are not applicable.

8. Parameter tH_{AR} is not applicable when address latching is used.

Table 18 - Microprocessor Write Access (Figure 38)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	10		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 38 - Microprocessor Write Access Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE can be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW}, tH_{LW} are not applicable.
4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.
5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

18 TOCTL I/O TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=3.3V ±10%

Table 19 - XCLK=37.056 MHz Input (Figure 39)

Symbol	Description	Min	Max	Units
t_{LXCLK}	XCLK Low Pulse Width[4]	10		ns
t_{HXCLK}	XCLK High Pulse Width[4]	10		ns
t_{XCLK}	XCLK Period (typically 1/37.056 MHz ± 32 ppm)[5]	20		ns

Figure 39 - XCLK=37.056 MHz Input Timing

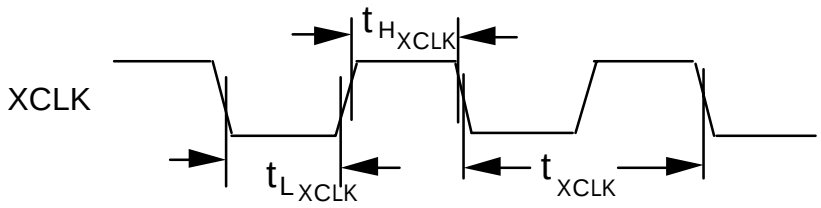


Table 20 - Egress Interface Timing - Clock Slave: EFP Enabled Mode (Figure 40)

Symbol	Description	Min	Max	Units
	Common Egress Clock Frequency[1,2](Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm)	1.5	2.1	MHz
$t1_{CECLK}$	Common Egress High Pulse Width[4]	167		ns
$t0_{CECLK}$	Common Egress Low Pulse Width[4]	167		ns
tS_{CECLK}	CECLK to Input Set-up Time[7,9]	20		ns
tH_{CECLK}	CECLK to Input Hold Time[8,9]	20		ns
tP_{EFP1}	CECLK to EFP[x] Propagation delay[9,10,11]		20	ns

Figure 40 - Egress Interface Timing - Clock Slave: EFP Enabled Mode

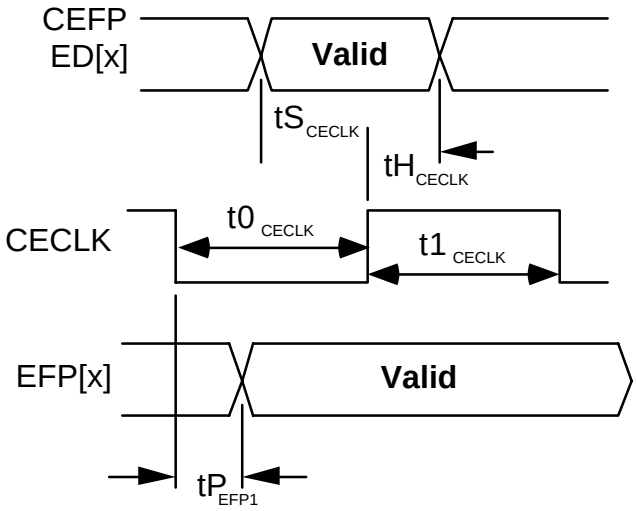


Table 21 - Egress Interface Timing - Clock Slave: External Signaling (Figure 41)

Symbol	Description	Min	Max	Units
	Common Egress Clock Frequency[1,2](Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm)	1.5	2.1	MHz
$t1_{CECLK}$	Common Egress High Pulse Width[4]	167		ns
$t0_{CECLK}$	Common Egress Low Pulse Width[4]	167		ns
tS_{CECLK}	CECLK to Input Set-up Time[7,9]	20		ns
tH_{CECLK}	CECLK to Input Hold Time[8,9]	20		ns

Figure 41 - Egress Interface Timing - Clock Slave: External Signaling Mode

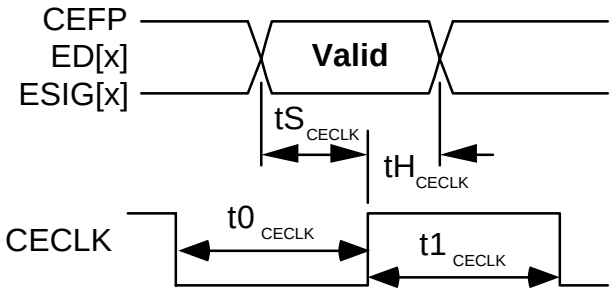


Table 22 - Egress Interface Timing - Clock Master: Full DS1 Figure 42)

Symbol	Description	Min	Max	Units
tSTLCLK	TLCLK[x] to ED[x] Set-up Time[7]	20		ns
tHTLCLK	TLCLK[x] to ED[x] Hold Time[8]	20		ns
tPEFP2	TLCLK[x]to EFP[x] Propagation delay[10,11]	-20	20	ns

Figure 42 - Egress Interface Timing - Clock Master: Full DS1 Mode

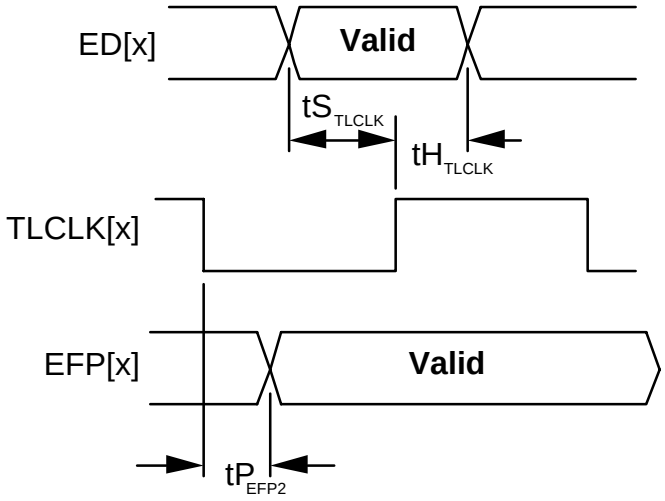


Table 23 - Egress Interface Input Timing - Clock Master : NxDS0 Mode (Figure 43)

Symbol	Description	Min	Max	Units
tSECLK	ECLK[x] to ED[x] Set-up Time[7,9]	20		ns
tHECLK	ECLK[x] to ED[x] Hold Time[8,9]	20		ns

Figure 43 - Egress Interface Input Timing - Clock Master : NxDS0 Mode

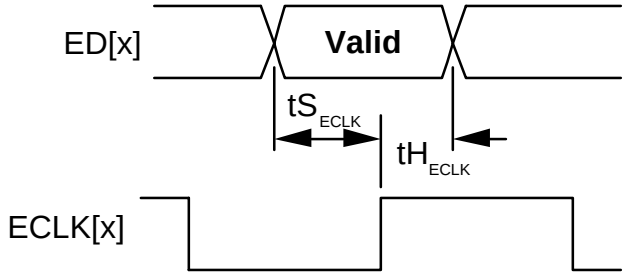


Table 24 - Ingress Interface Timing - Clock Slave Modes (Figure 44)

Symbol	Description	Min	Max	Units
	Common Ingress Clock Frequency[1,2] (Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm)	1.5	2.1	MHz
t1CICLK	Common Ingress High Pulse Width[4]	167		ns
t0CICLK	Common Ingress Low Pulse Width[4]	167		ns
tSCICLK	CICLK to CIFP Set-up Time[7,9]	20		ns
tHCICLK	CICLK to CIFP Hold Time[8,9]	20		ns
tPCICLK	CICLK to Ingress Output Prop. Delay[9,10,11]		20	ns

Figure 44 - Ingress Interface Timing - Clock Slave Modes

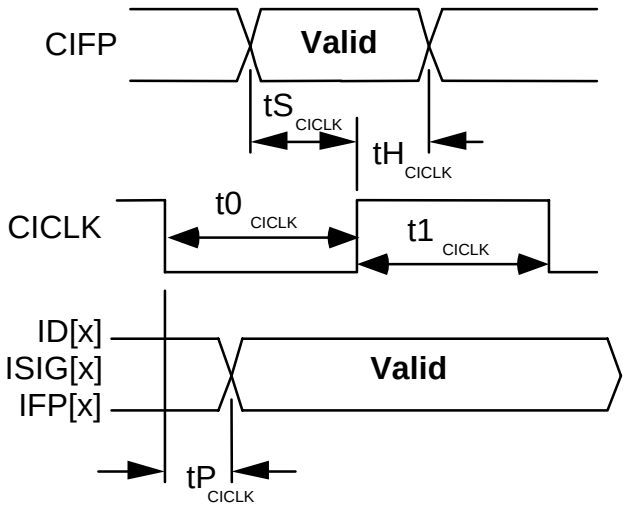


Table 25 - Ingress Interface Timing - Clock Master Modes (Figure 45)

Symbol	Description	Min	Max	Units
tP_{ICLK}	ICLK[x] to Ingress Output Prop. Delay[9,10,11]	20	20	ns

Figure 45 - Ingress Interface Timing - Clock Master Modes

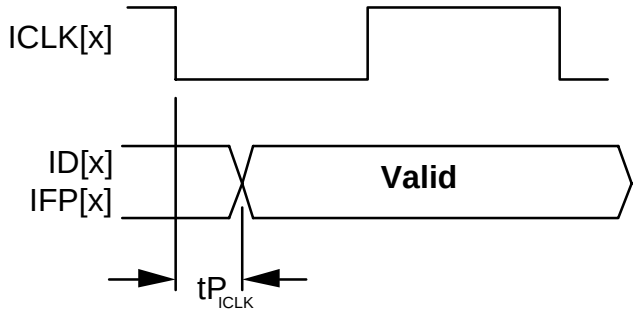


Table 26 - Transmit Line Interface Timing (Figure 46)

Symbol	Description	Min	Max	Units
	CTCLK Frequency (when used for TJAT REF), typically 1.544 MHz± 130 ppm[2,6]		1.545	MHz
t_{HCTCLK}	CTCLK High Duration[4] (when used for TJAT REF)	160		ns
t_{LCTCLK}	CTCLK Low Duration[4] (when used for TJAT REF)	160		ns
tP_{TLCLK}	TLCLK[x] to TLD[x] Output Prop. Delay[9,10,11]	-20	20	ns

Figure 46 - Transmit Line Interface Timing

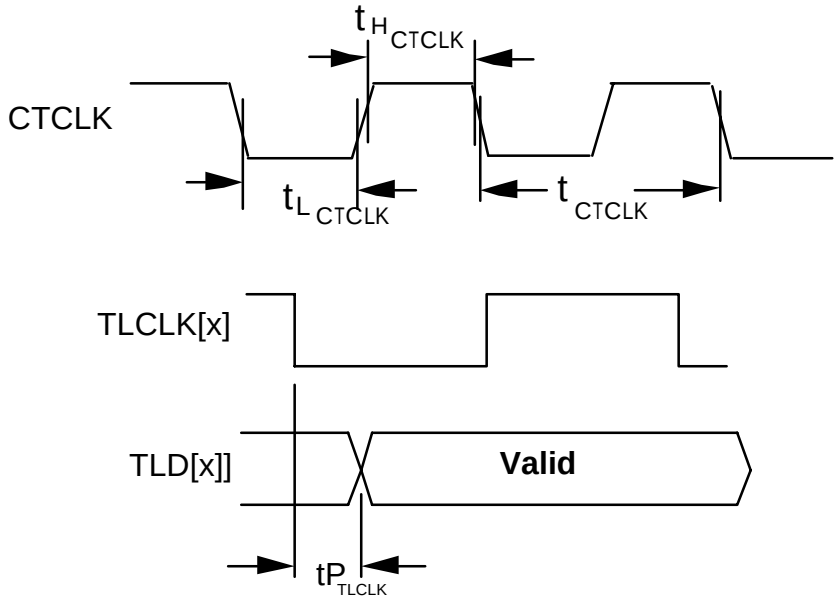


Table 27 - Receive Line Interface Timing (Figure 47)

Symbol	Description	Min	Max	Units
	RLCLK[x] Frequency, typically 1.544 MHz± 130 ppm[2,6]		1.545	MHz
$t_{HI_{RLCLK}}$	RLCLK[x] High Duration[4]	180		ns
$t_{LO_{RLCLK}}$	RLCLK[x] Low Duration[4]	180		ns
$t_{S_{RLCLK}}$	RLCLK[x] to RLD[x] Set-up Time[7,9]	20		ns
$t_{H_{RLCLK}}$	RLCLK[x] to RLD[x] Hold Time[8,9]	20		ns

Figure 47 - Line Interface Input Timing

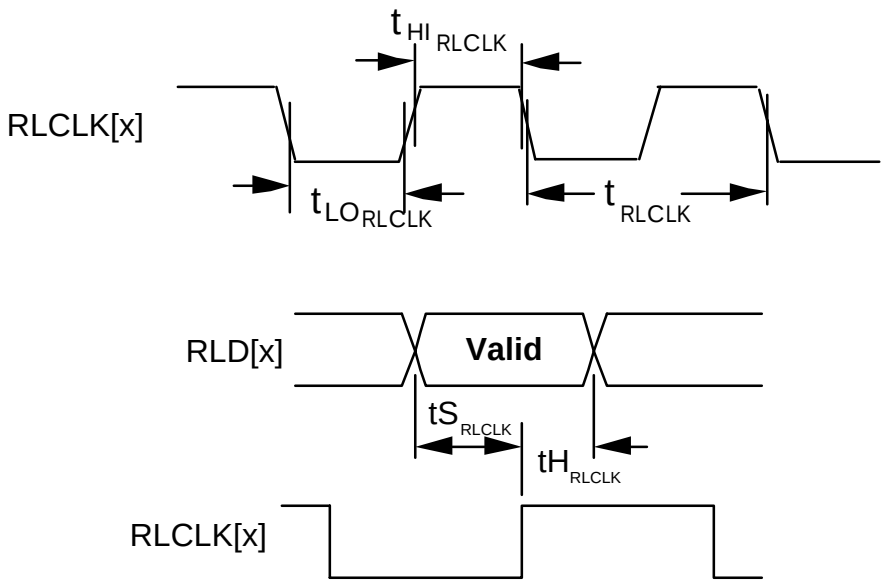
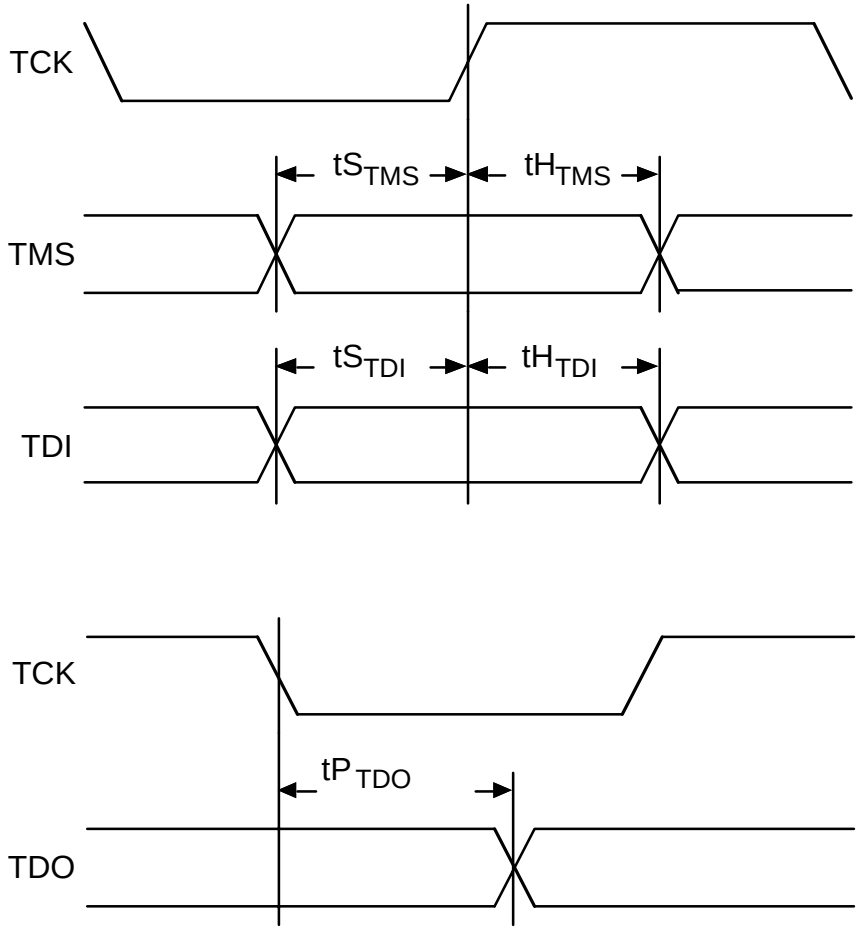


Table 28 - JTAG Port Interface Timing (Figure 48)

Symbol	Description	Min	Max	Units
tTCK	TCK Frequency		1	MHz
tDTCK	TCK Duty Cycle[4]	40	60	%
tS_{TMS}	TMS Set-up time to TCK[7]	50		ns
tH_{TMS}	TMS Hold time to TCK[8]	50		ns
tS_{TDI}	TDI Set-up time to TCK[7]	50		ns
tH_{TDI}	TDI Hold time to TCK[8]	50		ns
tP_{TDO}	TCK Low to TDO Valid[10,11]	2	50	ns

Figure 48 - JTAG Port Interface Timing Diagram



Notes on AC Timing:

1. CECLK and CICLK can be gapped and/or jittered clock signals subject to the minimum high and low times shown. These specifications correspond to nominal XCLK input frequencies.

2. Guaranteed by design for nominal XCLK input frequency (37.056 MHz ±100 ppm).

3. CTCLK can be a jittered clock signal subject to the minimum high and low times shown. These specifications correspond to nominal XCLK input frequency of 37.056 MHz ±100 ppm.

4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

5. XCLK frequency must be 24x the line rate ±32 ppm when TJAT is free-running or referenced to a derivative of XCLK. XCLK may be ± 100 ppm if an accurate reference is provided to TJAT. XCLK frequency may be as high as 50 MHz only if the line rate is increased to 1/24 of XCLK, or if both RJAT and TJAT are bypassed.

6. CTCLK[x] can be a jittered clock signal subject to the minimum high and low durations tH_{CTCLK}, tL_{CTCLK}. These durations correspond to nominal XCLK input frequency.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

9. Setup, hold, and propagation delay specifications are shown relative to the default active clock edge, but are equally valid when the opposite edge is selected as the active edge.

10. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

11. Output propagation delays are measured with a 50 pF load on all outputs.

19 ORDERING AND THERMAL INFORMATION

Table 29 - TOCTL Ordering Information

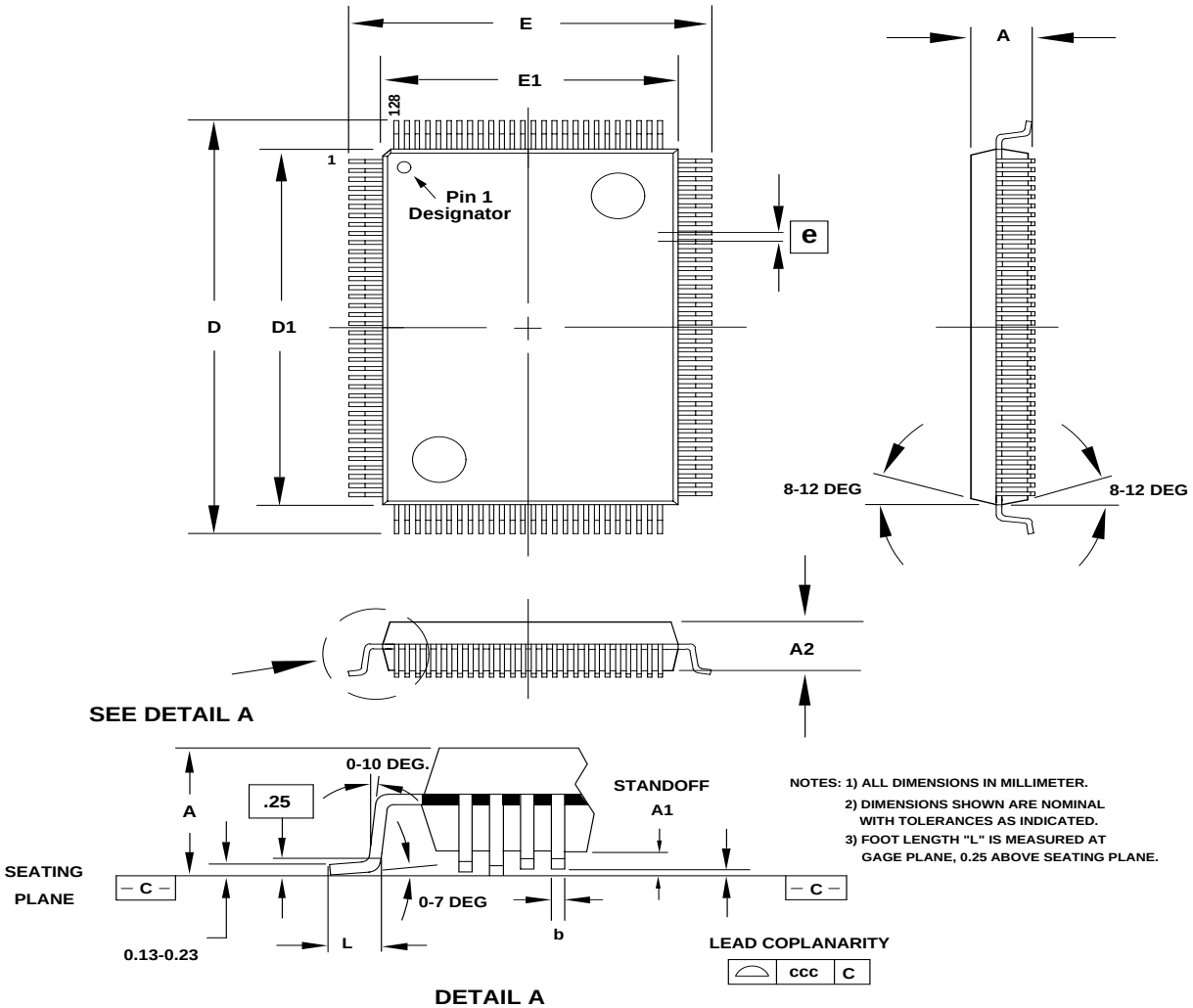
PART NO.	DESCRIPTION
PM4388-RI	128 Plastic Quad Flat Pack (PQFP)
PM4388-NI	128 Chip Array Ball Grid Array (CABGA)

Table 30 - TOCTL Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM4388-RI	-40°C to 85°C	47 °C/W	14 °C/W
PM4388-NI	-40°C to 85°C	50 °C/W	

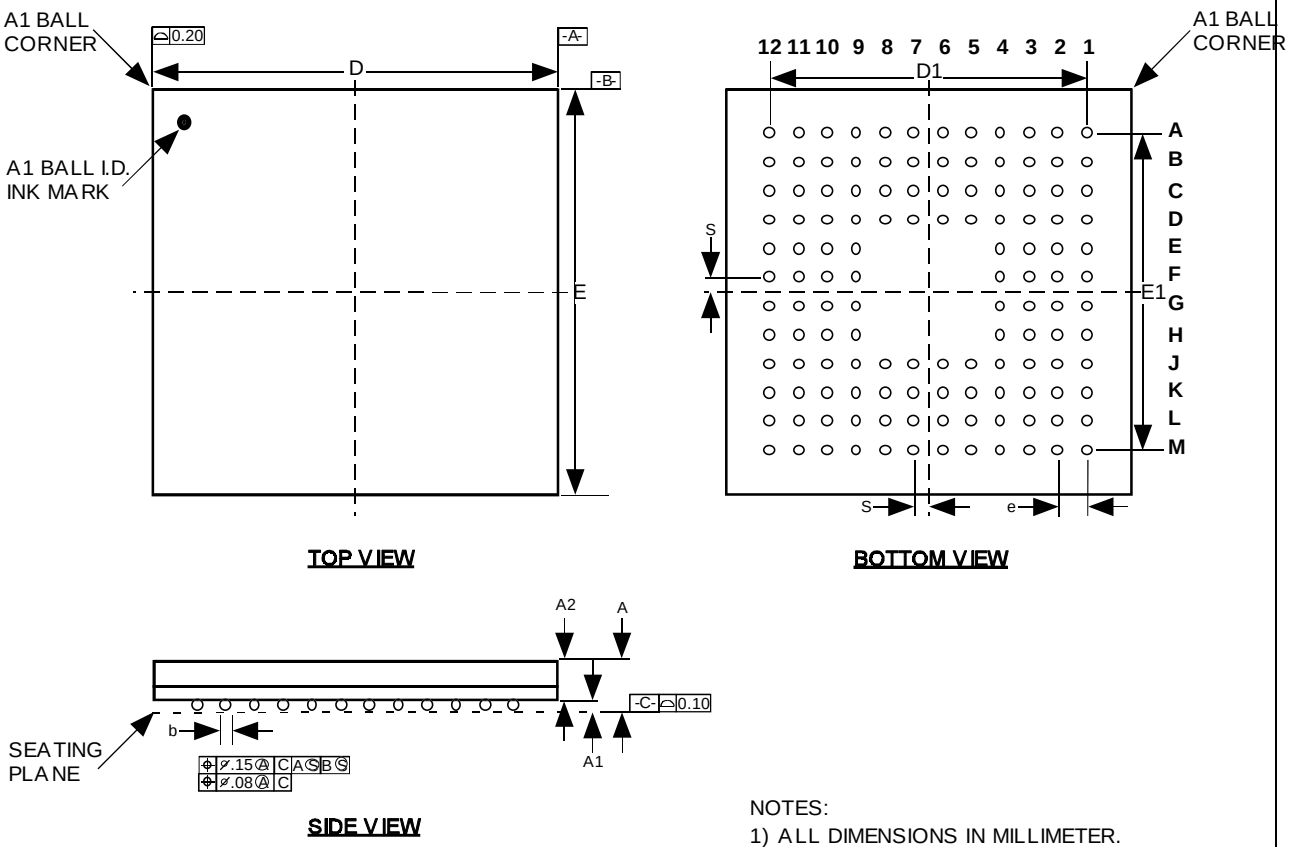
20 MECHANICAL INFORMATION

Figure 49 - 128 Pin Copper Leadframe Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 128 PIN METRIC RECTANGULAR PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 20 x 2.7 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.82	0.25	2.57	22.95	19.90	16.95	13.90	0.73		0.17	
Nom.			2.70	23.20	20.00	17.20	14.00	0.88	0.50	0.22	
Max.	3.40	0.53	2.87	23.45	20.10	17.45	14.10	1.03		0.27	0.10

Figure 50 - 128 Pin Chip Array Ball Grid Array (N Suffix):



NOTES:
1) ALL DIMENSIONS IN MILLIMETER.

PACKAGE TYPE : 128 CHIP ARRAY BALL GRID ARRAY - CABGA										
BODY SIZE : 11 X11 x 1.4 MM										
Dim.	A	A1	A2	D	D1	E	E1	b	e	S
Min.	1.30	0.31	0.99							
Nom.	1.40	0.36	1.04	11.00	8.80	11.00	8.80	0.46	0.80	0.40
Max.	1.50	0.41	1.09							

NOTES

NOTES

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