PMC-Sierra

PM3386
S/UNI®-2xGE

Dual Gigabit Ethernet Controller

FEATURES

- Two port full-duplex Gigabit Ethernet Controller with an industry standard POS-PHY Level 3™ system interface.
- Provides direct connection to optics.
- Connection to copper Gigabit Ethernet physical layer devices via two GMII interfaces.
- Incorporates dual SERDES, compatible to IEEE 802.3 1998 PMA physical layer specification.
- Supports dual IEEE 802.3 -1998 GMII/TBI interfaces for connection to copper Gigabit Ethernet physical layer devices.
- Provides dual standard IEEE 802.3 Gigabit Ethernet MACs for frame verification.
- Provides on-chip data recovery and clock synthesis.
- Provides eight unicast exact-match address filters to filter frames based on DA, SA, or VID.
- Each address filter can indicate whether to accept or discard based on a match.
- Provides 64-group multicast address filter.
- Internal 16 kbyte TX and 64 kbyte RX FIFOs to accommodate system latencies.
- SATURN® compatible interface for Packet-Over-SONET Physical Layer and Link Layer devices Level 3 (POS-PHY Level 3 system interface).
- Line side loopback for system level diagnostic capability.
- 16 bit generic microprocessor interface for device initialization, control, register and per port statistics access.

GIGABIT ETHERNET MAC

- Verifies frame integrity (FCS and length checks).
- Errored frames can be filtered or passed to a higher layer device.
- Automatic Base Page Autonegotiation, extended Autonegotiation (Next Page) supported via host.
- Egress Ethernet frame encapsulation (pad to minimum size, add preamble, IFG and CRC generation).
- Supports Ethernet 2.0, IEEE 802.3 LLC and IEEE 802.3 SNAP/LLC encoding formats, and VLAN tagged frames.
- Minimum frame size 64 bytes. Supports jumbo frames up to 9.6 kbytes.
- Supports big endian data formats.
- Programmable inter-packet gap (IPG).
- Loopback for diagnostic capability through GMAC.

FLOW CONTROL

- Option to support IEEE 802.3-1998 flow control at each Ethernet port.
- Programmable watermarks for full/empty FIFO conditions.
- Automatic generation of pause frames based on FIFO fill levels.
- Upper layer device can flow control Ethernet ports using side-band or host signaling to cause generation of a Pause frame.
- Provides per-port side-band Pause state indication for upstream devices.
- Loss-less flow control on all valid frames up to 9.6 kbytes.

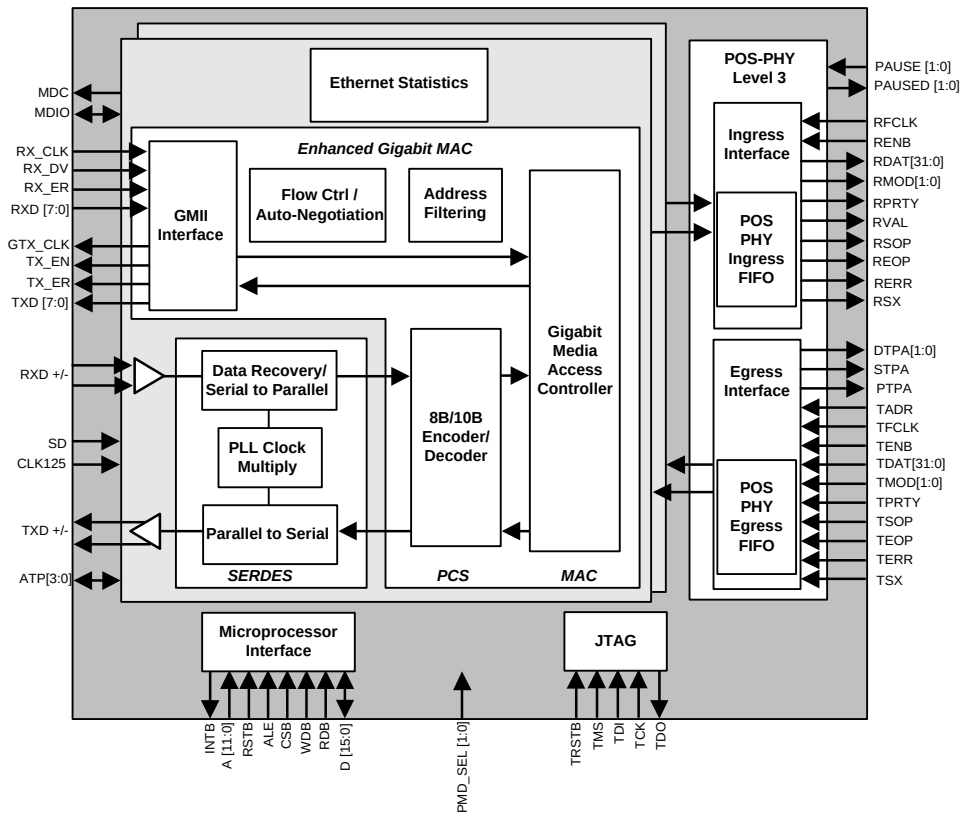
STATISTICS

- 40 bit counters are used to ensure rollover compliance with IEEE 802.3-1998.
- Minimum 58 minutes before rollover.
- Provides statistic counters to support SNMP and RMON implementations.

POS-PHY LEVEL 3 SYSTEM INTERFACE

- Standard OC-48 bandwidth Packet/Cell interface.
- Compatible with PMC-Sierra devices supporting POS-PHY Level 3, including:
  - PM5381 S/UNI®-2488 ATM and POS physical layer device.
  - PM5358 S/UNI®-4x622 single channel OC-48c device with integrated analog.
  - PM7390 S/UNI-MACH-48 multi-service access device for channelized interfaces.
  - PM5382 S/UNI-16x155 sixteen channel OC-3c framer with integrated analog and POS-PHY Level 3 and UTOPIA Level 3 interface.
- POS-PHY Level 3 provides connection to upper layer device at data rates up to 2,400 Mbit/s.

BLOCK DIAGRAM



Dual Gigabit Ethernet Controller

- Supports point-to-point POS-PHY Level 3 applications.
- 32 bit data at 104 MHz.
- In-band addressing for dual port PHY support.

PACKAGING

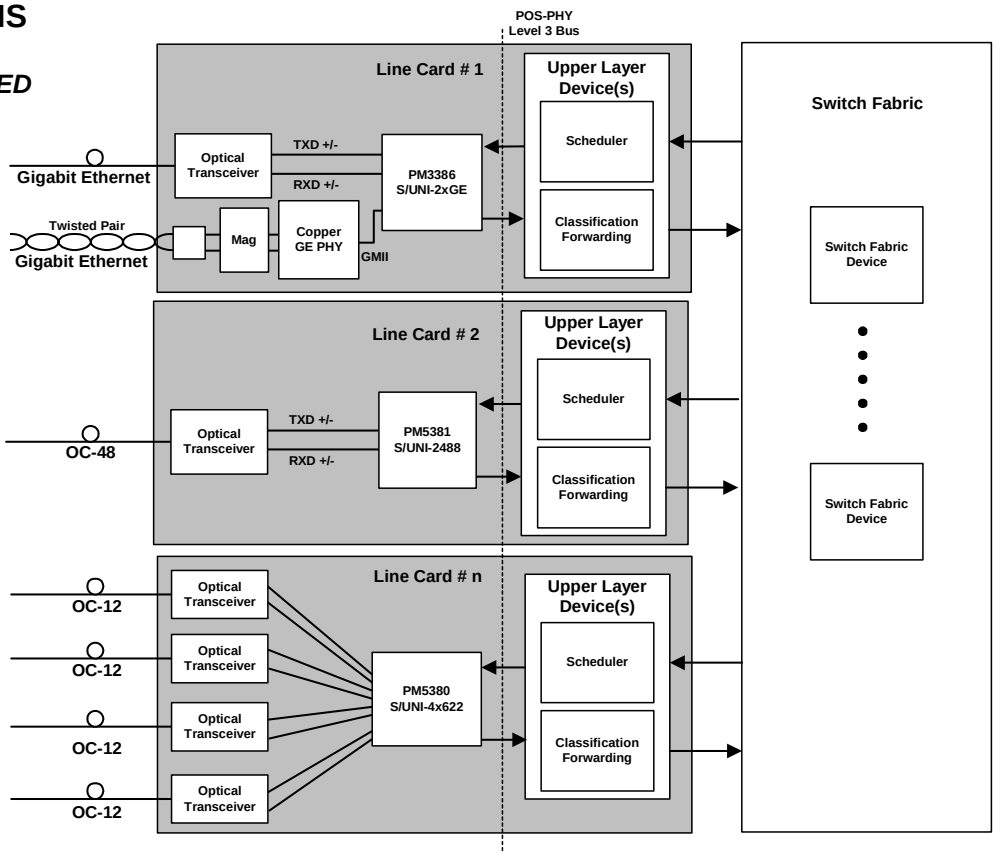
- Packaged in a 352-pin UBGA.
- Implemented in low power 1.8 V CMOS technology with 3.3 V compatible I/O.
- Industrial temperature range (-40 °C to +85 °C).
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

APPLICATIONS

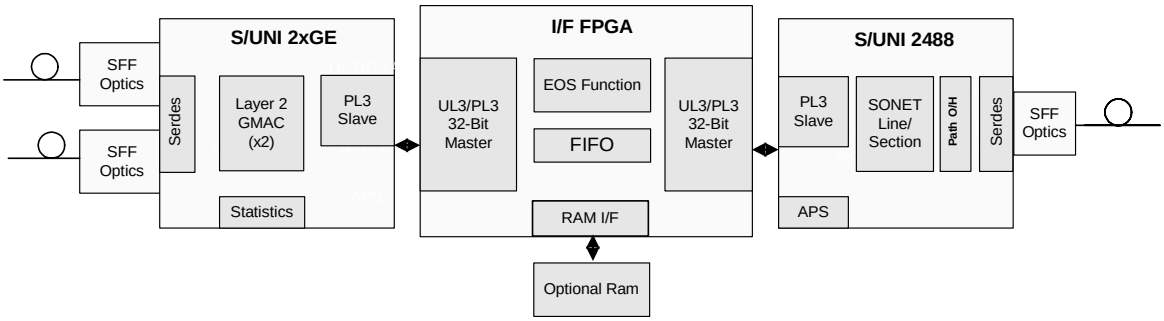
- POS-PHY Level 3 provides consistent system interface for multiple PHY types.
- Edge and Core Routers.
- Multi-Service Switches.
- SONET/SDH Transport Equipment.
- Ethernet over SONET uplinks.
- Gigabit Ethernet ports for Optical Cross Connects.
- Gigabit Ethernet Access IADs.
- Gigabit Ethernet Test Equipment.

TYPICAL APPLICATIONS

SAMPLE LINE CARDS LINKED WITH POS-PHY LEVEL 3 INTERFACE



ETHERNET OVER SONET



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PMC-1991223 (R4)