# Quad Cell Delineation Block Device

## FEATURES

- Quad cell delineation block operating up to a maximum rate of 52 Mbit/s.
- Provides a UTOPIA Level 2-compatible ATM-PHY Interface.
- Implements the Physical Layer Convergence Protocol (PLCP) for DS1 transmission systems according to the ATM Forum User Network Interface specification and ANSI TA-TSY-000773, TA-TSY-000772, and E1 transmission systems according to the ETSI 300-269 and ETSI 300-270.
- Supports SMDS PLCP and ATM Direct Mapping into various rate transmission systems in the following formats:
  - E1 (2.048 Mbit/s) in CRC-4 and PCM30;
  - T1 (1.544 Mbit/s) in ESF and SF;
  - Arbitrary Cell Rate (up to 52 Mbit/s) with ATM Direct Mapping only.
- Uses the PMC-Sierra PM4341 T1XC, PM4344 TQUAD, PM6341 E1XC, and PM6344 EQUAD T1 and E1 framer/line interface chips for DS-1 and E1 applications.
- Provides programmable pseudo-random test pattern generation, detection and analysis features.
- Provides performance monitoring counters suitable for accumulation periods of up to 1 second.

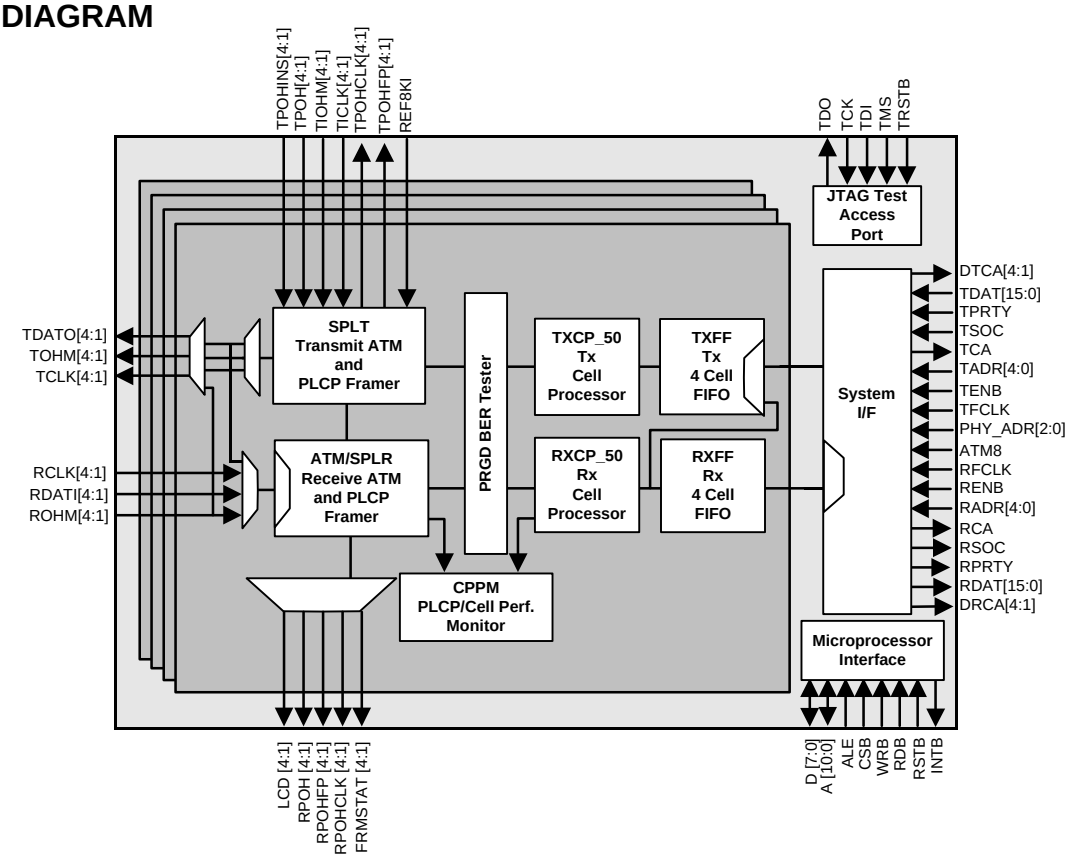
### *RECEIVER SECTION*

- Provides PLCP frame synchronization, path overhead extraction and cell extraction for DS1 and E1 PLCP formatted streams.
- Provides a 50 MHz 8-bit wide or 16-bit wide UTOPIA FIFO buffer in the receive path with parity support, and multi-PHY (Level 2) control signals.
- Provides ATM framing using cell delineation. ATM cell delineation may optionally be disabled to allow all cell bytes to pass regardless of cell delineation status.
- Provides cell descrambling, header check sequence (HCS) error detection, idle cell filtering, header descrambling (for use with PPP packets), and accumulates the number of received idle cells, the number of received cells written to the FIFO and the number of HCS errors.
- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cell FIFOs.
- Provides programmable pseudo-random test-sequence detection and analysis features.

### *TRANSMITTER SECTION*

- Provides a 50 MHz 8-bit wide or 16-bit wide Utopia FIFO buffer in the transmit path with parity support and multi-PHY (Level 2) control signals.
- Provides optional ATM cell scrambling, header scrambling (for use with PPP packets), HCS generation/insertion, programmable idle cell insertion, diagnostics features and accumulates transmitted cells read from the FIFO.

## BLOCK DIAGRAM



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- Provides a four cell FIFO for rate decoupling between the line and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cell FIFOs.
- Provides an 8 kHz reference input for locking the transmit PLCP frame rate to an externally applied frame reference.
- Provides programmable pseudo-random test sequence generation (up to $2^{32}$-1 bit length sequences conforming to ITU-T O.151 standards). Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from $10^{-1}$ to $10^{-7}$.

### *LOOPBACK FEATURES*

- Provides for diagnostic loopbacks and line loopbacks.

### *GENERAL*

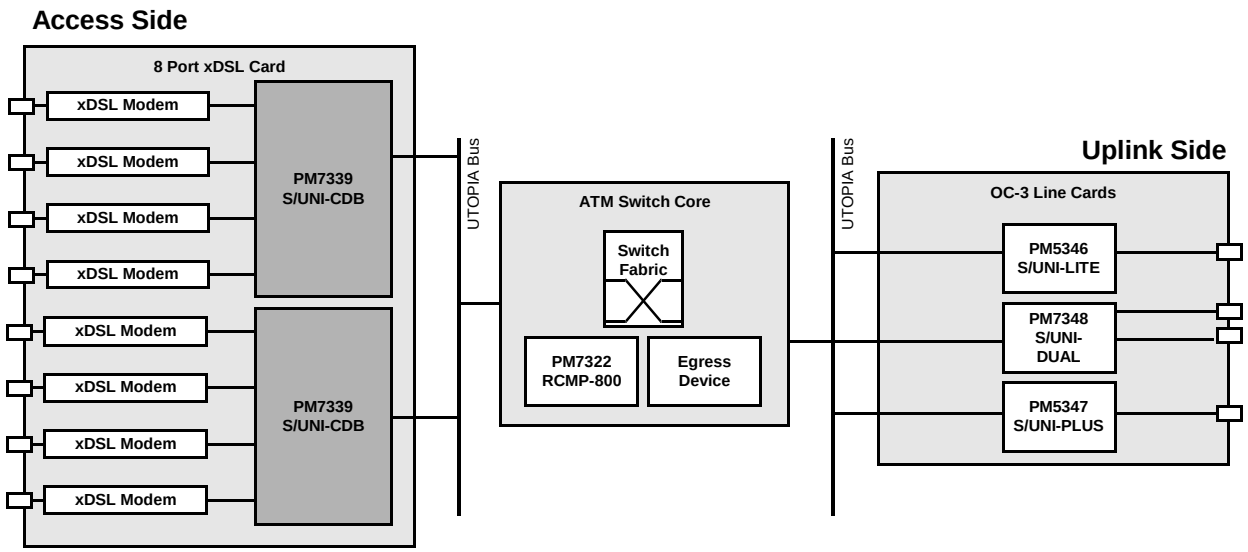
- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.
- Provides a standard five signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 3.3 V CMOS technology with 5 V tolerant inputs.
- Available in a high density 256-pin SBGA package (27 mm x 27 mm).

## APPLICATIONS

- ATM Switches, Multiplexers, and Routers.
- SMDS Switches, Multiplexers and Routers.
- DSLAM.
- Integrated Access Devices (IAD).

## TYPICAL APPLICATION

### *ATM BASED DSLAM EQUIPMENT*

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