Packet/ATM Traffic Manager and Switch

FEATURES

- ATM (fixed length cell) and packet/ frame traffic manager and switch.
- 128 line ports, 4 WAN ports, and a high speed microprocessor port. Any port to any port switching for 1024 independent connections.
- Manages up to 256 Kbyte cell (16 Mbyte) data buffer and 4 Mbyte context memory shared over all ports.
- Configurable progressive throttling of buffer consumption, with memory reservation under high consumption. Performs EFCI marking for ABR support.
- Buffer congestion controlled via Partial Packet Discard, Early Packet Discard (PPD/EPD). Cell at a time discard also supported.
- For frame/packet flows:
  - Supports external wire speed HDLC processor, SAR, and flow classifier via packet-contiguous queuing and scheduling.
  - Error indication in AAL5 EOM trailer (set by SAR or classifier) can invoke errored packet discard, thereby eliminating need for packet buffers in external devices.
- Traffic queuing algorithm is highly configurable on a per connection, per class, and per port basis.
- Configurable scheduling of 4 classes of service on every port, with rate shaping available for the 4 WAN ports. Configurable traffic parameters enabling a mix of CBR, VBR, GFR, and UBR classes.
- Configurable OAM cell queuing and special handling on all ports.
- VPI/VCI header mapping.
- Supports 700 Mb/s ingress traffic and 700 Mb/s egress traffic aggregated across all ports.
- Low power 3.3/ 2.5 V CMOS.
- Standard 5-pin P1149 JTAG port.
- 352-ball SBGA, 35 mm x 35 mm.

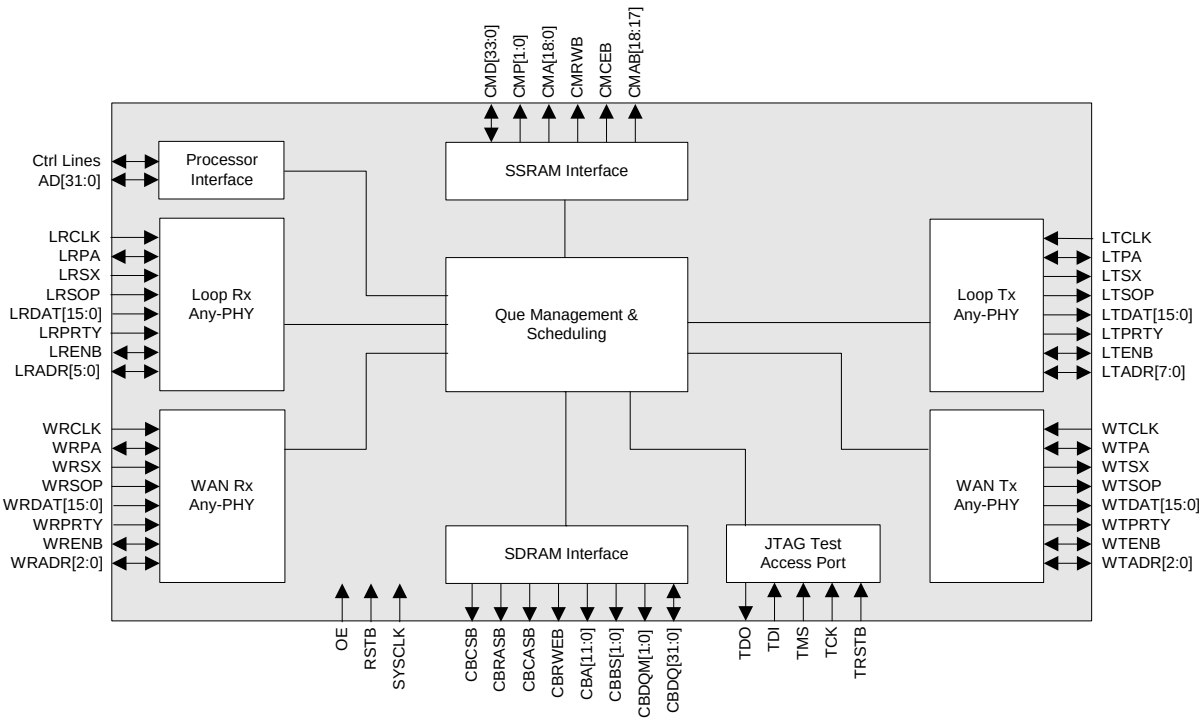
BUS INTERFACES

- 8/16 bit, 52 MHz UTOPIA L2 bus.
- Line side:
  - Enhanced UTOPIA Tx master supports 128 ports. Rx master supports 32 ports.
  - Or single port slave.
- WAN side:
  - Master (with optional cell length expansion) supports 4 Tx or Rx ports.
  - Or single port slave.

MICROPROCESSOR INTERFACE

- 66 MHz, 32 bit address/data bus capable of single or burst access to internal registers and cell buffers.
- Supports cell/packet transfer to/from any port, with CRC32 and CRC10 calculation supported in hardware.

BLOCK DIAGRAM



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CONGESTION CONTROL

- Traffic discard thresholds configurable per connection (independent CLP0 and CLP1 thresholds), per class, per port, and per direction.
- Guaranteed Frame Rate (GFR) implemented via CLP0 minimum buffer size reservation per connection.

QUEUING & SCHEDULING

- 1024 traffic staging queues (one per connection) individually assignable to any CoS on any port.
- 512 + 20 scheduling queues: 4 CoS queues per port, 128 line ports, 4 WAN ports, and 1 processor port.
- Each port's queuing and scheduling is configurable as cell at a time or packet at a time.
- Connections are scheduled into each class queue using configurable weighted fair queuing (cell mode), or FIFO (frame mode).
- Classes are scheduled into ports using strict priority with configurable minimum bandwidth reservation.
- Ports are scheduled onto their corresponding bus using a configurable weighted interleaved round robin algorithm.
- On the WAN ports: rate shaping, individually configured per connection, within four classes.

ACCOUNTING

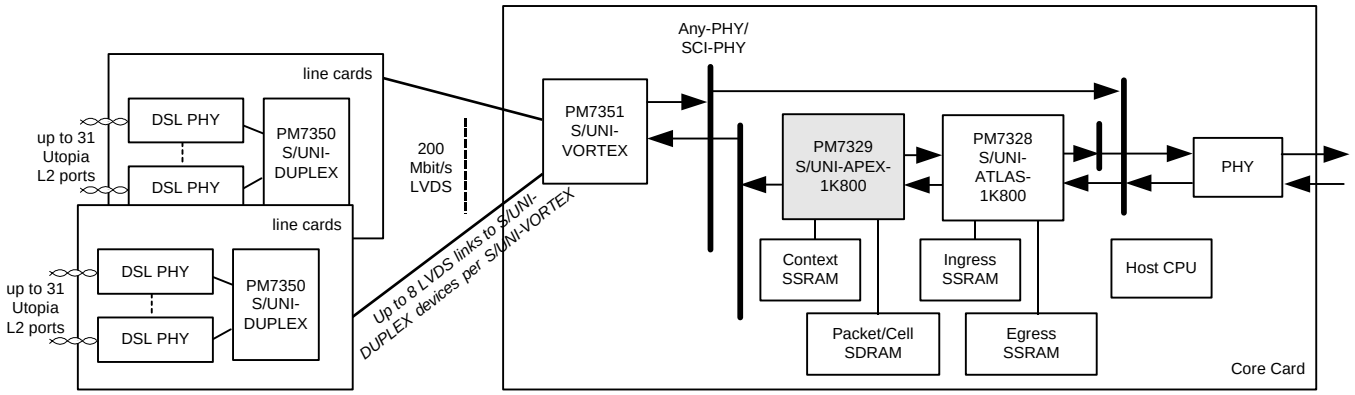
- Per connection CLP0/CLP1 upstream/ downstream Tx counts.
- Error statistics accumulation.
- CLP0/CLP1 cell discard counts with indication of connection ID of last cell discarded.

APPLICATIONS

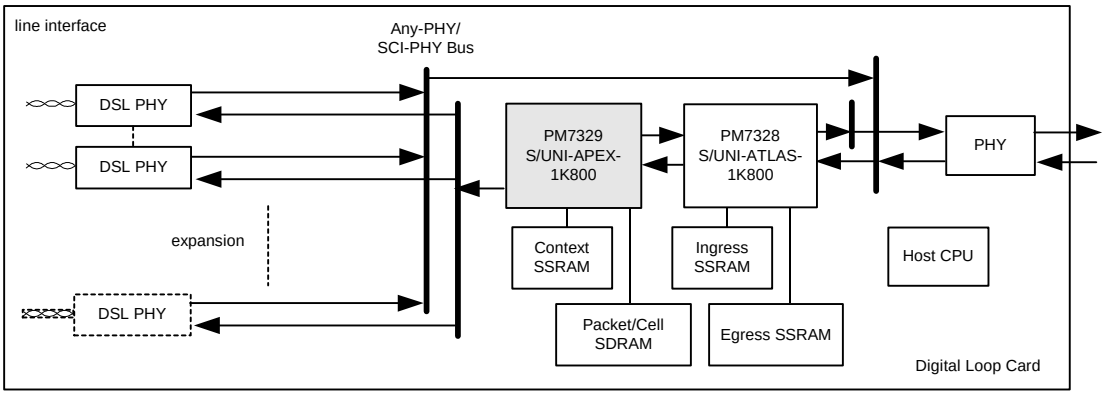
- Mini Digital Subscriber Loop Access Multiplexer (mini-DSLAM).
- Subscriber Access equipment.
- Digital Loop Card traffic aggregation.

TYPICAL APPLICATION

S/UNI-APEX-1K800 IN OC3 MINI-DSLAM APPLICATION



S/UNI-APEX-1K800 IN OC3 DIGITAL LOOP CARD APPLICATION



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