

QL7100 EclipsePlus Data Sheet



••••• Combining Performance, Density, and Embedded RAM

Device Highlights

Flexible Programmable Logic

- .25 μm five layer metal CMOS Process
- 2.5 V V_{CC} , 2.5/3.3 V Drive Capable I/O
- 960 Logic Cells
- 248,160 Max System Gates
- Up to 250 I/O Pins

Embedded Dual Port SRAM

- Twenty 2,304-bit Dual Port High Performance SRAM Blocks
- 46,100 RAM bits
- RAM/ROM/FIFO Wizard for Automatic Configuration
- Configurable and Cascadable

Programmable I/O

- High performance Enhanced I/O (EIO)—less than 3 ns T_{CO}
- Programmable Slew Rate Control
- Programmable I/O Standards:
 - LVTTTL, LVCMOS, PCI, GTL+, SSTL2, and SSTL3
 - Eight Independent I/O Banks
 - Three Register Configurations: Input, Output, and Output Enable

Advanced Clock Network

- Nine Global Clock Networks:
 - One Dedicated
 - Eight Programmable
- 20 Quad-Net Networks—five per Quadrant
- 16 I/O Controls—two per I/O Bank
- Four phase locked loops

Embedded Computational Units

ECUs provide integrated Multiply, Add, and Accumulate Functions.

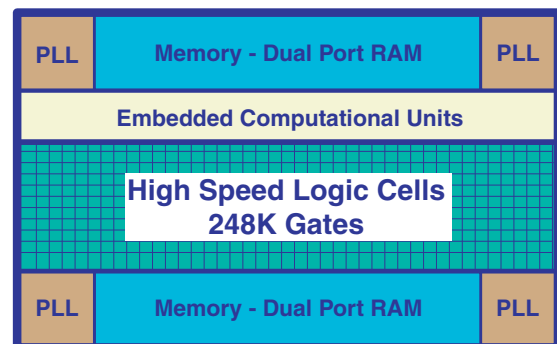


Figure 1: EclipsePlus Block Diagram

Electrical Specifications

AC Characteristics*

*(at $V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{ C}$, Typical Corner, Speed Grade = -7 ($K = 0.74$))

The AC Specifications are provided from **Table 1** to **Table 10**. Logic Cell diagrams and waveforms are provided from **Figure 2** to **Figure 15**.

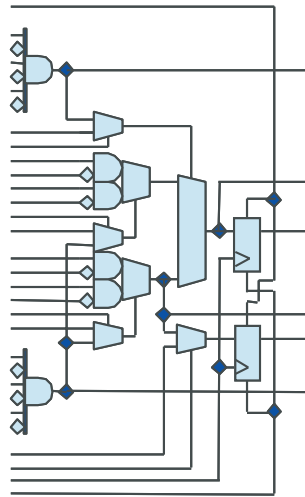


Figure 2: EclipsePlus Logic Cell

Table 1: Logic Cells

Symbol Logic Cells	Parameter	Value	
		Min	Max
t_{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output	-	0.257 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.22 ns	-
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	-
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge.	-	0.255 ns
t_{CWHI}	Clock High Time: required minimum time the clock stays high	0.46 ns	-
t_{CWL0}	Clock Low Time: required minimum time that the clock stays low	0.46 ns	-
t_{SET}	Set Delay: time between when the flip-flop is "set" (high) and when the output is consequently "set" (high)	-	0.18 ns

Table 1: Logic Cells (Continued)

Symbol Logic Cells	Parameter	Value	
		Min	Max
t_{RESET}	Reset Delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	-	0.09 ns
t_{SW}	Set Width: time that the SET signal remains high/low	0.3 ns	-
t_{RW}	Reset Width: time that the RESET signal remains high/low	0.3 ns	-

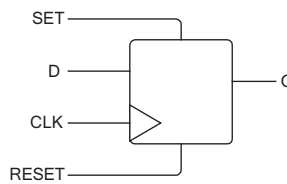


Figure 3: Logic Cell Flip-Flop

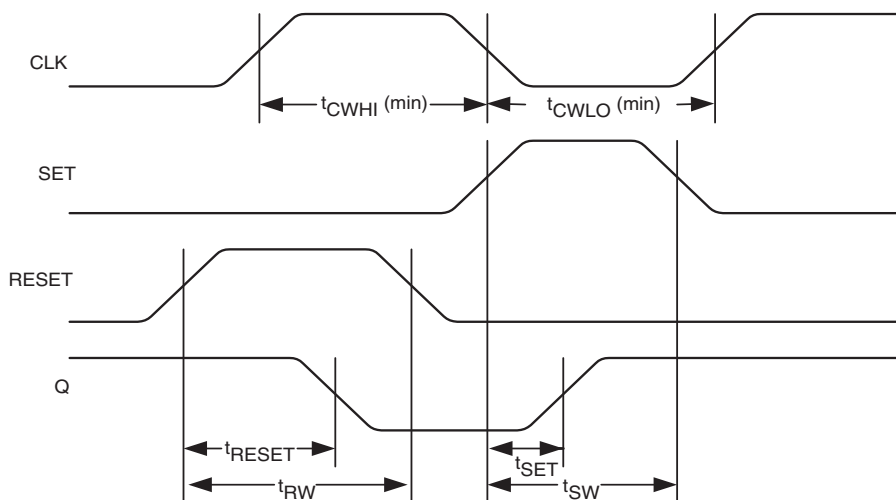


Figure 4: Logic Cell Flip-Flop Timings—First Waveform

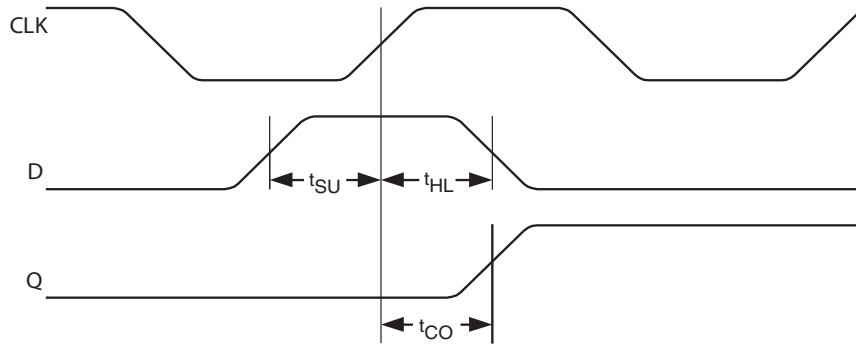


Figure 5: Logic Cell Flip-Flop Timings—Second Waveform

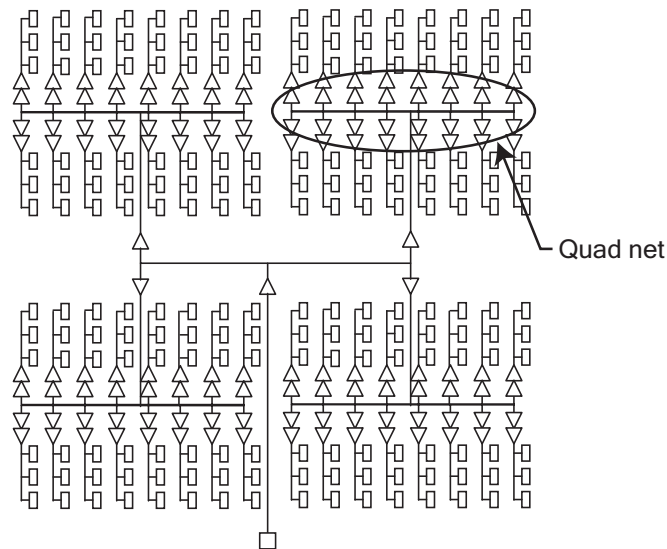


Figure 6: EclipsePlus Global Clock Structure

Table 2: EclipsePlus Clock Delay

Clock Source	Parameters	Clock Performance	
		Global	Dedicated
Logic Cells (Internal)	Clock signal generated internally	1.51 ns (max)	
Clock Pad	Clock signal generated externally	2.06 ns (max)	1.73 ns (max)

Table 3: EclipsePlus Global Clock Delay

Clock Segment	Parameter	Value	
		Min	Max
t_{PGCK}^a	Global clock pin delay to quad net	-	1.34 ns
t_{BGCK}	Global clock tree delay (quad net to flip-flop)	-	0.56 ns

- a. When using a PLL, t_{PGCK} and t_{BGCK} are effectively zero due to delay adjustment by Phase Locked Loop.

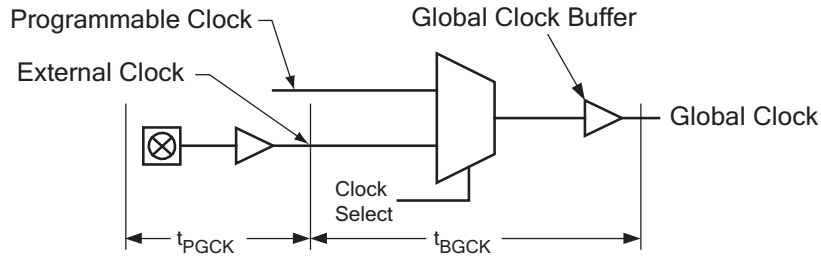


Figure 7: Global Clock Structure Schematic

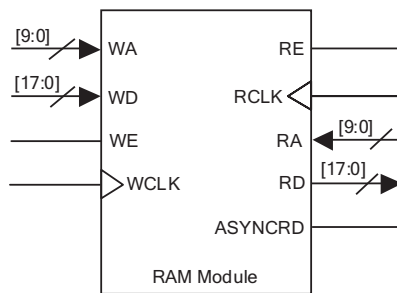


Figure 8: RAM Module

Table 4: RAM Cell Synchronous Write Timing

Symbol	Parameter	Value	
		Min	Max
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.675 ns	-
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.654 ns	-
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.623 ns	-
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	-	4.38 ns

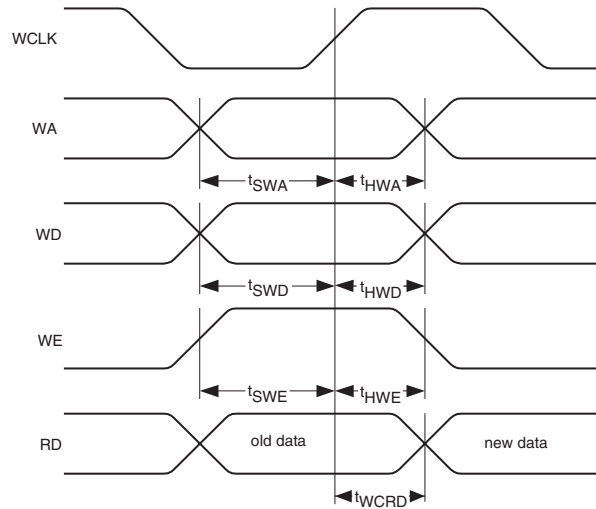


Figure 9: RAM Cell Synchronous Write Timing

Table 5: RAM Cell Synchronous & Asynchronous Read Timing

Symbol	RAM Cell Synchronous Read Timing		Value	
	Parameter	Min	Max	
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.686 ns	-	
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	-	
t_{SRE}	RE setup time to WCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.243 ns	-	
t_{HRE}	RE hold time to WCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	0 ns	-	
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	-	4.38 ns	
RAM Cell Asynchronous Read Timing				
t_{PDRD}	RA to RD: time between when the READ ADDRESS is input and when the DATA is output	-	2.06 ns	

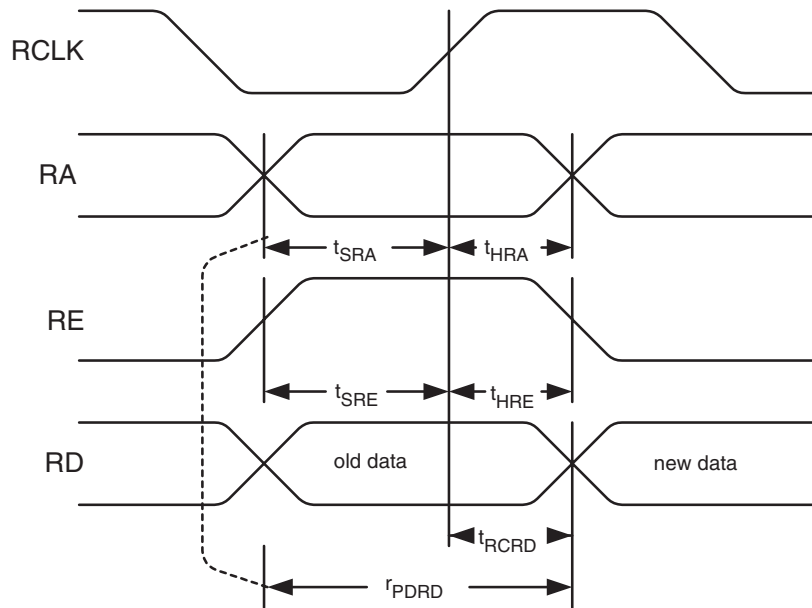


Figure 10: RAM Cell Synchronous & Asynchronous Read Timing

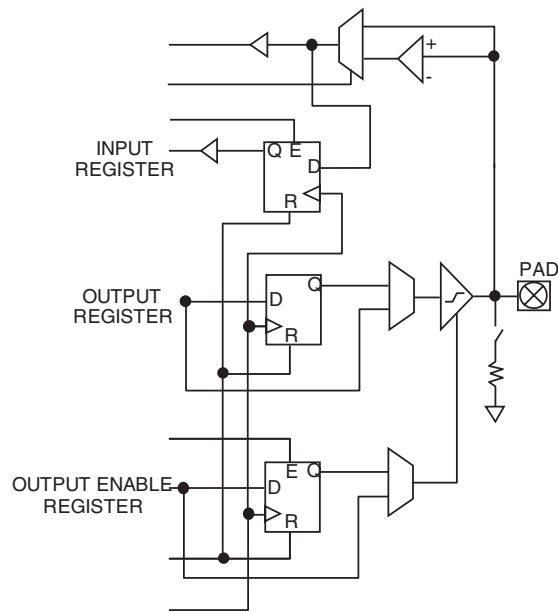


Figure 11: EclipsePlus Cell I/O

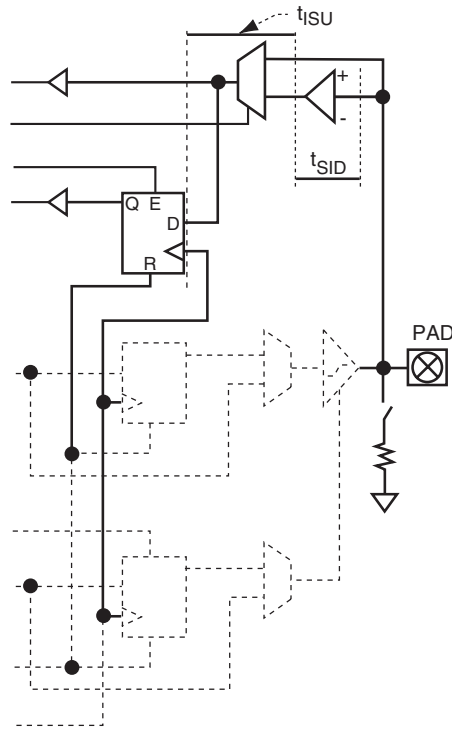


Figure 12: EclipsePlus Input Register Cell

Table 6: Input Register Cell

Symbol	Parameter: Input Register Cell Only	Value	
		Min	Max
t_{SU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	3.12 ns	-
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	-
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output after the active clock edge	-	1.08 ns
t_{IRST}	Input register reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	-	0.99 ns
t_{IESU}	Input register clock enable setup time: time “enable” must be stable before the active clock edge	0.37 ns	-
t_{IEH}	Input register clock enable hold time: time “enable” must be stable after the active clock edge	0 ns	-

Table 7: Standard Input Delays

Symbol	Parameter	Value	
		Min	Max
t_{SID} (LVTTTL)	LVTTTL input delay: Low Voltage TTL for 3.3 V applications	-	0.34 ns
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	-	0.42 ns
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	-	0.68 ns
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	-	0.55 ns
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	-	0.61 ns

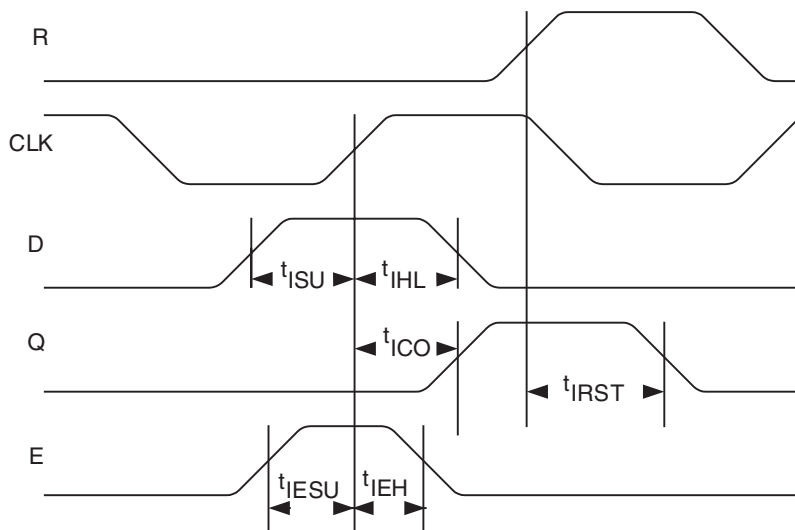


Figure 13: EclipsePlus Input Register Cell Timing

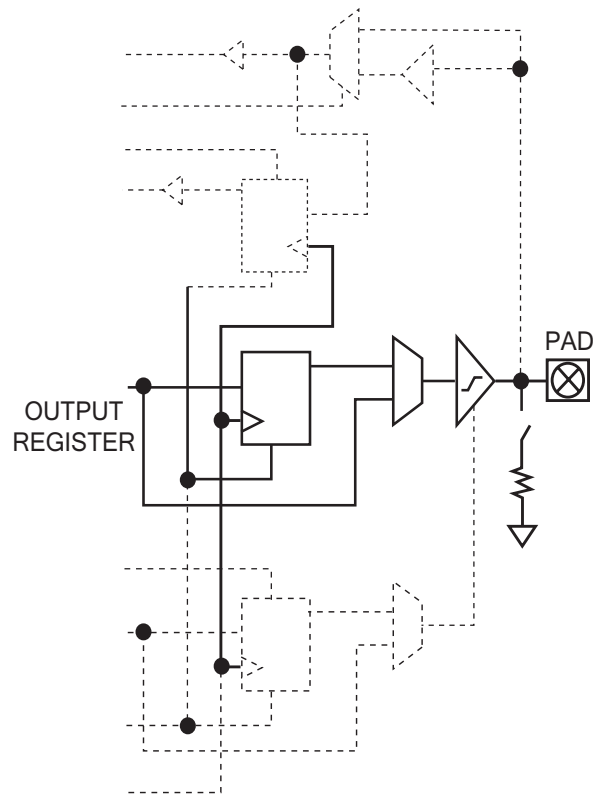


Figure 14: EclipsePlus Output Register Cell

Table 8: EclipsePlus Output Register Cell

Symbol	Parameter	Value	
		Min	Max
Output Register Cell Only			
t_{OUTLH}	Output Delay low to high (90% of H)	-	0.40 ns
t_{OUTHL}	Output Delay high to low (10% of L)	-	0.55 ns
t_{PZH}	Output Delay tri-state to high (90% of H)	-	2.94 ns
t_{PZL}	Output Delay tri-state to low (10% of L)	-	2.34 ns
t_{PHZ}	Output Delay high to tri-State	-	3.07 ns
t_{PLZ}	Output Delay low to tri-State	-	2.53 ns
t_{COP}	Clock-to-out delay (does not include clock tree delays)	-	3.15 ns (fast slew) 10.2 ns (slow slew)

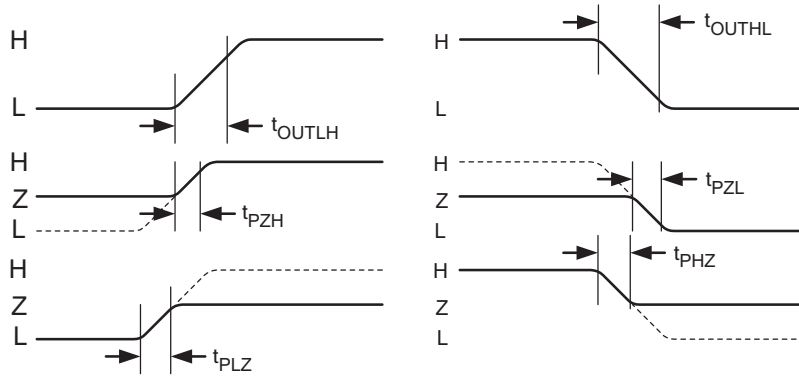


Figure 15: EclipsePlus Output Register Cell Timing

Table 9: Output Slew Rates @ $V_{CCIO} = 3.3\text{ V}$

	Fast Slew	Slow Slew
Rising Edge	2.8 V/ns	1.0 V/ns
Falling Edge	2.86 V/ns	1.0 V/ns

Table 10: Output Slew Rates @ $V_{CCIO} = 2.5\text{ V}$

	Fast Slew	Slow Slew
Rising Edge	1.7 V/ns	0.6 V/ns
Falling Edge	1.9 V/ns	0.6 V/ns

DC Characteristics

The DC Specifications are provided in **Table 11** through **Table 13**.

Table 11: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V _{CC} Voltage	-0.5 V to 3.6 V	DC Input Current	±20 mA
V _{CCIO} Voltage	-0.5 V to 4.6 V	ESD Pad Protection	±2000 V
INREF Voltage	2.7 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to V _{CCIO} +0.5 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C
Latch-up Immunity	±100 mA		

Table 12: Operating Range

Symbol	Parameter	Military		Industrial		Commercial		Unit	
		Min	Max	Min	Max	Min	Max		
V _{CC}	Supply Voltage	2.3	2.7	2.3	2.7	2.3	2.7	V	
V _{CCIO}	I/O Input Tolerance Voltage	2.3	3.6	2.3	3.6	2.3	3.6	V	
TA	Ambient Temperature	-55		-40	85	0	70	°C	
TC	Case Temperature	-	125	-	-	-	-	°C	
K	Delay Factor	-4 Speed Grade	0.42	2.3	0.43	2.16	0.47	2.11	n/a
		-5 Speed Grade	0.42	1.92	0.43	1.80	0.46	1.76	n/a
		-6 Speed Grade	0.42	1.35	0.43	1.26	0.46	1.23	n/a
		-7 Speed Grade	0.42	1.28	0.43	1.19	0.46	1.16	n/a

Table 13: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
I _I	I or I/O Input Leakage Current	V _I = V _{CCIO} or GND	-10	10	μA
I _{OZ}	3-State Output Leakage Current	V _I = V _{CCIO} or GND	-10	10	μA
C _I	Input Capacitance ^a	-	-	8	pF
I _{OS}	Output Short Circuit Current ^b	V _o = GND V _o = V _{CC}	-15 40	-180 210	mA mA
I _{CC}	D.C. Supply Current ^c	V _I , V _o = V _{CCIO} or GND	0.50 (typ)	2	mA
I _{CCIO}	D.C. Supply Current on V _{CCIO}	-	0	2	mA
I _{CCIO(DIF)}	D.C. Supply Current on V _{CCIO} for Differential I/O	-	-	-	mA
I _{REF}	D.C. Supply Current on INREF	-	-10	10	μA
I _{PD}	Pad Pull-down (programmable)	V _{CCIO} = 3.6 V	-	150	μA

a. Capacitance is sample tested only. Clock pins are 12 pF maximum.

b. Only one output at a time. Duration should not exceed 30 seconds.

c. For -4/-5/-6/-7 commercial grade devices only. Maximum I_{CC} is 3 mA for -0 commercial grade and all industrial grade devices, and 5 mA for all military grade devices.

Embedded Computational Unit (ECU)

Traditional Programmable Logic architectures do not implement arithmetic functions efficiently or effectively—these functions require high logic cell usage while garnering only moderate performance results.

The QL7100 architecture allows for functionality above and beyond that achievable using programmable logic devices. By embedding a dynamically reconfigurable computational unit, the QL7100 device can address various arithmetic functions efficiently. This approach offers greater performance than traditional programmable logic implementations. The embedded block is implemented at the transistor level as shown in **Figure 16**.

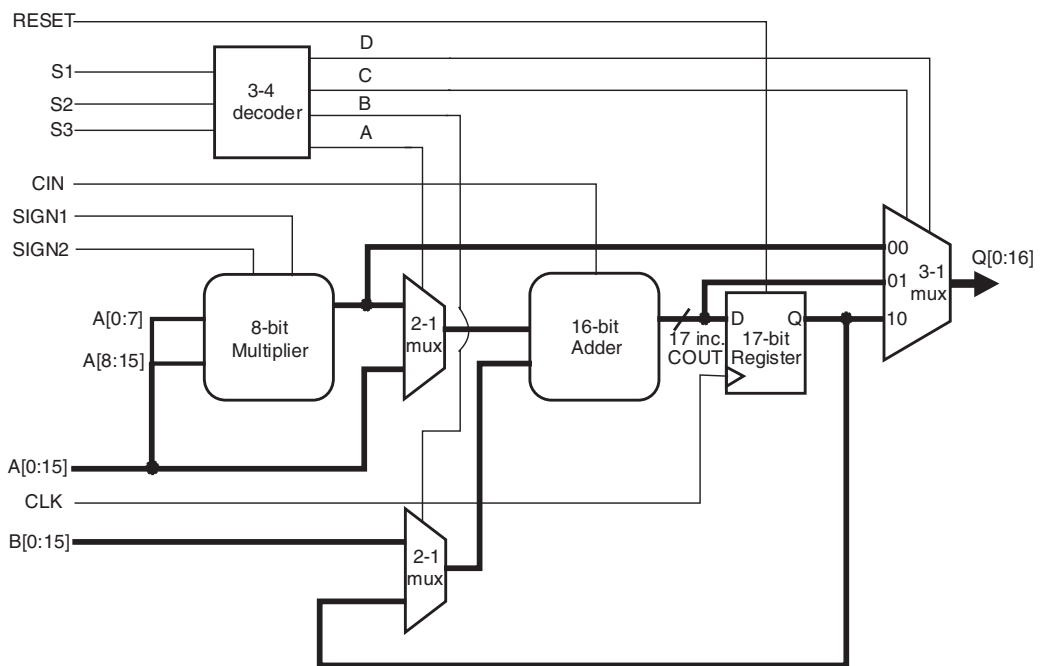


Figure 16: ECU Block Diagram

The 10 QL7100 ECU blocks are placed next to the SRAM circuitry for efficient memory/instruction fetch and addressing for DSP algorithmic implementations.

Ten 8-bit Multiply-Accumulate (MAC) functions can be implemented per cycle for a total of 1 billion MACs/s when clocked at 100 MHz. Additional MAC functions can be implemented in the programmable logic.

The modes for the ECU block are dynamically re-programmable through the programmable logic as shown in **Table 14**.

Table 14: ECU Mode Select Criteria

Instruction			Operation	ECU Performance ^a , -7 WCC ^b		
S1	S2	S3		t _{PD}	t _{SU}	t _{CO}
0	0	0	Multiply	6.57 ns max		
0	0	1	Multiply-Add	8.84 ns max		
0	1	0	Accumulate ^c		3.91 ns min	1.16 ns max
0	1	1	Add	3.14 ns max		
1	0	0	Multiply (registered) ^d		9.61 ns min	1.16 ns max
1	0	1	Multiply- Add (registered)		9.61 ns min	1.16 ns max
1	1	0	Multiply - Accumulate		9.61 ns min	1.16 ns max
1	1	1	Add (registered)		3.91 ns min	1.16 ns max

- a. t_{PD}, t_{SU} and t_{CO} do not include routing paths in/out of the ECU block.
- b. Timing numbers represent -7 Worst Case Commercial conditions.
- c. Internal feedback path in ECU restricts max clk frequency to 238 MHz.
- d. B [15:0] set to zero.

Phase Locked Loops (PLLs)

Instead of requiring extra components, designers simply need to instantiate one of the pre-configured models described in this section and listed in [Table 15](#). The QuickLogic built-in PLLs support a wider range of frequencies than many other PLLs. Also, QuickLogic PLLs can be cascaded to support different ranges of frequency multiplications or divisions, driving the device at a faster or slower rate than the incoming clock frequency. Most importantly, they achieve a very short clock-to-out time—generally less than 3 ns. This low clock-to-out time is achieved by the PLL subtracting the clock tree delay through the feedback path, effectively making the clock tree delay zero.

Figure 17 illustrates a typical QuickLogic ESP PLL.

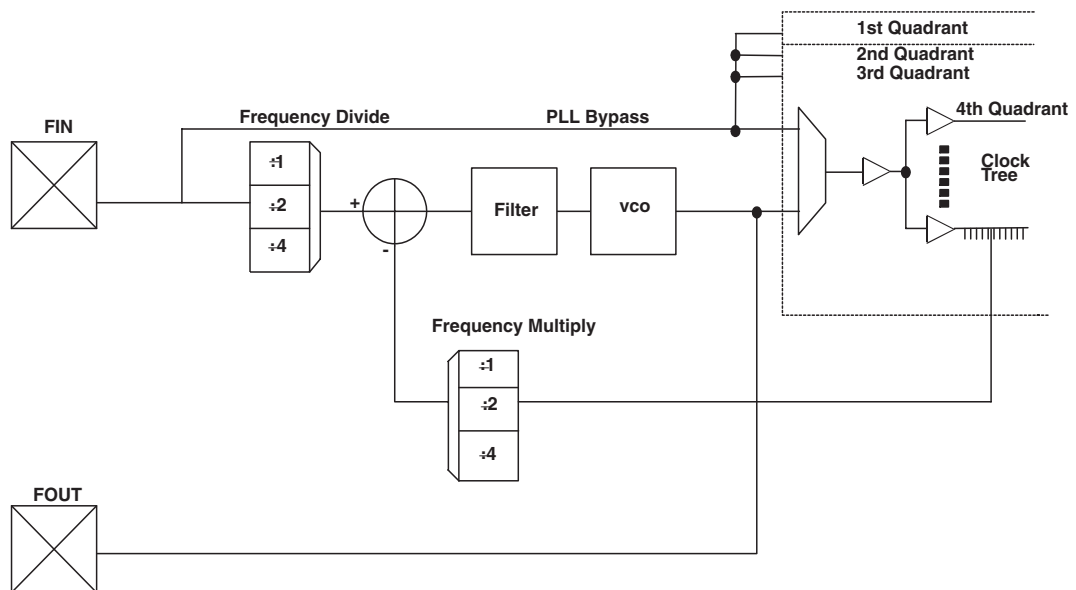


Figure 17: PLL Block

F_{in} represents a very stable high-frequency input clock and produces an accurate signal reference. This signal can either bypass the PLL entirely, thus entering the clock tree directly, or it can pass through the PLL itself.

Within the PLL, a voltage-controlled oscillator (VCO) is added to the circuit. The external F_{in} signal and the local VCO form a control loop. The VCO is multiplied or divided down to the reference frequency, so that a phase detector (the crossed circle in [Figure 17](#)) can compare the two signals. If the phases of the external and local signals are not within the tolerance required, the phase detector sends a signal through the charge pump and loop filter ([Figure 17](#)). The charge pump generates an error voltage to bring the VCO back into alignment and the loop filter removes any high frequency noise before the error voltage enters the VCO. This new VCO signal enters the clock tree to drive the chip's circuitry.

F_{out} represents the clock signal that emerges from the output pad (the output signal PLLPAD_OUT is explained in [Table 16](#)). This clock signal is meaningful only when the PLL is configured for external use; otherwise, it remains in high Z state, as shown in the post-simulation waveform.

Most QuickLogic products contain four PLLs, one to be used in each quadrant. The PLL presented in **Figure 17** controls the clock tree in the fourth Quadrant of its ESP. As previously mentioned, QuickLogic PLLs compensate for the additional delay created by the clock tree itself by subtracting the clock tree delay through the feedback path.

For more specific information on the Phase Locked Loops, please refer to Application Note 58 at <http://www.quicklogic.com/images/appnote58.pdf>

PLL Modes of Operation

QuickLogic PLLs have eight modes of operation, based on the input frequency and desired output frequency—**Table 15** indicates the features of each mode.

Table 15: PLL Mode Frequencies

PLL Model	Output Frequency	Input Frequency Range ^a	Output Frequency Range
PLL_HF ^b	Same as input frequency	66 MHz–150 MHz	66 MHz–150 MHz
PLL_LF	Same as input frequency	25 MHz–133 MHz	25 MHz–133 MHz
PLL_MULT2HF	2 × input frequency	50 MHz–125 MHz	100 MHz–250 MHz
PLL_MULT2LF	2 × input frequency	16 MHz–50 MHz	32 MHz–100 MHz
PLL_DIV2HF	1/2 × input frequency	100 MHz–250 MHz	50 MHz–125 MHz
PLL_DIV2LF	1/2 × input frequency	50 MHz–100 MHz	25 MHz–50 MHz
PLL_MULT4	4 × input frequency	16 MHz–40 MHz	64 MHz–160 MHz
PLL_DIV4	1/4 × input frequency	100 MHz–300 MHz	25 MHz–75 MHz

a. The input frequency can range from 12.5 MHz to 500 MHz, while output frequency ranges from 25 MHz to 250 MHz. When you add PLLs to your top-level design, be sure that the PLL mode matches your desired input and output frequencies.

b. HF stands for high frequency and LF stands for low frequency.

PLL Signals

Table 16 summarizes the key signals in QuickLogic's PLLs.

Table 16: PLL Signals

Signal Name	Description
PLLCLK_IN ^a	Input clock signal
PLL_RESET	Active High Reset If PLL_RESET is asserted, then CLKNET_OUT and PLLPAD_OUT are reset to 0. This signal must be asserted and then released in order for the LOCK_DETECT to work.
ONn_OFFCHIP	PLL output This signal selects whether the PLL will drive the internal clock network or be used off-chip. This is a static signal, not a dynamic signal. Tied to GND = outgoing signal drives internal gates. Tied to VCC = outgoing signal used off-chip.
CLKNET_OUT	Out to internal gates This signal bypasses the PLL logic before driving the internal gates. Note that this signal cannot be used in the same quadrant where the PLL signal is used (PLLCLK_OUT).
PLLCLK_OUT	Out from PLL to internal gates This signal can drive the internal gates after going through the PLL. For this to work, ONn_OFFCHIP must be tied to GND.
PLLPAD_OUT	Out to off-chip This outgoing signal is used off-chip. For this to work, ONn_OFFCHIP signal must be tied to VCC.
LOCK_DETECT	Active High Lock detection signal NOTE: For simulation purposes, this signal gets asserted after 10 clock cycles. However, it can take a maximum of 200 clock cycles to sync with the input clock upon release of the RESET signal.

a. Because PLLCLK_IN and PLL_RESET signals have INPAD, and PLLPAD_OUT has OUTPAD, you do not have to add additional pads to your design

I/O Characteristics

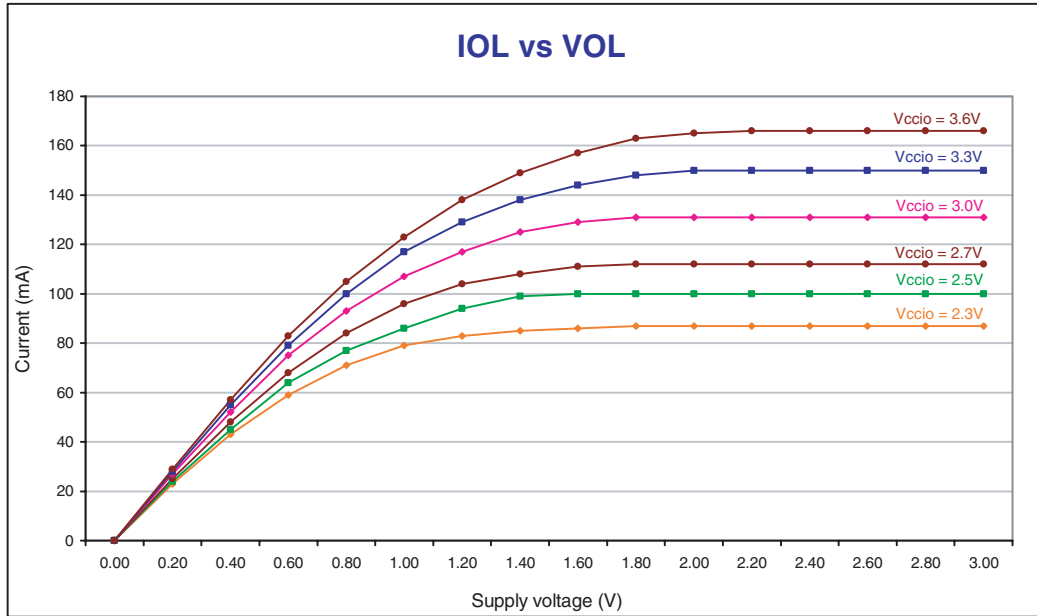


Figure 18: IOL vs. VOL

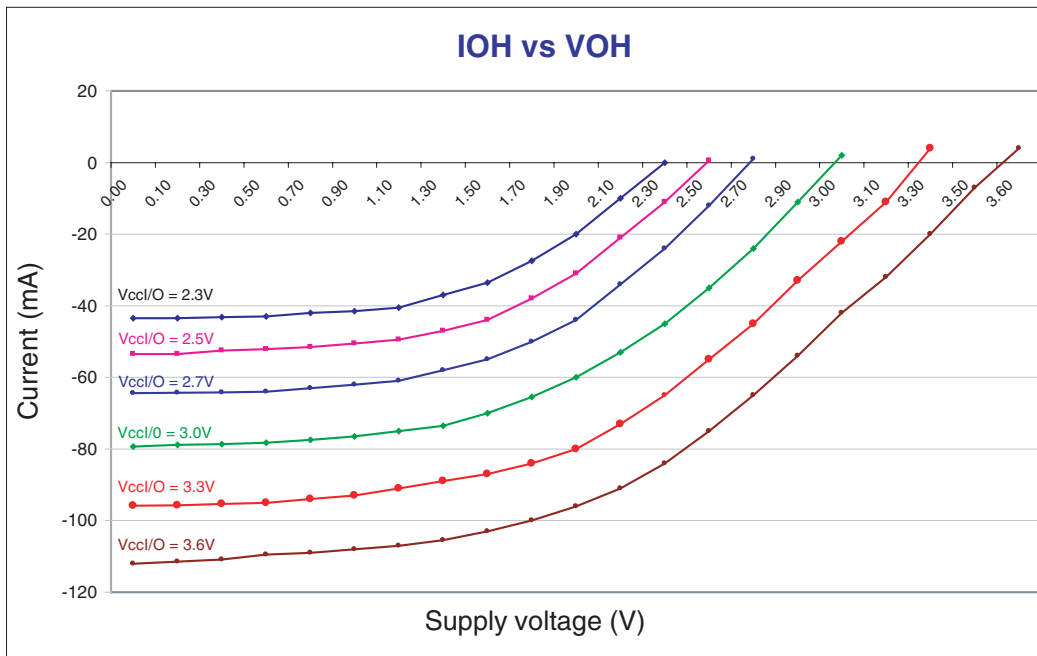


Figure 19: IOH vs. VOH

Table 17: DC Input and Output Levels^a

	INREF		V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V _{MIN}	V _{MAX}	V _{MIN}	V _{MAX}	V _{MIN}	V _{MAX}	V _{MAX}	V _{MIN}	mA	mA
LVTTTL	n/a	n/a	-0.3	0.8	2.0	V _{CCIO} + 0.3	0.4	2.4	2.0	-2.0
LVC MOS2	n/a	n/a	-0.3	0.7	1.7	V _{CCIO} + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	V _{CCIO} + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x V _{CCIO}	0.5 x V _{CCIO}	V _{CCIO} + 0.5	0.1 x V _{CCIO}	0.9 x V _{CCIO}	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	V _{CCIO} + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	V _{CCIO} + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 17** are JEDEC and PCI Specifications—QuickLogic devices either meet or exceed these requirements. For data specific to QuickLogic I/Os, see **Table 1** through **Table 13** and **Figure 1** through **Figure 19**.

NOTE: All CLK and IOCTRL pins are clamped to the V_{CC} rail, not the V_{CCIO}. Therefore, these pins can only be driven up to V_{CC} + 0.3 V.

Package Thermal Characteristics

Thermal Resistance Equations:

$$\theta_{JC} = (T_J - T_C) / P$$

$$\theta_{JA} = (T_J - T_A) / P$$

$$P_{MAX} = (T_{JMAX} - T_{AMAX}) / \theta_{JA}$$

Parameter Description:

θ_{JC} : Junction-to-case thermal resistance

θ_{JA} : Junction-to-ambient thermal resistance

T_J : Junction temperature

T_A : Ambient temperature

P: Power dissipated by the device while operating

P_{MAX} : The maximum power dissipation for the device

T_{JMAX} : Maximum junction temperature

T_{AMAX} : Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 150° C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 18**, pick an appropriate T_{AMAX} and use:

$$P_{MAX} = (150^\circ \text{ C} - T_{AMAX}) / \theta_{JA}$$

Table 18: Package Thermal Characteristics

Package Description		θ_{JA} (° C/W) @ various flow rates (m/sec)				θ_{JC} (° C/W)
Pin Count	Package Type	0	0.5	1	2	
516	PBGA	20.0	19.0	17.5	16.0	7.0
484	PBGA	28.0	26.0	25.0	23.0	9.0
280	LF-PBGA	18.5	17.0	15.5	14.0	7.0
208	PQFP	26.0	24.5	23.0	22.0	11.0

Kv and Kt Graphs

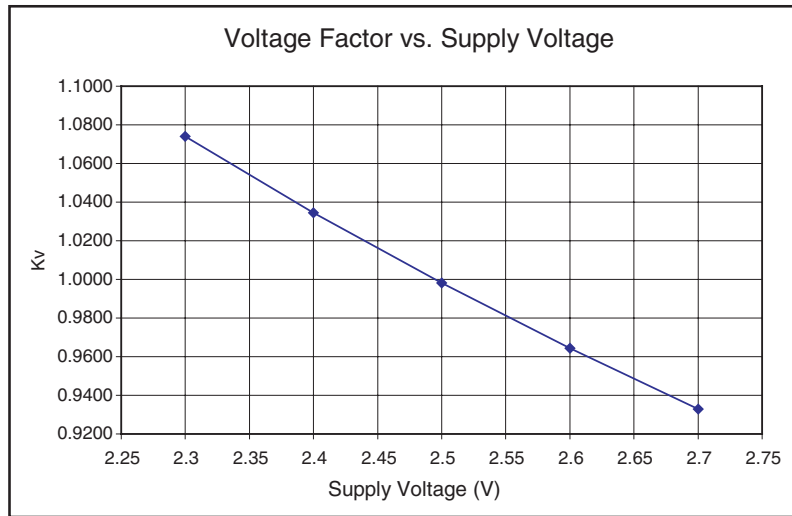


Figure 20: Voltage Factor vs. Supply Voltage

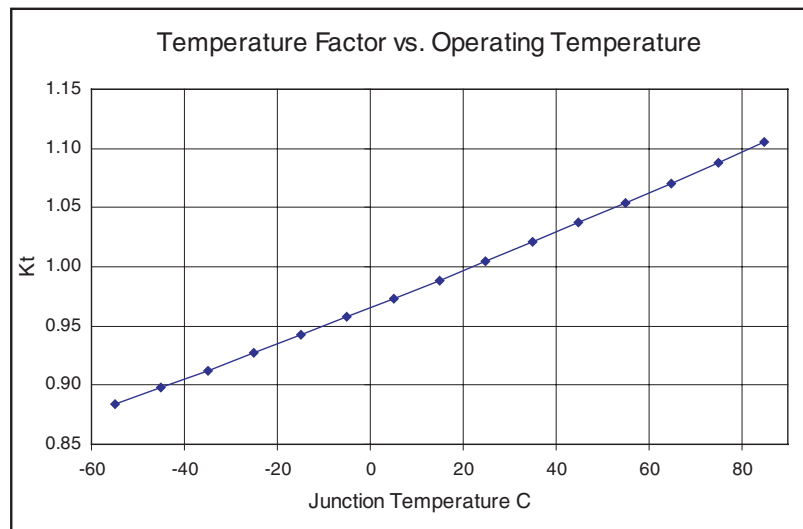


Figure 21: Temperature Factor vs. Operating Temperature

Power vs. Operating Frequency

The basic power equation which best models power consumption is given below:

$$P_{TOTAL} = 0.350 + f[0.0031 \eta_{LC} + 0.0948 \eta_{CKBF} + 0.01 \eta_{CLBF} + 0.0263 \eta_{CKLD} + 0.543 \eta_{RAM} + 0.20 \eta_{PLL} + 0.0035 \eta_{INP} + 0.0257 \eta_{OUTP}] \text{ (mW)}$$

Where

- η_{LC} is the total number of logic cells in the design
- η_{CKBF} = # of clock buffers
- η_{CLBF} = # of column clock buffers
- η_{CKLD} = # of loads connected to the column clock buffers
- η_{RAM} = # of RAM blocks
- η_{PLL} = # of PLLs
- η_{INP} is the number of input pins
- η_{OUTP} is the number of output pins

Figure 22 exhibits the power consumption in an EclipsePlus QL7100 device. The chip was filled with (300) 8-bit counters—approximately 76% logic cell utilization.

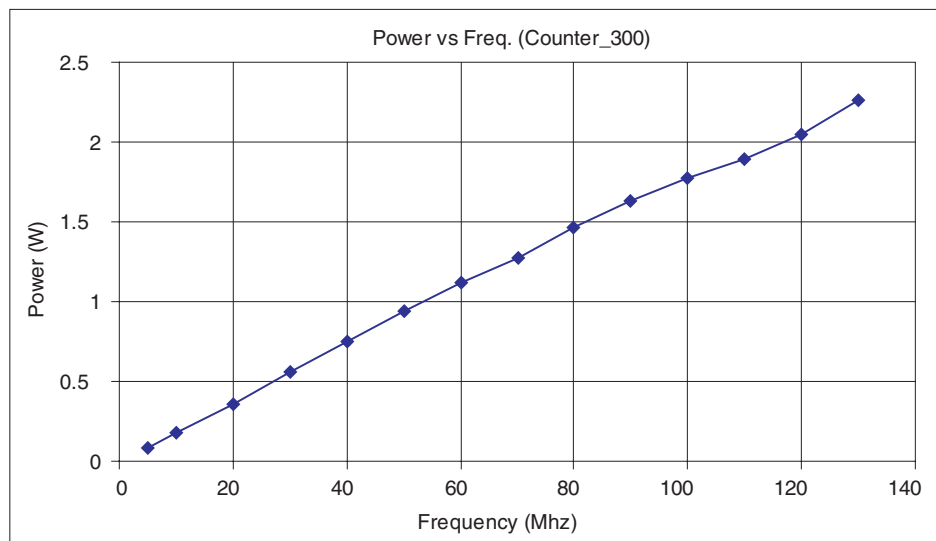


Figure 22: Power Consumption

Figure 23 illustrates the theoretical worst-case scenarios for 50%, 70%, and 90% utilizations of the 6600-516 package. The resources of the device are divided exactly in half; meaning, for 50% utilization, exactly 50% of the I/Os, Logic Cells, RAM blocks, clock network, etc. are utilized. These situations may never occur in a real design, but they do provide a very rough quantitative measure of power consumption when talking in terms of 50% or 70% utilization of an EclipsePlus device.

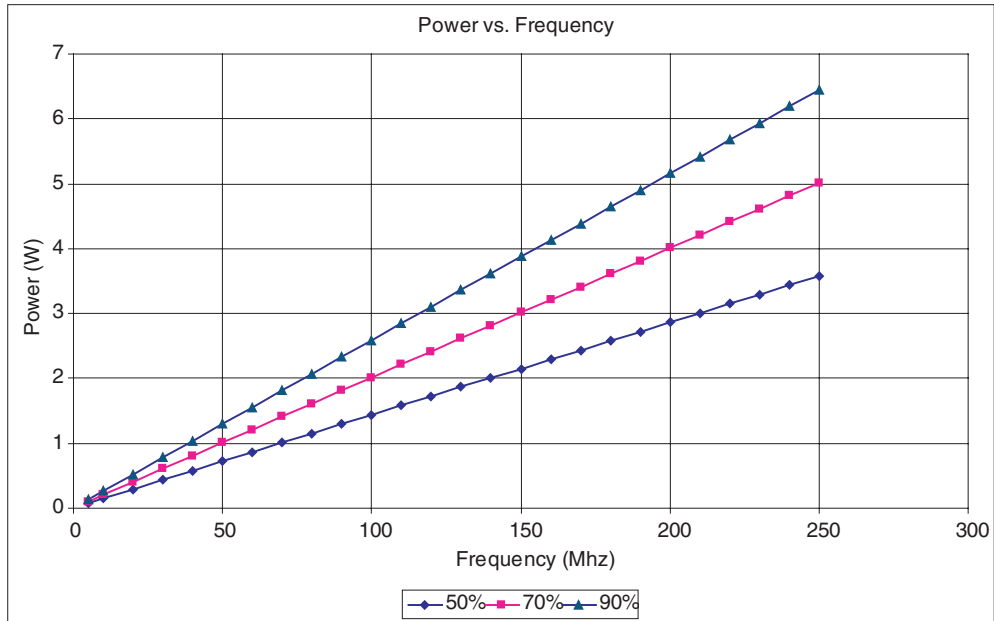


Figure 23: Power vs. Frequency (Absolute 50%, 70%, and 90% of the Available Resources on Chip)

NOTE: To learn more about power consumption, please refer to application note #60 which is located at <http://www.quicklogic.com/images/appnote60.pdf>.

Power-up Sequencing

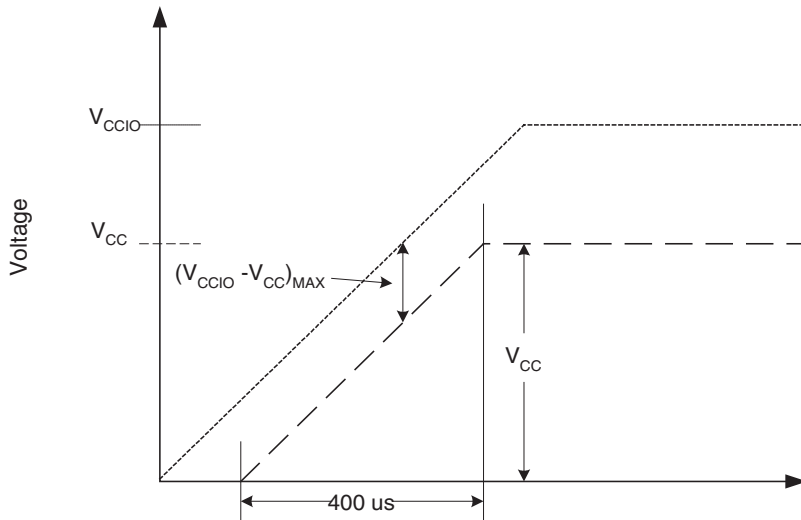


Figure 24: Power-up Requirements

The following requirements must be met when powering up a device (refer to **Figure 24**):

- When ramping up the power supplies keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV. Deviation from this recommendation can cause permanent damage to the device.
- V_{CCIO} must lead V_{CC} when ramping the device.
- The power supply must be greater than or equal to $400 \mu s$ to reach V_{CC} . Ramping to V_{CC}/V_{CCIO} before reaching $400 \mu s$ can cause the device to behave improperly.

A diode is present in-between V_{CC} and V_{CCIO} , as shown in **Figure 25**.

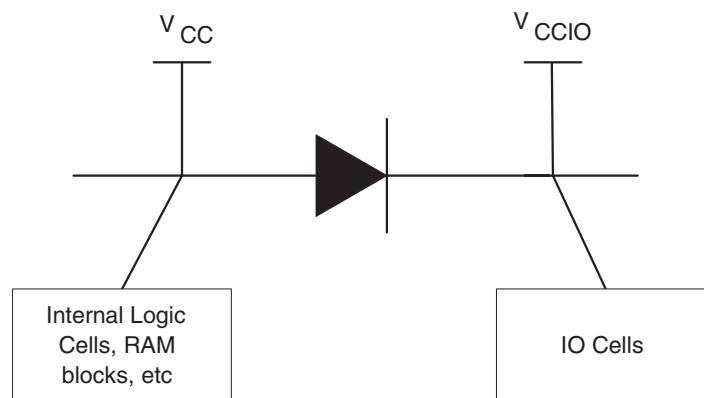


Figure 25: Internal Diode Between V_{CC} and V_{CCIO}

Joint Test Access Group (JTAG)

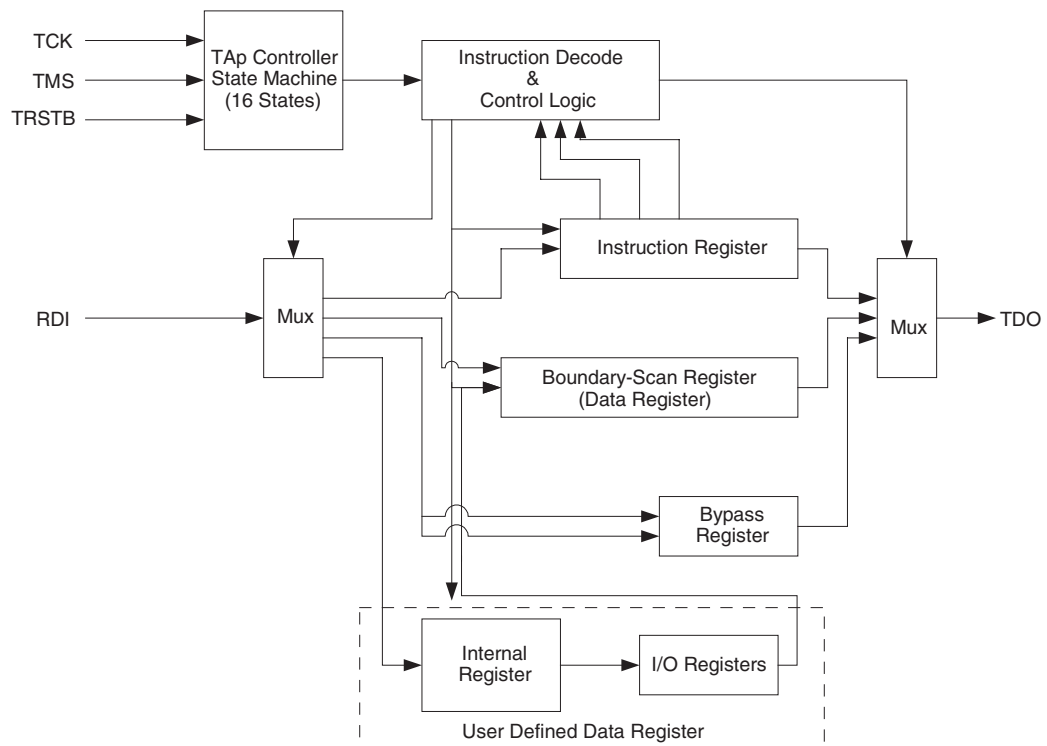


Figure 26: JTAG Block Diagram

Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, one problem being the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Pin Descriptions

Table 19: JTAG Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG/RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to V _{CC} if unused
TRSTB/RRO	Active low Reset for JTAG/RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V _{CC} if not used for JTAG
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V _{CC} or ground if not used for JTAG
TDO/RCO	Test data out for JTAG/RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization

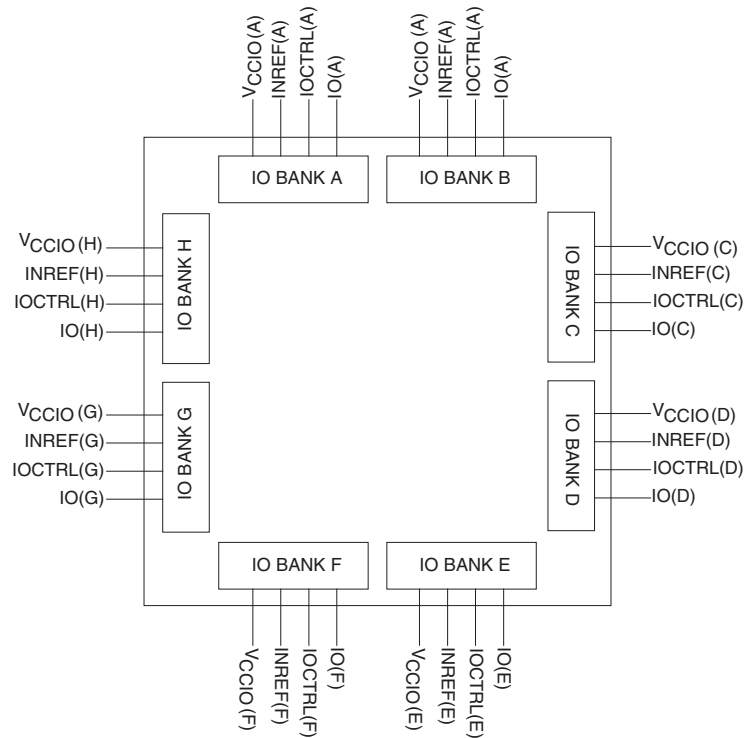


Figure 27: I/O Banks with Relevant Pins

Table 20: Dedicated Pin Descriptions

Pin	Function	Description
GCLK	Global clock network driver	Low skew global clock. This pin provides access to a dedicated, distributed network capable of driving the CLOCK, SET, RESET, F1, and A2 inputs to the Logic Cell, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, CLOCK of the ECUs, and Output Enables of the I/Os.
I/O(A)	Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The A inside the parenthesis means that the I/O is located in Bank A. If an I/O is not used, SpDE (QuickWorks Tool) provides the option of tying that pin to GND, V_{CC} , or TriState during programming.
V_{CC}	Power supply pin	Connect to 2.5 V supply
$V_{CCIO}(A)$	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V device or a 2.5 V device. The A inside the parenthesis means that V_{CCIO} is located in BANK A. Every I/O pin in Bank A will be tolerant of V_{CCIO} input signals and will output V_{CCIO} level signals. This pin must be connected to either 3.3 V or V_{CC} .
GND	Ground pin	Connect to ground
PLLIN	PLL clock input	Clock input for PLL
DEDCLK	Dedicated clock pin	Low skew global clock. This pin provides access to a dedicated, distributed clock network capable of driving the CLOCK inputs of all sequential elements of the device (e.g. RAM, Flip Flops).
GNDPLL	Ground pin for PLL	Connect to GND
INREF(A)	Differential reference voltage	The INREF is the reference voltage pin for GTL+, SSTL2, and STTL3 standards. Follow the recommendations provided in Table 17 for the appropriate standard. The A inside the parenthesis means that INREF is located in BANK A. This pin should be tied to GND if not needed.
PLLOUT	PLL output pin	Dedicated PLL output pin. Otherwise may be left unconnected
IOCTRL(A)	Highdrive input	This pin provides fast RESET, SET, CLOCK, and ENABLE access to the I/O cell flip-flops, providing fast clock-to-out and fast I/O response times. This pin can also double as a high-drive pin to the internal logic cells. The A inside the parenthesis means that IOCTRL is located in Bank A. This pin should be tied to GND or V_{CC} if it is not used.

Recommended Unused Pin Terminations for the EclipsePlus devices

All unused, general purpose I/O pins can be tied to V_{CC} , GND, or HIZ (high impedance) internally using the Configuration Editor. This option is given in the bottom-right corner of the placement window. To use the Placement Editor, choose **Constraint > Fix Placement** in the Option pull-down menu of SpDE.

The rest of the pins should be terminated at the board level in the manner presented in **Table 21**.

Table 21: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
PLLOUT<x> ^a	Unused PLL output pins must be connected to either V_{CC} or GND so that their associated input buffer never floats. Utilized PLL output pins that route the PLL clock outside of the chip should not be tied to either V_{CC} or GND.
IOCTRL<y> ^b	Any unused pins of this type must be connected to either V_{CC} or GND.
CLK/PLLIN<x>	Any unused clock pins should be connected to V_{CC} or GND.
PLL_RST<x>	If a PLL module is not used, then the associated PLL_RST<x> must be connected to V_{CC} ; under normal operation, use it as needed.
INREF<y>	If an I/O bank does not require the use of INREF signal the pin should be connected to GND.

a. x represents a number.

b. y represents an alphabetical character.

208 PQFP Pinout Diagram



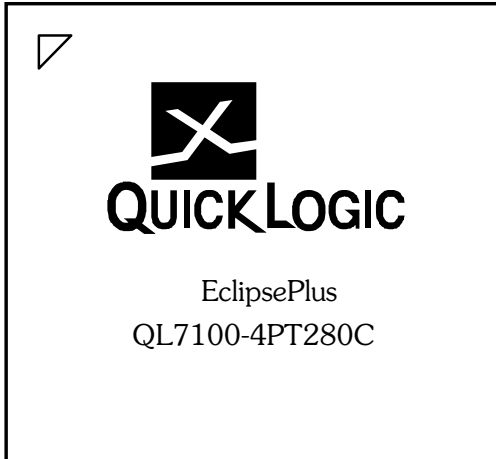
208 PQFP Pinout Table

Table 22: 208 PQFP Pinout Table

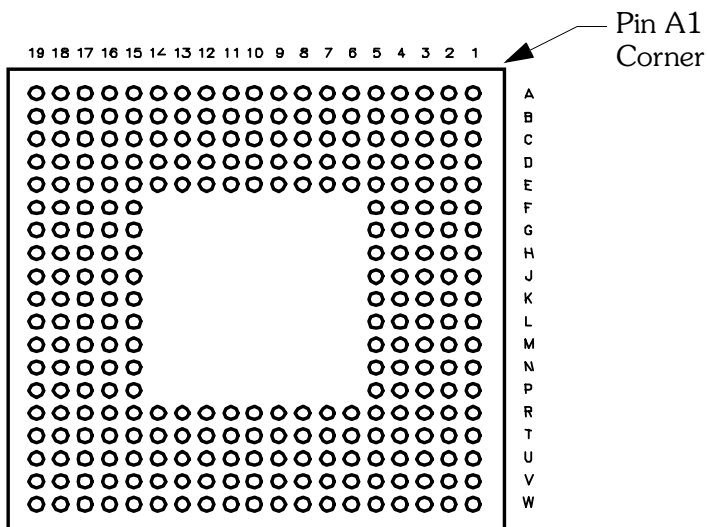
PQFP	Function	PQFP	Function	PQFP	Function	PQFP	Function	PQFP	Function
1	PLL RST(3)	43	IO(B)	85	IO(D)	127	CLK(5), PLLIN(3)	169	IOCTRL(G)
2	V _{CCPLL} (3)	44	V _{CCIO} (B)	86	V _{CC}	128	CLK(6)	170	INREF(G)
3	GND	45	IO(B)	87	IO(D)	129	V _{CC}	171	IOCTRL(G)
4	GND	46	V _{CC}	88	IO(D)	130	CLK(7)	172	IO(G)
5	IO(A)	47	IO(B)	89	V _{CC}	131	V _{CC}	173	IO(G)
6	IO(A)	48	IO(B)	90	IO(D)	132	CLK(8)	174	IO(V)
7	IO(A)	49	GND	91	IO(D)	133	TMS	175	V _{CC}
8	V _{CCIO} (A)	50	TDO	92	IOCTRL(D)	134	IO(F)	176	IO(G)
9	IO(A)	51	PLLOUT(1)	93	INREF(D)	135	IO(F)	177	V _{CCIO} (G)
10	IO(A)	52	GNDPLL(2)	94	IOCTRL(D)	136	IO(F)	178	GND
11	IOCTRL(A)	53	GND	95	IO(D)	137	GND	179	IO(G)
12	V _{CC}	54	V _{CCPLL} (2)	96	IO(D)	138	V _{CCIO} (F)	180	IO(G)
13	INREF(A)	55	PLL RST(2)	97	IO(D)	139	IO(F)	181	IO(G)
14	IOCTRL(A)	56	V _{CC}	98	V _{CCIO} (D)	140	IO(F)	182	V _{CC}
15	IO(A)	57	IO(C)	99	IO(D)	141	IO(F)	183	TCK
16	IO(A)	58	GND	100	IO(D)	142	IO(F)	184	V _{CC}
17	IO(A)	59	IO(C)	101	GND	143	IO(F)	185	IO(H)
18	IO(A)	60	V _{CCIO} (C)	102	PLLOUT(0)	144	IOCTRL(F)	186	IO(H)
19	V _{CCIO} (A)	61	IO(C)	103	GND	145	INREF(F)	187	IO(H)
20	IO(A)	62	IO(C)	104	GNDPLL(1)	146	V _{CC}	188	GND
21	GND	63	IO(C)	105	PLL RST(1)	147	IOCTRL(F)	189	V _{CCIO} (H)
22	IO(A)	64	IO(C)	106	V _{CCPLL} (1)	148	IO(F)	190	IO(H)
23	TDI	65	IO(C)	107	IO(E)	149	IO(F)	191	IO(H)
24	CLK(0)	66	IO(C)	108	GND	150	V _{CCIO} (F)	192	IOCTRL(H)
25	CLK(1)	67	IOCTRL(C)	109	IO(E)	151	IO(F)	193	IO(H)
26	V _{CC}	68	INREF(C)	110	IO(E)	152	IO(F)	194	INREF(H)
27	CLK(2), PLLIN(2)	69	IOCTRL(C)	111	V _{CCIO} (E)	153	GND	195	V _{CC}
28	CLK(3), PLLIN(1)	70	IO(C)	112	IO(E)	154	IO(F)	196	IOCTRL(H)
29	V _{CC}	71	IO(C)	113	V _{CC}	155	PLLOUT(3)	197	IO(H)
30	CLK(4), DEDCLK, PLLIN(0)	72	V _{CCIO} (C)	114	IO(E)	156	GNDPLL(0)	198	IO(H)
31	IO(B)	73	IO(C)	115	IO(E)	157	GND	199	IO(H)
32	IO(B)	74	IO(C)	116	IO(E)	158	V _{CCPLL} (0)	200	IO(H)
33	GND	75	GND	117	IOCTRL(E)	159	PLL RST(0)	201	IO(H)
34	V _{CCIO} (B)	76	V _{CC}	118	INREF(E)	160	GND	202	IO(H)
35	IO(B)	77	IO(C)	119	IOCTRL(E)	161	IO(G)	203	V _{CCIO} (H)
36	IO(B)	78	TRSTB	120	IO(E)	162	V _{CCIO} (G)	204	GND
37	IO(B)	79	V _{CC}	121	IO(E)	163	IO(G)	205	IO(H)
38	IO(B)	80	IO(D)	122	V _{CCIO} (E)	164	IO(G)	206	PLLOUT(2)
39	IOCTRL(B)	81	IO(D)	123	GND	165	V _{CC}	207	GND
40	INREF(B)	82	IO(D)	124	IO(E)	166	IO(G)	208	GNDPLL(3)
41	IOCTRL(B)	83	GND	125	IO(E)	167	IO(G)		
42	IO(B)	84	V _{CCIO} (D)	126	IO(E)	168	IO(G)		

280 PBGA Pinout Diagram

Top



Bottom



280 PBGA Pinout Table

Table 23: 280 PBGA Pinout Table

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	PLLOUT<3>	C10	CLK<5>/PLLIN<3>	E19	IOCTRL<D>	K16	I/O<C>	R4	I/O<H>	U13	I/O
A2	GNDPLL<0>	C11	V _{ccio} <E>	F1	INREF<G>	K17	I/O<D>	R5	GND	U14	IOCTRL
A3	I/O<F>	C12	I/O<E>	F2	IOCTRL<G>	K18	I/O<C>	R6	GND	U15	V _{ccio}
A4	I/O<F>	C13	I/O<E>	F3	I/O<G>	K19	TRSTB	R7	V _{cc}	U16	I/O
A5	I/O<F>	C14	I/O<E>	F4	I/O<G>	L1	I/O<H>	R8	V _{cc}	U17	TDO
A6	IOCTRL<F>	C15	V _{ccio} <E>	F5	GND	L2	I/O<H>	R9	GND	U18	PLLRST<2>
A7	I/O<F>	C16	I/O<E>	F15	V _{cc}	L3	V _{ccio} <H>	R10	GND	U19	I/O
A8	I/O<F>	C17	I/O<E>	F16	IOCTRL<D>	L4	I/O<H>	R11	V _{cc}	V1	PLLOUT<2>
A9	I/O<F>	C18	I/O<E>	F17	I/O<D>	L5	V _{cc}	R12	V _{cc}	V2	GNDPLL<3>
A10	CLK<7>	C19	I/O<E>	F18	I/O<D>	L15	GND	R13	V _{cc}	V3	GND
A11	I/O<E>	D1	I/O<G>	F19	I/O<D>	L16	I/O<C>	R14	V _{cc}	V4	I/O<A>
A12	I/O<E>	D2	I/O<G>	G1	I/O<G>	L17	V _{ccio} <C>	R15	GND	V5	I/O<A>
A13	I/O<E>	D3	I/O<F>	G2	I/O<G>	L18	I/O<C>	R16	I/O<C>	V6	IOCTRL<A>
A14	IOCTRL<E>	D4	I/O<F>	G3	IOCTRL<G>	L19	I/O<C>	R17	V _{ccio} <C>	V7	I/O<A>
A15	I/O<E>	D5	I/O<F>	G4	I/O<G>	M1	I/O<H>	R18	I/O<C>	V8	I/O<A>
A16	I/O<E>	D6	I/O<F>	G5	V _{cc}	M2	I/O<H>	R19	I/O<C>	V9	I/O<A>
A17	I/O<E>	D7	I/O<F>	G15	V _{cc}	M3	I/O<H>	T1	I/O<H>	V10	CLK<1>
A18	PLLRST<1>	D8	I/O<F>	G16	I/O<D>	M4	I/O<H>	T2	I/O<H>	V11	CLK<4> DEDCLK/PLLIN<0>
A19	GND	D9	CLK<8>	G17	I/O<D>	M5	V _{cc}	T3	I/O<A>	V12	I/O
B1	PLLRST<0>	D10	I/O<E>	G18	I/O<D>	M15	V _{cc}	T4	I/O<A>	V13	I/O
B2	GND	D11	I/O<E>	G19	I/O<D>	M16	INREF<C>	T5	I/O<A>	V14	INREF
B3	I/O<F>	D12	I/O<E>	H1	I/O<G>	M17	I/O<C>	T6	IOCTRL<A>	V15	I/O
B4	I/O<F>	D13	INREF<E>	H2	I/O<G>	M18	I/O<C>	T7	I/O<A>	V16	I/O
B5	I/O<F>	D14	I/O<E>	H3	I/O<G>	M19	I/O<C>	T8	I/O<A>	V17	I/O
B6	INREF<F>	D15	I/O<E>	H4	I/O<G>	N1	IOCTRL<H>	T9	I/O<A>	V18	GNDPLL<2>
B7	I/O<F>	D16	I/O<D>	H5	V _{cc}	N2	I/O<H>	T10	I/O<A>	V19	GND
B8	I/O<F>	D17	I/O<D>	H15	V _{cc}	N3	I/O<H>	T11	CLK<3>/PLLIN<1>	W1	GND
B9	TMS	D18	I/O<D>	H16	V _{cc}	N4	I/O<H>	T12	I/O	W2	PLLRST<3>
B10	CLK<6>	D19	I/O<D>	H17	I/O<D>	N5	V _{cc}	T13	I/O	W3	I/O<A>
B11	I/O<E>	E1	I/O<G>	H18	I/O<D>	N15	V _{cc}	T14	I/O	W4	I/O<A>
B12	I/O<E>	E2	I/O<G>	H19	I/O<D>	N16	I/O<C>	T15	I/O	W5	I/O<A>
B13	IOCTRL<E>	E3	V _{ccio} <G>	J1	I/O<G>	N17	I/O<C>	T16	I/O	W6	I/O<A>
B14	I/O<E>	E4	I/O<F>	J2	I/O<G>	N18	IOCTRL<C>	T17	V _{ccPLL} <2>	W7	I/O<A>
B15	I/O<E>	E5	GND	J3	V _{ccio} <G>	N19	IOCTRL<C>	T18	I/O	W8	I/O<A>
B16	I/O<E>	E6	V _{cc}	J4	I/O<G>	P1	I/O<H>	T19	I/O	W9	TDI
B17	V _{ccPLL} <1>	E7	V _{cc}	J5	GND	P2	I/O<H>	U1	I/O<A>	W10	CLK<2>/PLLIN<2>
B18	GNDPLL<1>	E8	V _{cc}	J15	V _{cc}	P3	IOCTRL<H>	U2	I/O<A>	W11	I/O
B19	PLLOUT<0>	E9	V _{cc}	J16	I/O<C>	P4	INREF<H>	U3	V _{ccPLL} <3>	W12	I/O
C1	I/O<F>	E10	GND	J17	V _{ccio} <D>	P5	V _{cc}	U4	I/O<A>	W13	I/O
C2	V _{ccPLL} <0>	E11	GND	J18	I/O<D>	P15	GND	U5	V _{ccio} <A>	W14	IOCTRL
C3	I/O<F>	E12	V _{cc}	J19	I/O<D>	P16	I/O<C>	U6	INREF<A>	W15	I/O
C4	I/O<F>	E13	V _{cc}	K1	V _{cc}	P17	I/O<C>	U7	I/O<A>	W16	I/O
C5	V _{ccio} <F>	E14	GND	K2	TCK	P18	I/O<C>	U8	I/O<A>	W17	I/O
C6	IOCTRL<F>	E15	GND	K3	I/O<G>	P19	I/O<C>	U9	V _{ccio} <A>	W18	I/O
C7	I/O<F>	E16	I/O<D>	K4	I/O<G>	R1	I/O<H>	U10	CLK<0>	W19	PLLOUT<1>
C8	I/O<F>	E17	V _{ccio} <D>	K5	GND	R2	I/O<H>	U11	V _{ccio} 		
C9	V _{ccio} <F>	E18	INREF<D>	K15	GND	R3	V _{ccio} <H>	U12	I/O		

280 PBGA Packaging Drawing

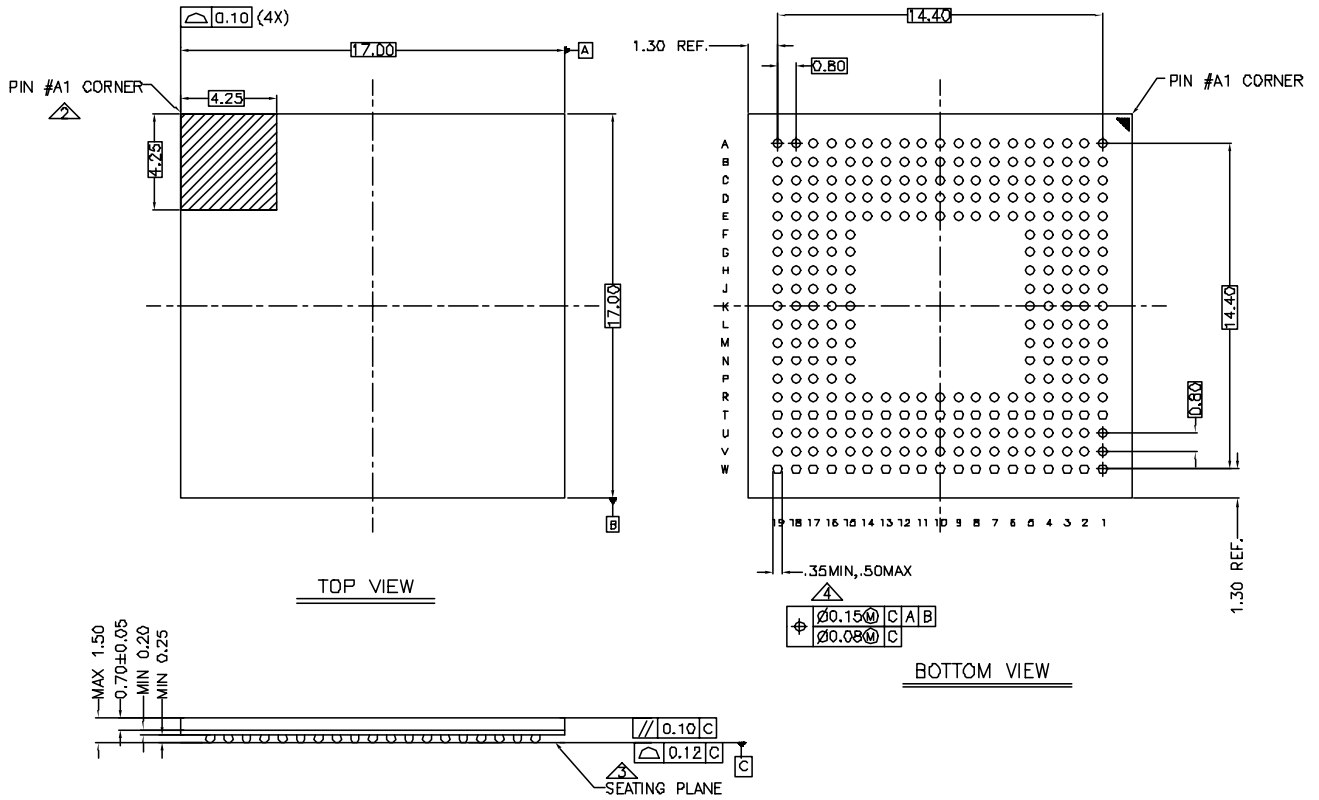
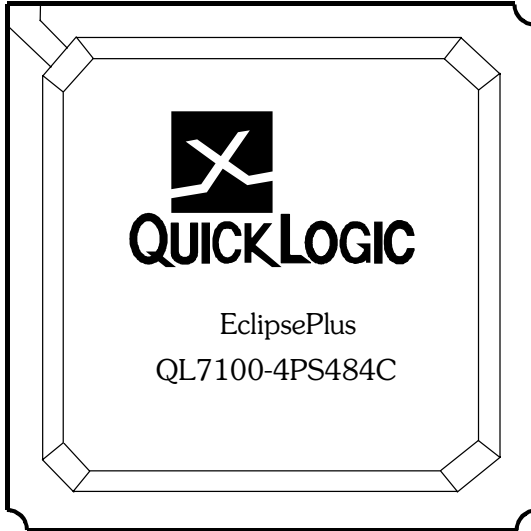


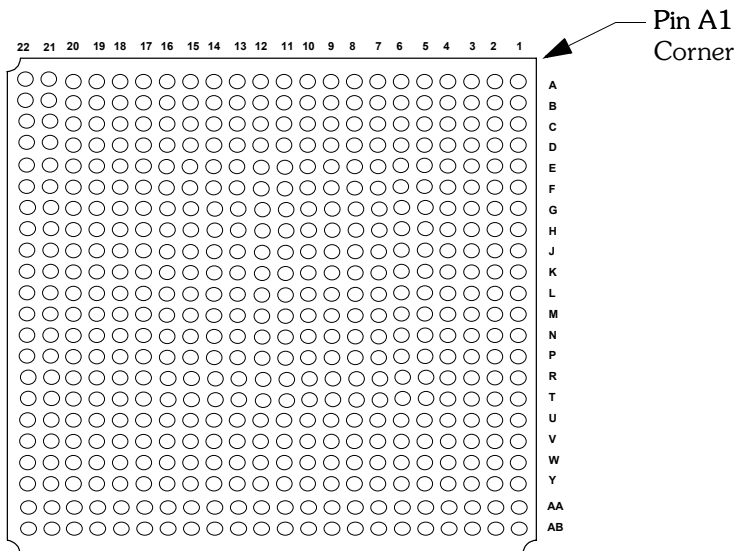
Figure 28: 280 PBGA Packaging Drawing

484 PBGA Pinout Diagram

Top



Bottom



484 PBGA Pinout Table

Table 24: 484 PBGA Pinout Table

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	NC	C1	NC	E1	IOCTRL<A>	G1	NC	J1	I/O<A>	L1	CLK<4> DEDCLK/PLLIN<0>
A2	PLLIRST<3>	C2	I/O<A>	E2	I/O<A>	G2	NC	J2	I/O<A>	L2	CLK<0>
A3	I/O<A>	C3	V _{CCPLL} <3>	E3	I/O<A>	G3	I/O<A>	J3	I/O<A>	L3	CLK<2>/PLLIN<2>
A4	I/O<A>	C4	PLLOUT<2>	E4	I/O<A>	G4	I/O<A>	J4	I/O<A>	L4	I/O<A>
A5	I/O<A>	C5	I/O<A>	E5	NC	G5	I/O<A>	J5	I/O<A>	L5	I/O<A>
A6	NC	C6	NC	E6	I/O<H>	G6	I/O<A>	J6	I/O<A>	L6	I/O<A>
A7	I/O<H>	C7	I/O<H>	E7	NC	G7	GND	J7	I/O<A>	L7	GND
A8	IOCTRL<H>	C8	NC	E8	I/O<H>	G8	I/O<H>	J8	V _{CC}	L8	GND
A9	I/O<H>	C9	IOCTRL<H>	E9	I/O<H>	G9	I/O<H>	J9	GND	L9	GND
A10	NC	C10	NC	E10	I/O<H>	G10	NC	J10	V _{CC}	L10	GND
A11	NC	C11	I/O<H>	E11	V _{CC}	G11	I/O<G>	J11	V _{CC}	L11	GND
A12	TCK	C12	NC	E12	I/O<G>	G12	GND	J12	GND	L12	GND
A13	I/O<G>	C13	I/O<G>	E13	I/O<G>	G13	NC	J13	V _{CC}	L13	GND
A14	I/O<G>	C14	NC	E14	NC	G14	NC	J14	GND	L14	V _{CC}
A15	I/O<G>	C15	I/O<G>	E15	IOCTRL<G>	G15	I/O<G>	J15	V _{CC}	L15	V _{CC}
A16	NC	C16	I/O<G>	E16	I/O<G>	G16	GND	J16	I/O<F>	L16	CLK<6>
A17	I/O<G>	C17	NC	E17	INREF<G>	G17	V _{CCIO} <F>	J17	V _{CCIO} <F>	L17	V _{CCIO} <F>
A18	I/O<G>	C18	I/O<G>	E18	NC	G18	I/O<F>	J18	I/O<F>	L18	I/O<F>
A19	I/O<F>	C19	I/O<F>	E19	I/O<F>	G19	I/O<F>	J19	I/O<F>	L19	CLK<8>
A20	GND	C20	GNDPLL<0>	E20	I/O<F>	G20	I/O<F>	J20	I/O<F>	L20	I/O<F>
A21	PLLOUT<3>	C21	I/O<F>	E21	NC	G21	INREF<F>	J21	I/O<F>	L21	NC
A22	I/O<F>	C22	I/O<F>	E22	I/O<F>	G22	I/O<F>	J22	I/O<F>	L22	I/O<F>
B1	I/O<A>	D1	I/O<A>	F1	I/O<A>	H1	I/O<A>	K1	TDI	M1	I/O
B2	GND	D2	I/O<A>	F2	INREF<A>	H2	I/O<A>	K2	I/O<A>	M2	I/O
B3	GNDPLL<3>	D3	I/O<A>	F3	NC	H3	I/O<A>	K3	I/O<A>	M3	I/O
B4	GND	D4	I/O<A>	F4	I/O<A>	H4	I/O<A>	K4	I/O<A>	M4	CLK<3>/PLLIN<1>
B5	I/O<A>	D5	I/O<A>	F5	I/O<A>	H5	IOCTRL<A>	K5	I/O<A>	M5	NC
B6	I/O<H>	D6	I/O<H>	F6	V _{CCIO} <A>	H6	V _{CCIO} <A>	K6	V _{CCIO} <A>	M6	V _{CCIO}
B7	I/O<H>	D7	NC	F7	V _{CCIO} <H>	H7	I/O<H>	K7	NC	M7	CLK<1>
B8	INREF<H>	D8	I/O<H>	F8	I/O<H>	H8	GND	K8	V _{CC}	M8	V _{CC}
B9	I/O<H>	D9	NC	F9	V _{CCIO} <H>	H9	V _{CC}	K9	V _{CC}	M9	V _{CC}
B10	I/O<H>	D10	I/O<H>	F10	I/O<H>	H10	V _{CC}	K10	GND	M10	GND
B11	I/O<H>	D11	I/O<H>	F11	V _{CCIO} <H>	H11	V _{CC}	K11	GND	M11	GND
B12	NC	D12	I/O<G>	F12	V _{CCIO} <G>	H12	GND	K12	GND	M12	GND
B13	NC	D13	I/O<G>	F13	I/O<G>	H13	V _{CC}	K13	GND	M13	GND
B14	NC	D14	I/O<G>	F14	V _{CCIO} <G>	H14	V _{CC}	K14	V _{CC}	M14	GND
B15	NC	D15	IOCTRL<G>	F15	NC	H15	GND	K15	V _{CC}	M15	GND
B16	I/O<G>	D16	I/O<G>	F16	V _{CCIO} <G>	H16	I/O<F>	K16	NC	M16	GND
B17	I/O<G>	D17	I/O<G>	F17	NC	H17	I/O<F>	K17	I/O<F>	M17	I/O<E>
B18	I/O<G>	D18	I/O<F>	F18	I/O<F>	H18	NC	K18	I/O<F>	M18	I/O<E>
B19	PLLIRST<0>	D19	V _{CCPLL} <0>	F19	I/O<F>	H19	I/O<F>	K19	NC	M19	I/O<E>
B20	I/O<F>	D20	I/O<F>	F20	IOCTRL<F>	H20	I/O<F>	K20	I/O<F>	M20	CLK<7>
B21	I/O<F>	D21	I/O<F>	F21	I/O<F>	H21	I/O<F>	K21	I/O<F>	M21	CLK<5>/PLLIN<3>
B22	I/O<F>	D22	I/O<F>	F22	IOCTRL<F>	H22	NC	K22	NC	M22	TMS

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Table 24: 484 PBGA Pinout Table (Continued)

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
N1	NC	P16	I/O<E>	T9	NC	V2	I/O	W17	NC	AA10	I/O<C>
N2	I/O	P17	NC	T10	TRSTB	V3	I/O	W18	I/O<E>	AA11	I/O<C>
N3	I/O	P18	I/O<E>	T11	GND	V4	I/O	W19	NC	AA12	I/O<D>
N4	NC	P19	NC	T12	NC	V5	I/O	W20	I/O<E>	AA13	I/O<D>
N5	I/O	P20	I/O<E>	T13	I/O<D>	V6	NC	W21	NC	AA14	I/O<D>
N6	NC	P21	I/O<E>	T14	NC	V7	I/O<C>	W22	I/O<E>	AA15	I/O<D>
N7	NC	P22	I/O<E>	T15	I/O<D>	V8	I/O<C>	Y1	I/O	AA16	NC
N8	V _{CC}	R1	I/O	T16	GND	V9	NC	Y2	I/O	AA17	NC
N9	V _{CC}	R2	INREF	T17	I/O<E>	V10	I/O<C>	Y3	V _{CCPLL<2>}	AA18	I/O<D>
N10	GND	R3	I/O	T18	I/O<E>	V11	NC	Y4	I/O<C>	AA19	I/O<E>
N11	GND	R4	I/O	T19	NC	V12	V _{CC}	Y5	I/O<C>	AA20	GNDPLL<1>
N12	GND	R5	I/O	T20	NC	V13	NC	Y6	I/O<C>	AA21	I/O<E>
N13	GND	R6	NC	T21	IOCTRL<E>	V14	I/O<D>	Y7	I/O<C>	AA22	I/O<E>
N14	V _{CC}	R7	I/O	T22	I/O<E>	V15	I/O<D>	Y8	IOCTRL<C>	AB1	I/O
N15	V _{CC}	R8	GND	U1	IOCTRL	V16	INREF<D>	Y9	I/O<C>	AB2	GNDPLL<2>
N16	I/O<E>	R9	V _{CC}	U2	I/O	V17	I/O<D>	Y10	I/O<C>	AB3	PLL _{RST<2>}
N17	V _{CCIO<E>}	R10	V _{CC}	U3	IOCTRL	V18	I/O<E>	Y11	I/O<D>	AB4	I/O
N18	I/O<E>	R11	GND	U4	I/O	V19	I/O<E>	Y12	NC	AB5	I/O
N19	I/O<E>	R12	V _{CC}	U5	I/O	V20	I/O<E>	Y13	NC	AB6	I/O<C>
N20	I/O<E>	R13	V _{CC}	U6	I/O<C>	V21	I/O<E>	Y14	I/O<D>	AB7	I/O<C>
N21	I/O<E>	R14	V _{CC}	U7	V _{CCIO<C>}	V22	I/O<E>	Y15	IOCTRL<D>	AB8	IOCTRL<C>
N22	I/O<E>	R15	GND	U8	NC	W1	I/O	Y16	I/O<D>	AB9	I/O<C>
P1	NC	R16	I/O<D>	U9	V _{CCIO<C>}	W2	I/O	Y17	I/O<D>	AB10	I/O<C>
P2	I/O	R17	V _{CCIO<E>}	U10	I/O<C>	W3	I/O	Y18	I/O<E>	AB11	NC
P3	I/O	R18	I/O<E>	U11	V _{CCIO<C>}	W4	I/O	Y19	PLLOUT<0>	AB12	I/O<D>
P4	I/O	R19	I/O<E>	U12	V _{CCIO<D>}	W5	I/O	Y20	PLL _{RST<1>}	AB13	I/O<D>
P5	I/O	R20	I/O<E>	U13	I/O<D>	W6	I/O<C>	Y21	I/O<E>	AB14	NC
P6	V _{CCIO}	R21	I/O<E>	U14	V _{CCIO<D>}	W7	NC	Y22	I/O<E>	AB15	I/O<D>
P7	I/O	R22	I/O<E>	U15	NC	W8	NC	AA1	TDO	AB16	IOCTRL<D>
P8	V _{CC}	T1	I/O	U16	V _{CCIO<D>}	W9	NC	AA2	PLLOUT<1>	AB17	I/O<D>
P9	GND	T2	I/O	U17	V _{CCIO<E>}	W10	NC	AA3	GND	AB18	I/O<D>
P10	V _{CC}	T3	I/O	U18	I/O<E>	W11	I/O<C>	AA4	I/O	AB19	I/O<E>
P11	GND	T4	I/O	U19	I/O<E>	W12	NC	AA5	I/O<C>	AB20	GND
P12	V _{CC}	T5	I/O	U20	IOCTRL<E>	W13	I/O<D>	AA6	I/O<C>	AB21	V _{CCPLL<1>}
P13	V _{CC}	T6	V _{CCIO}	U21	NC	W14	NC	AA7	NC	AB22	I/O<E>
P14	GND	T7	GND	U22	INREF<E>	W15	I/O<D>	AA8	INREF<C>		
P15	V _{CC}	T8	I/O<C>	V1	I/O	W16	NC	AA9	NC		

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484 PBGA Packaging Drawing

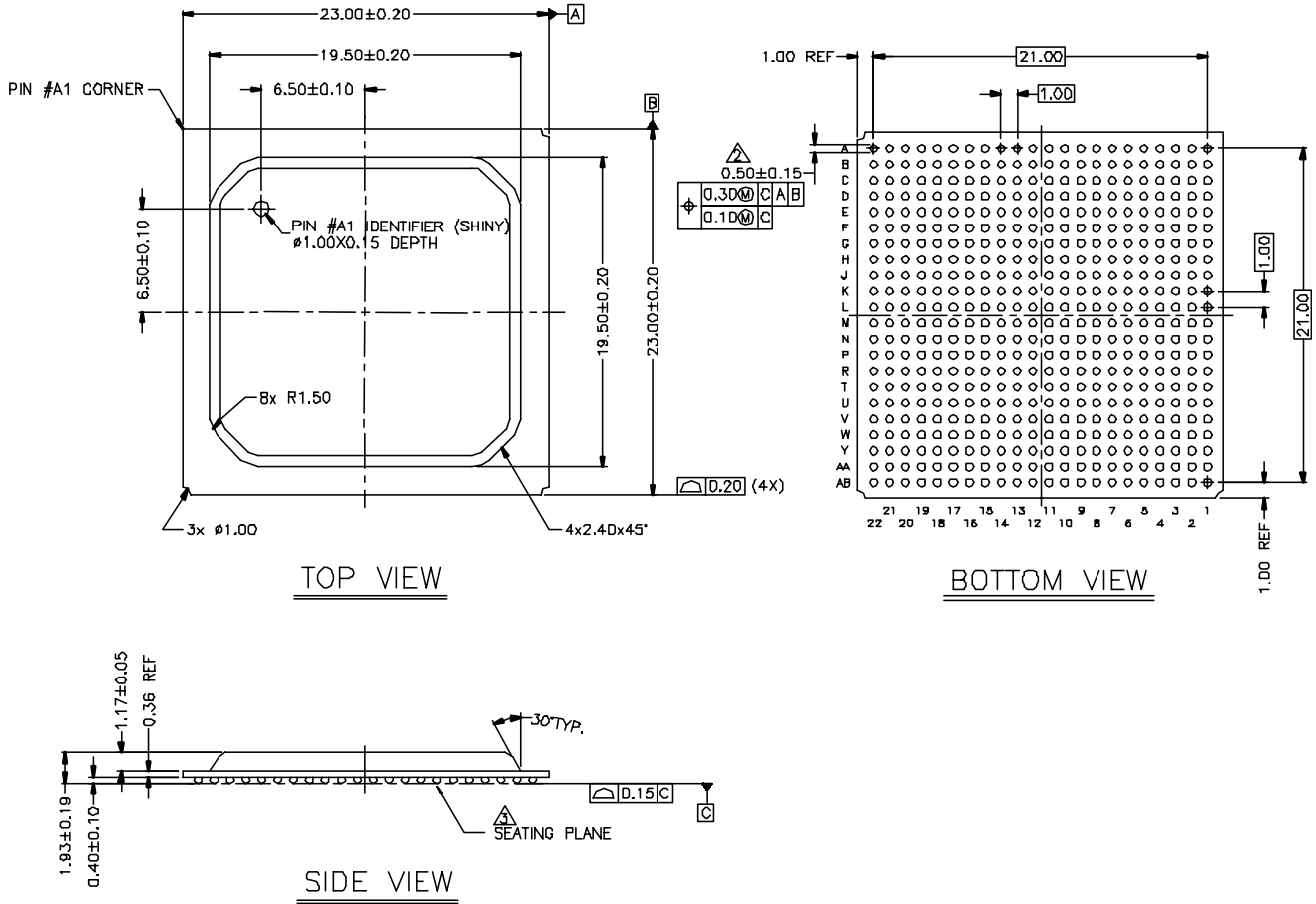
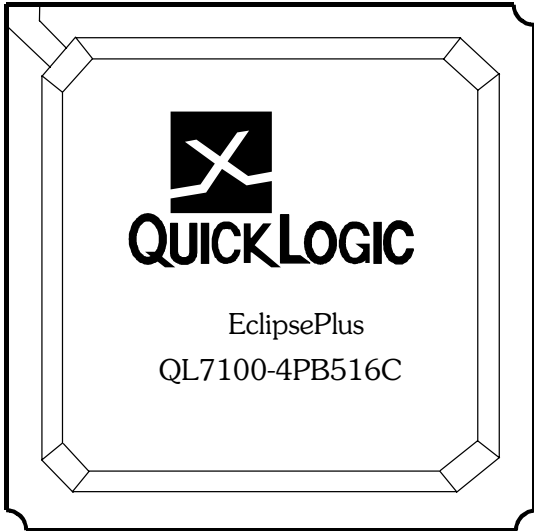


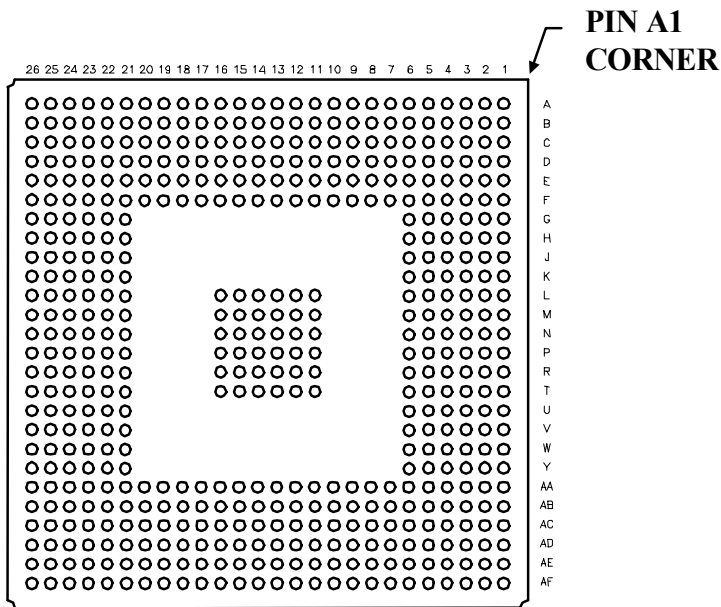
Figure 29: 484 PBGA Packaging Drawing

516 PBGA Pinout Diagram

Top



Bottom



516 PBGA Pinout Table

Table 25: 516 PBGA Pinout Table

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	GND	C1	IO(F)	E1	IO(G)	G1	NC	L5	V _{CC}	P3	IO(H)
A2	IO(F)	C2	NC	E2	IO(G)	G2	INREF(G)	L6	V _{CC}	P4	V _{CC}
A3	IO(F)	C3	IO(F)	E3	NC	G3	IO(G)	L11	GND	P5	IO(H)
A4	IO(F)	C4	PLLOUT(3)	E4	V _{CCPLL(0)}	G4	IO(G)	L12	GND	P6	V _{CCIO(H)}
A5	NC	C5	IO(F)	E5	IO(F)	G5	IO(G)	L13	GND	P11	GND
A6	IO(F)	C6	IO(F)	E6	IO(F)	G6	V _{CCIO(G)}	L14	GND	P12	GND
A7	IOCTRL(F)	C7	IO(F)	E7	IO(F)	G21	V _{CCIO(D)}	L15	GND	P13	GND
A8	IO(F)	C8	INREF(F)	E8	V _{CC}	G22	IO(D)	L16	GND	P14	GND
A9	IO(F)	C9	IO(F)	E9	NC	G23	IO(D)	L21	V _{CC}	P15	GND
A10	IO(F)	C10	NC	E10	IO(F)	G24	NC	L22	IO(D)	P16	GND
A11	NC	C11	IO(F)	E11	IO(F)	G25	NC	L23	IO(D)	P21	V _{CCIO(C)}
A12	IO(F)	C12	NC	E12	V _{CC}	G26	INREF(D)	L24	NC	P22	IO(C)
A13	IO(E)	C13	CLK(7)	E13	IO(F)	H1	NC	L25	IO(D)	P23	V _{CC}
A14	NC	C14	IO(E)	E14	IO(F)	H2	IO(G)	L26	IO(D)	P24	NC
A15	IO(E)	C15	IO(E)	E15	IO(E)	H3	IOCTRL(G)	M1	NC	P25	NC
A16	IO(E)	C16	IO(E)	E16	V _{CC}	H4	IO(G)	M2	NC	P26	TRSTB
A17	IO(E)	C17	NC	E17	CLK(6)	H5	IO(G)	M3	NC	R1	NC
A18	IOCTRL(E)	C18	IO(E)	E18	IO(E)	H6	V _{CC}	M4	NC	R2	IO(H)
A19	IOCTRL(E)	C19	IO(E)	E19	NC	H21	V _{CC}	M5	IO(G)	R3	NC
A20	NC	C20	IO(E)	E20	IO(E)	H22	V _{CC}	M6	V _{CCIO(G)}	R4	IO(H)
A21	IO(E)	C21	IO(E)	E21	NC	H23	IO(D)	M11	GND	R5	V _{CC}
A22	NC	C22	IO(E)	E22	NC	H24	IOCTRL(D)	M12	GND	R6	V _{CC}
A23	IO(E)	C23	IO(E)	E23	GNDPLL(1)	H25	IOCTRL(D)	M13	GND	R11	GND
A24	IO(E)	C24	IO(E)	E24	IO(E)	H26	IO(D)	M14	GND	R12	GND
A25	PLL RST(1)	C25	IO(E)	E25	IO(D)	J1	NC	M15	GND	R13	GND
A26	GND	C26	IO(E)	E26	IO(D)	J2	IO(G)	M16	GND	R14	GND
B1	IO(F)	D1	IO(G)	F1	IOCTRL(G)	J3	IO(G)	M21	V _{CCIO(D)}	R15	GND
B2	PLL RST(0)	D2	IO(G)	F2	NC	J4	NC	M22	V _{CC}	R16	GND
B3	IO(F)	D3	IO(F)	F3	NC	J5	IO(G)	M23	NC	R21	V _{CC}
B4	IO(F)	D4	NC	F4	NC	J6	V _{CCIO(G)}	M24	NC	R22	IO(C)
B5	IO(F)	D5	GNDPLL(0)	F5	IO(F)	J21	V _{CCIO(D)}	M25	IO(D)	R23	NC
B6	IO(F)	D6	IO(F)	F6	GND	J22	IO(D)	M26	NC	R24	NC
B7	IOCTRL(F)	D7	IO(F)	F7	V _{CCIO(F)}	J23	IO(D)	N1	TCK	R25	NC
B8	IO(F)	D8	NC	F8	V _{CC}	J24	NC	N2	NC	R26	IO(C)
B9	IO(F)	D9	IO(F)	F9	V _{CCIO(F)}	J25	IO(D)	N3	IO(G)	T1	NC
B10	IO(F)	D10	IO(F)	F10	GND	J26	IO(D)	N4	IO(G)	T2	IO(H)
B11	IO(F)	D11	IO(F)	F11	V _{CC}	K1	NC	N5	IO(G)	T3	IO(H)
B12	IO(F)	D12	NC	F12	V _{CCIO(F)}	K2	IO(G)	N6	GND	T4	IO(H)
B13	CLK(5), PLLI N(3)	D13	TMS	F13	GND	K3	IO(G)	N11	GND	T5	NC
B14	IO(E)	D14	IO(E)	F14	V _{CCIO(E)}	K4	IO(G)	N12	GND	T6	V _{CC}
B15	IO(E)	D15	IO(E)	F15	V _{CC}	K5	NC	N13	GND	T11	GND
B16	IO(E)	D16	NC	F16	V _{CC}	K6	GND	N14	GND	T12	GND
B17	IO(E)	D17	IO(E)	F17	GND	K21	GND	N15	GND	T13	GND
B18	INREF(E)	D18	IO(F)	F18	V _{CCIO(E)}	K22	IO(D)	N16	GND	T14	GND
B19	IO(E)	D19	CLK(8)	F19	V _{CC}	K23	IO(D)	N21	GND	T15	GND
B20	NC	D20	IO(E)	F20	V _{CCIO(E)}	K24	NC	N22	IO(D)	T16	GND
B21	IO(E)	D21	IO(E)	F21	GND	K25	NC	N23	IO(D)	T21	V _{CC}
B22	IO(E)	D22	NC	F22	NC	K26	NC	N24	NC	T22	V _{CC}
B23	IO(E)	D23	V _{CCPLL(1)}	F23	NC	L1	IO(G)	N25	IO(D)	T23	NC
B24	IO(E)	D24	IO(E)	F24	IO(D)	L2	NC	N26	IO(D)	T24	IO(C)
B25	IO(E)	D25	IO(E)	F25	NC	L3	IO(G)	P1	NC	T25	NC
B26	PLLOUT(0)	D26	NC	F26	IO(D)	L4	IO(G)	P2	IO(H)	T26	IO(C)

(Sheet 1 of 2)

Table 25: 516 PBGA Pinout Table (Continued)

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
U1	IO(H)	W25	INREF(C)	AA21	GND	AC3	IO(A)	AD11	IO(A)	AE19	IO(B)
U2	IO(H)	W26	IO(C)	AA22	V _{CCPLL(2)}	AC4	IO(A)	AD12	TDI	AE20	IO(B)
U3	NC	Y1	IO(H)	AA23	IO(C)	AC5	IO(A)	AD13	CLK(4), DEDCLK, PLLIN(0)	AE21	IO(B)
U4	IO(H)	Y2	IO(H)	AA24	IO(C)	AC6	IO(A)	AD14	IO(A)	AE22	IO(B)
U5	IO(H)	Y3	NC	AA25	IO(C)	AC7	IO(A)	AD15	NC	AE23	IO(B)
U6	GND	Y4	IO(H)	AA26	NC	AC8	IO(A)	AD16	IO(B)	AE24	IO(B)
U21	GND	Y5	IO(H)	AB1	IO(H)	AC9	IO(A)	AD17	NC	AE25	PLL _{RST} (2)
U22	NC	Y6	V _{CCIO(H)}	AB2	NC	AC10	NC	AD18	INREF(B)	AE26	IO(B)
U23	NC	Y21	V _{CCIO(C)}	AB3	IO(A)	AC11	IO(A)	AD19	IO(B)	AF1	IO(A)
U24	NC	Y22	NC	AB4	GNDPLL(3)	AC12	IO(A)	AD20	IO(B)	AF2	IO(A)
U25	IO(C)	Y23	IO(C)	AB5	V _{CCPLL(3)}	AC13	NC	AD21	IO(B)	AF3	NC
U26	IO(C)	Y24	IO(C)	AB6	NC	AC14	CLK(1)	AD22	IO(B)	AF4	IO(A)
V1	IO(H)	Y25	NC	AB7	NC	AC15	NC	AD23	IO(B)	AF5	IO(A)
V2	IOCTRL(H)	Y26	IOCTRL(C)	AB8	IO(A)	AC16	NC	AD24	GND	AF6	IOCTRL(A)
V3	IOCTRL(H)	AA1	IO(H)	AB9	IO(A)	AC17	IO(B)	AD25	IO(B)	AF7	IO(A)
V4	IO(H)	AA2	IO(H)	AB10	IO(A)	AC18	IO(B)	AD26	IO(B)	AF8	IO(A)
V5	NC	AA3	NC	AB11	V _{CC}	AC19	IO(B)	AE1	GND	AF9	NC
V6	V _{CCIO(H)}	AA4	IO(A)	AB12	IO(A)	AC20	IO(B)	AE2	GND	AF10	IO(A)
V21	V _{CCIO(C)}	AA5	IO(A)	AB13	IO(A)	AC21	IO(B)	AE3	IO(A)	AF11	IO(A)
V22	IO(C)	AA6	GND	AB14	CLK(3),PLLIN(1)	AC22	TDO	AE4	IO(A)	AF12	CLK(2),PLLIN(2)
V23	NC	AA7	V _{CCIO(A)}	AB15	V _{CC}	AC23	PLL _{OUT} (1)	AE5	IO(A)	AF13	NC
V24	IOCTRL(C)	AA8	V _{CC}	AB16	IO(B)	AC24	IO(B)	AE6	IO(A)	AF14	IO(B)
V25	IO(C)	AA9	V _{CCIO(A)}	AB17	NC	AC25	NC	AE7	INREF(A)	AF15	IO(B)
V26	IO(C)	AA10	GND	AB18	IO(B)	AC26	IO(C)	AE8	NC	AF16	IO(B)
W1	INREF(H)	AA11	V _{CC}	AB19	V _{CC}	AD1	IO(A)	AE9	IO(A)	AF17	IO(B)
W2	IO(H)	AA12	V _{CCIO(A)}	AB20	NC	AD2	PLL _{OUT} (2)	AE10	IO(A)	AF18	IO(B)
W3	NC	AA13	GND	AB21	IO(B)	AD3	PLL _{RST} (3)	AE11	IO(A)	AF19	IOCTRL(B)
W4	NC	AA14	V _{CCIO(B)}	AB22	GNDPLL(2)	AD4	NC	AE12	CLK(0)	AF20	IOCTRL(B)
W5	V _{CC}	AA15	V _{CC}	AB23	IO(B)	AD5	IO(A)	AE13	IO(B)	AF21	NC
W6	V _{CC}	AA16	V _{CC}	AB24	IO(C)	AD6	IO(A)	AE14	IO(B)	AF22	IO(B)
W21	V _{CCIO(C)}	AA17	GND	AB25	IO(C)	AD7	IO(A)	AE15	NC	AF23	IO(B)
W22	NC	AA18	V _{CCIO(B)}	AB26	IO(C)	AD8	IOCTRL(A)	AE16	IO(B)	AF24	IO(B)
W23	IO(C)	AA19	V _{CC}	AC1	NC	AD9	NC	AE17	IO(B)	AF25	IO(B)
W24	IO(C)	AA20	V _{CCIO(B)}	AC2	IO(A)	AD10	IO(A)	AE18	IO(B)	AF26	IO(B)

(Sheet 2 of 2)

516 PBGA Packaging Drawing

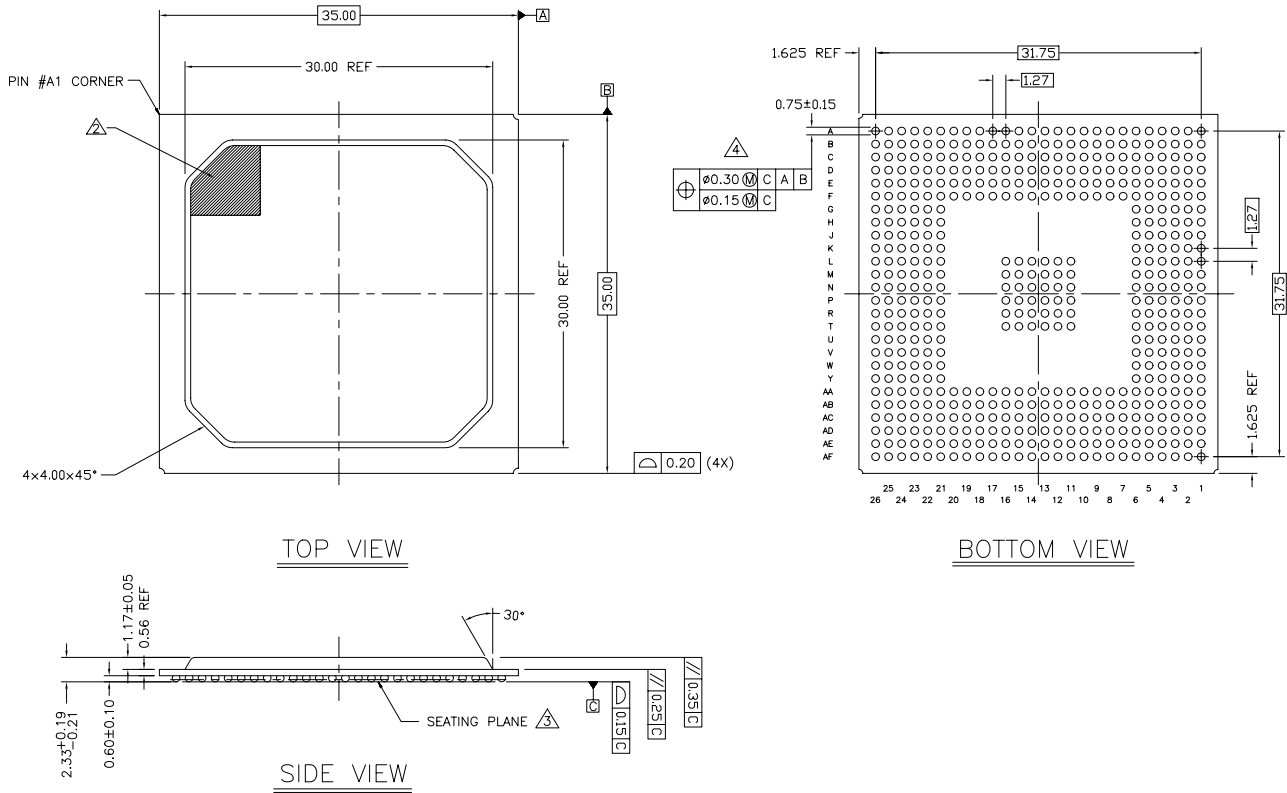


Figure 30: 516 PBGA Packaging Drawing

Ordering Information

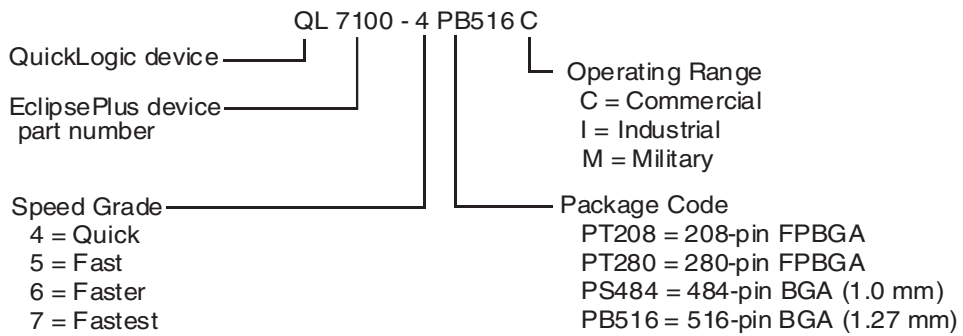


Figure 31: Ordering Information

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Revision History

Table 26: Revision History

Revision	Date	Comments
A	August 2002	Brian Faith, Judd Heape, Andreea Rotaru, Paul Micallef

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