Raytheon

RMBA19500A-58
PCS1900 2 Watt GaAs MMIC Power Amplifier

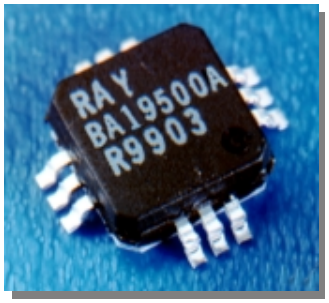
ADVANCED INFORMATION

Description

The RMBA19500A-58 is a high power, highly linear Power Amplifier. The circuit uses Raytheon's pHEMT process. It has been designed for use as a driver stage for PCS1900 base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for PCS operation. The device is matched for 50 ohms input impedance.

Features

- 2 Watt linear output power at 38 dBc ACPR1 for CDMA operation
- OIP3 ≥43 dBm at 27 and 30 dBm output
- Small Signal Gain of 28 dB
- Small outline SMD package



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Supply Voltage[1]	Vd	+10	Volts
Gate Supply Voltage (max absolute value)	Vg	-5	Volts
RF Input Power (from 50Ω source)	Pin	+5	dBm
Operating Case Temperature Range	Tc	-30 to +85	°C
Storage Temperature Range	Tstg	-40 to +100	°C

Electrical Characteristics[2]

Parameter	Min	Typ	Max	Unit
Frequency Range	1930		1990	MHz
Gain (small signal) Over 1930-1990 MHz	28	30		dB
Gain variation: Over frequency range		+/- 1.0		dB
Over temperature range		+/- 1.5		dB
Noise Figure		6		dB
P1dB Output	28	30		dBm
Output Power @ CDMA[3]	33			dBm

Parameter	Min	Typ	Max	Unit
PAE (At P1dB output power[4])		22		%
OIP3[5]	43	45		dBm
Drain Voltage (Vd)		7.0		Volts
Gate Voltages[6]	-1.5		-0.5	Volts
Quiescent current (Idq1,2, 3)[6]		185 445		mA
Thermal Resistance (Channel to Case)	Rjc	11		°C/W

Notes:

1. Only under quiescent conditions - no RF applied.
2. 50 ohm system, Vd = 7.0V, Tc = 25°C.
3. 9 channel forward line QPSK source; 1.23 Mbps modulation rate. ACPR1 measured at 885 KHz offset at a value of ≥38 dBc. CDMA waveform measured using the ratio of the average power within the 1.23 MHz channel and within a 30 KHz bandwidth at an 885 KHz offset.
4. Single tone at Bandcenter.
5. Ultra-linear OIP3 specifications are achieved for output power levels of 27 and 30 dBm per tone.
6. Quiescent currents can be adjusted to optimize the linearity of the amplifier for differing operation. Default biasing is optimized for PCS . Gate voltages are to be adjusted to achieve these quiescent currents.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

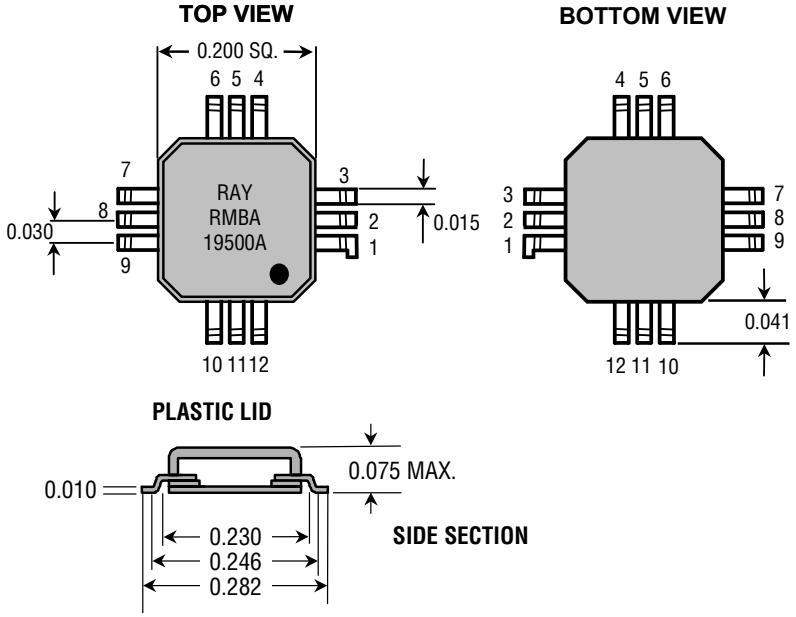
The following describes a procedure for evaluating the RMBA19500A-58, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for PCS1900 Base station or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. It should be noted that RMBA19500A-58 requires external passive components for DC bias and RF output matching circuits. A recommended schematic circuit is shown in Figure 3. The gate biases for the three stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of figure 3. The following designations should be noted:

(1) Pin designations are as shown in figure 2.
(2) Vg1, Vg2, and Vg3 are the Gate Voltages (negative) applied at the pins of the package.
(3) Vgg1, 2, and Vgg3 are the negative supply voltages at the evaluation board terminals (Vg1 and Vg2 are tied together).
(4) Vd1, Vd2, and Vd3 are the Drain Voltages (positive) applied at the pins of the package.
(5) Vdd is the positive supply voltage at the evaluation board terminal (Vd1, Vd2, and Vd3 are tied together).

Note: The base of the package must be soldered on to a heat sink for proper operation.

Figure 1
Package Outline and Pin Designations

Dimensions in inches



Pin#	Description
1	RF Out &Vd3
2	RF Out &Vd3
3	RF Out &Vd3
4	Vd1
5	GND
6	Vg1
7	RF In
8	GND
9	Vg2
10	Vd2
11	GND
12	Vg3
13	GND

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Figure 2
Functional Block Diagram

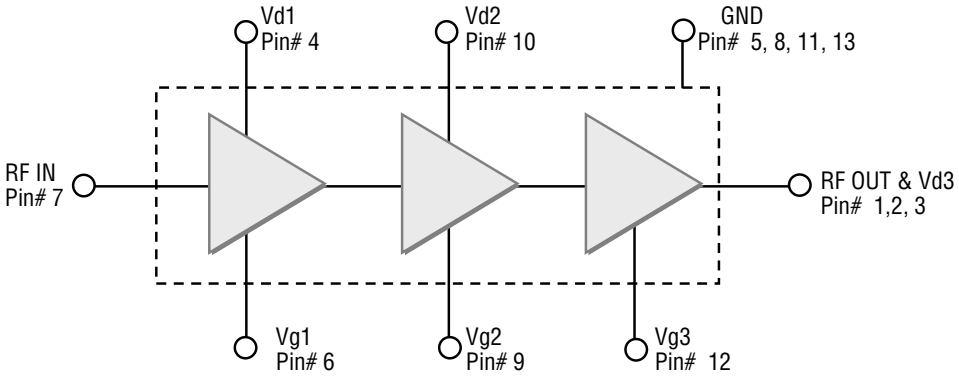

Figure 3
Schematic of Application Circuit showing external components

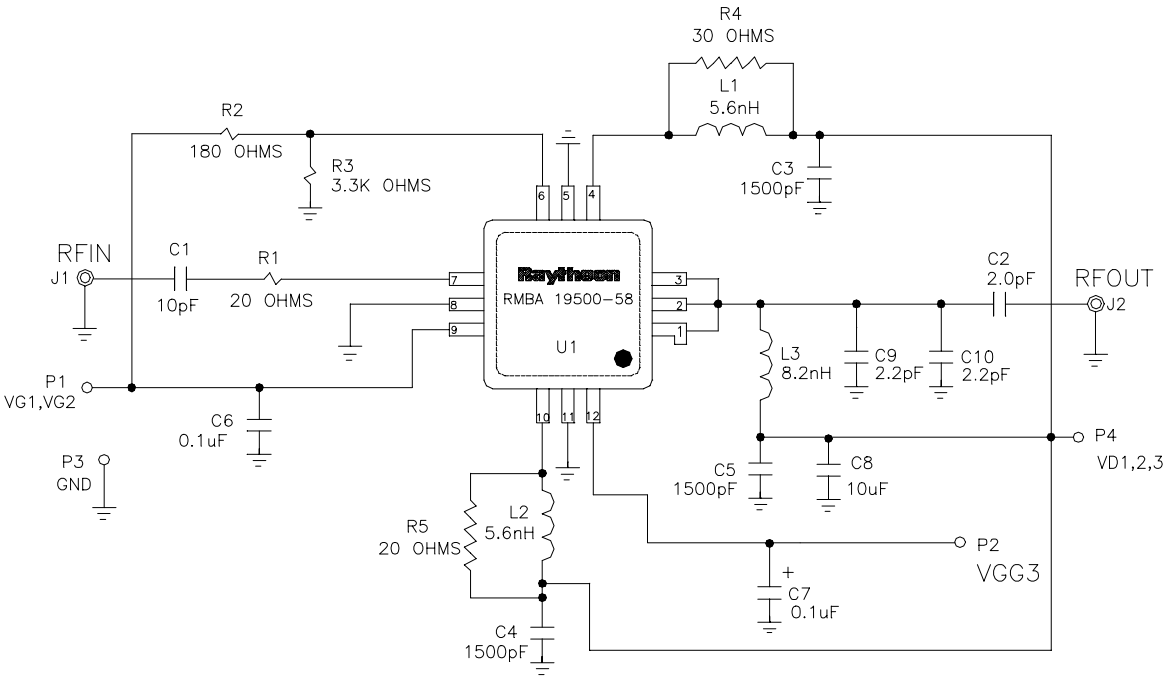

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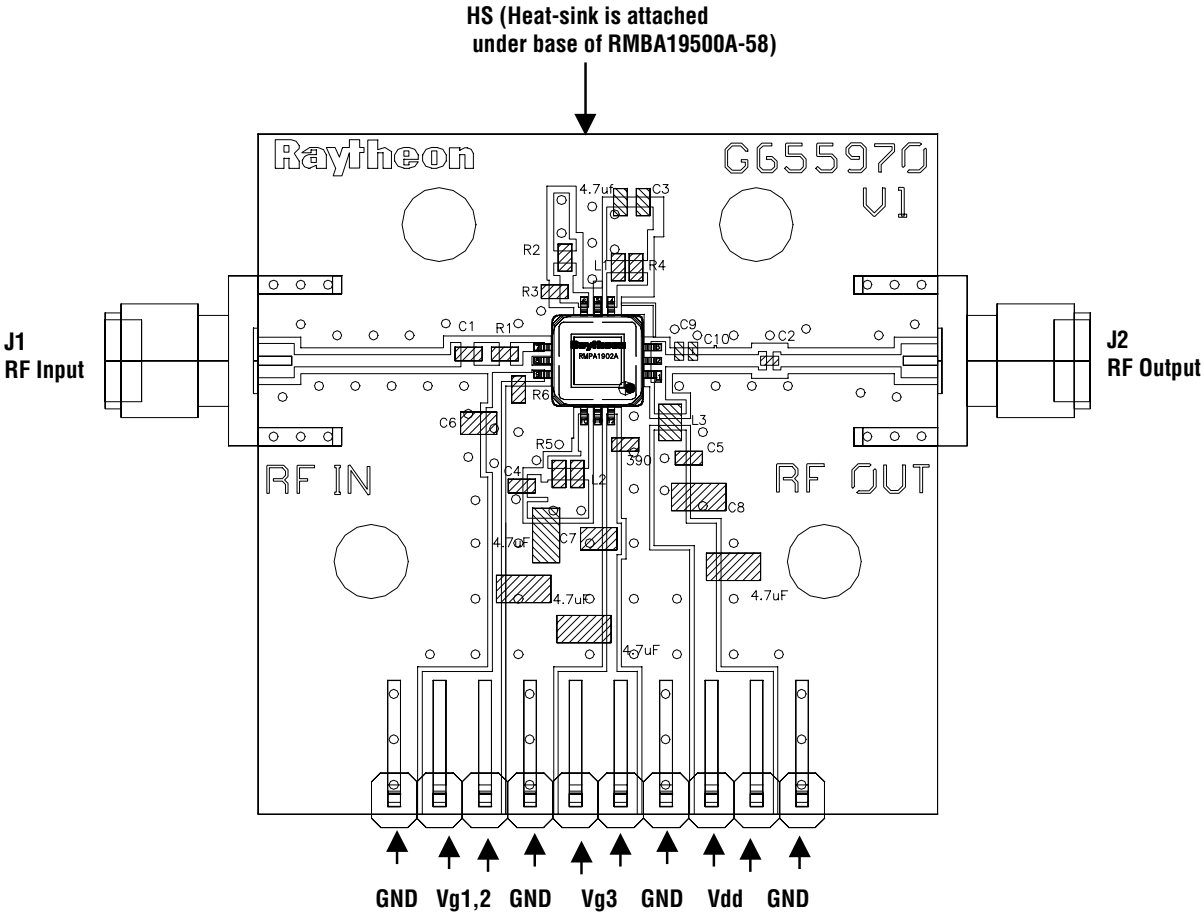
Figure 4
Layout of Test Evaluation Board (RMBA19500A-58-TB)



Test Procedure
for the evaluation board (RMBA19500A-58-TB)

CAUTION: LOSS OF GATE VOLTAGES (Vg1, Vg2, Vg3) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA19500A.)

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies. Set Vgg1, 2 and Vgg3 to -4V (pinch-off).

Step 3: Slowly apply drain supply voltages of +5 V to the board terminal Vdd ensuring that there is no short.

Step 4: Adjust Vgg3 up from -3V until the drain current (with no RF applied) increases to Idq3 as per supplied result sheet. Then adjust Vgg1, 2 until the total drain current becomes equal to the sum of Idq1, 2 and Idq3.

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.

Step 6: Follow turn-off sequence of:

(i) Turn off RF Input Power

(ii) Turn down and off drain voltage Vdd.

(iii) Turn down and off gate voltages Vgg1, 2 and Vgg3.

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Parts List
for Test Evaluation Board (RMBA19500A-58-TB, G654188/G654942)

Part	Value	EIA Size	Vendor(s)
L1, L2	5.6 nH	.06" x .03"	Toko (LL1608-F5N6)
L3	8.2 nH	.08" x .05"	Coilcraft (0805HT-8N2TKBC)
C1	10 pF	.06" x .03"	Murata (GRM39COG100J050AD)
C2	2.2 pF	.06" x .03"	Murata (GRM39COG2R2J050BD)
C3, C4, C5	1500 pF	.06" x .03"	Murata (GRM39Y5V152Z50V)
C10, C9	2.2 pF	.06" x .03"	Murata (GRM39COG2R2J050BD)
C8	10.0 uF	.12"x.06"	TDK (CC1206JX5R106M)
C6,C7	0.1uF		Murata (GRM39Y5V104Z)
R1-R5	20 Ohms	.06"x .03"	IMS (RCI-0603-20R0J)
R2	180 Ohms	.06"x .03"	IMS (RCI-0603-1800J)
R3	3.3K Ohms	.06"x .03"	IMS (RCI-0603-3301J)
R4	30 Ohms	.06"x .03"	IMS (RCI-0603-30R0J)
U1	RMBA19500A-58	.31" x .41	Raytheon, G654466/G653367
HS	Heatsink		Raytheon, G655548
P1-P5	Terminals		Samtec (TSW-102-09-T-S-RE)
J1, J2	SMA Connectors		E.F. Johnson (142-0701-841)
Board	FR4		Raytheon Dwg# G654187/G654941

Thermal Considerations
for Heat Sinking the RMBA 19500A-58

PWB must be prepared with either an embedded copper slug in the board where the package is to be mounted or a heat sink should be attached to the backside of PWB where the package is to be mounted on the front side. Both the slug or the heat sink should be made of a highly conductive (electrical and thermal) material such as copper or aluminum. The slug should be at least of the same thickness as PWB. In case of heat sink, a small pedestal should protrude through a hole in the PWB where the package bottom is directly soldered. In either configuration, the top surface of the slug or the pedestal should be made coplanar with the package lead mounting plane i.e., the top surface of PWB.

Use Sn/Pb (67/37) solder (or Sn/Pn/Ag 62/36/2 solder) at 2200C for 20 seconds or less. The package bottom should be firmly soldered to the slug or the pedestal while the pins are soldered to the respective pads on the front side of the PWB without causing any stress on the pins. Remove flux completely if used for soldering.

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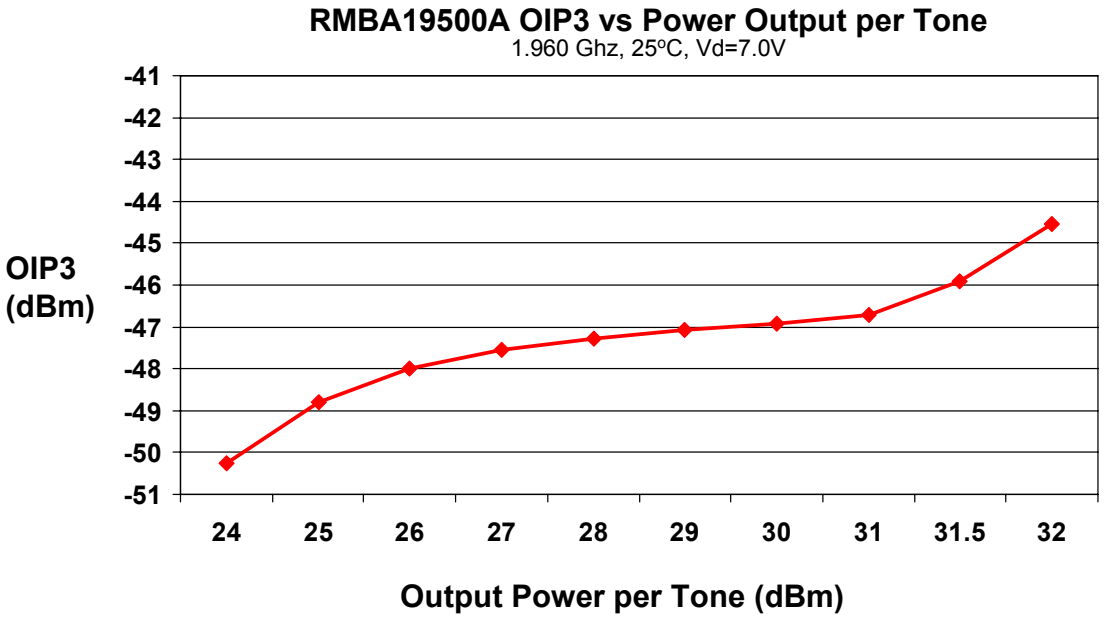
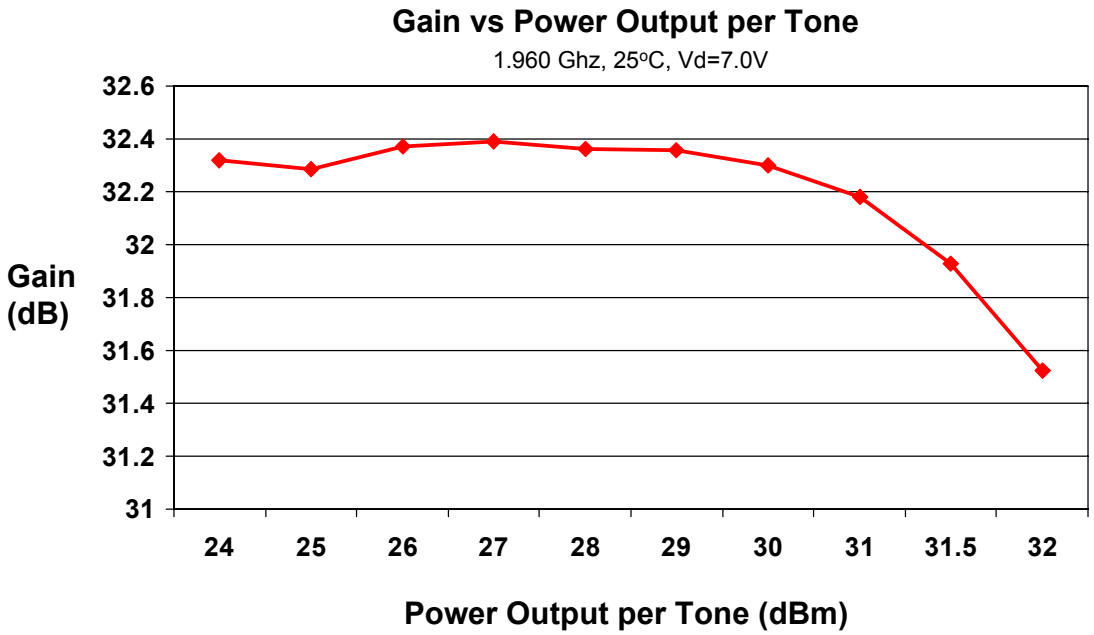
Performance Data





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