Raytheon

RMDA00400
OC-768 Modulator Driver MMIC

ADVANCED INFORMATION

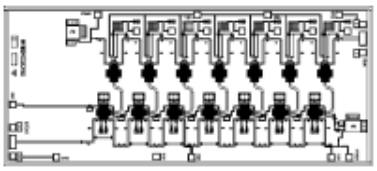
Description

The Raytheon RMDA00400 is a medium power broadband amplifier MMIC suitable as a driver for external optical modulators for OC-768 fiber optic systems. It is available in die form, and is manufactured using Raytheon's advanced 0.15µm pHEMT process.

Applications include Long haul, Medium haul and Metro fiber systems

Features

- DC-43 GHz bandwidth
- High gain: 10 dB typ
- Low group delay
- Low gain ripple.
- Psat = 19dBm typ
- Low power dissipation~ 1.4W
- Chip size 3.84 mm x 1.28 mm



Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units
Supply Voltage	Vd		+8.0		V
RF Input Power	Pin			18	dBm
Case Operating Temperature	Tc	-40		+85	°C
Storage Temperature	Tstg	-40		+100	°C

Electrical Characteristics1,2

Parameter	Min	Typ	Max	Unit
3 dB Bandwidth (small signal)		43		GHz
Gain		10		dB
Output Power (saturated)		19		dBm
Group Delay		±20		pS

Parameter	Min	Typ	Max	Unit
Input Return Loss		15		dB
Output Return Loss		10		dB
Quiescent Current		130		mA
Vd		8.0		V
Vg1		-0.3		V

Notes:

1. Off-chip decoupling and blocking capacitors required.
2. All parameters met at T = 25°C, Vd = 8.0V, IDQ= 130mA. Measured in 50 ohm system

Characteristic performance data and specifications are subject to change without notice.

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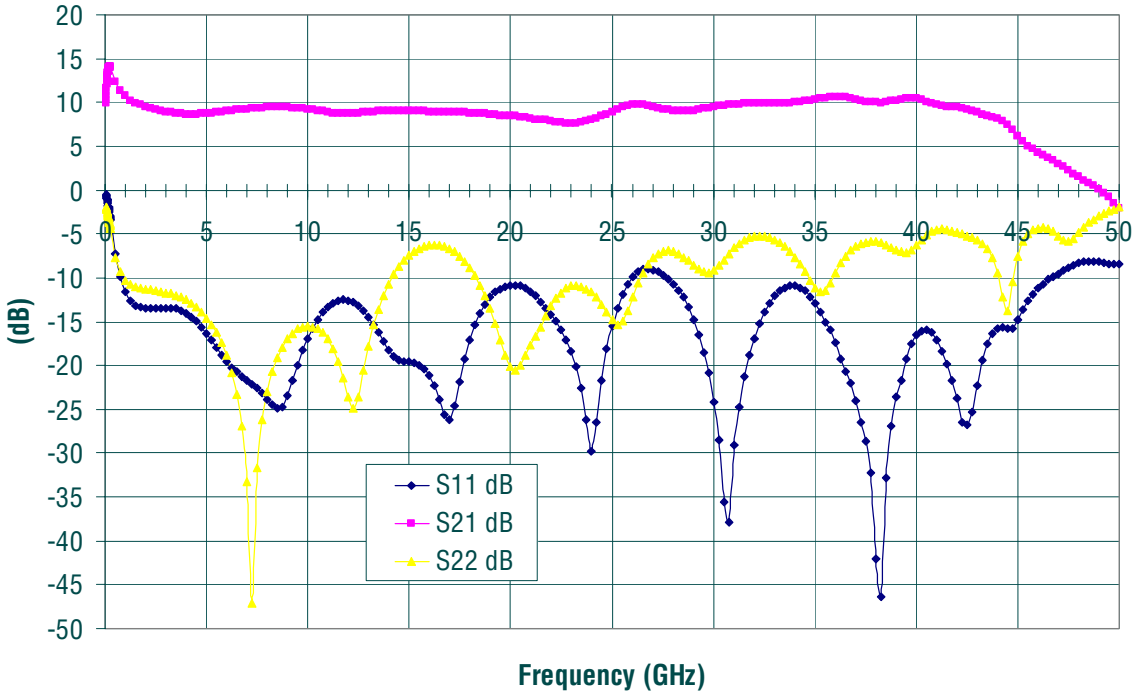
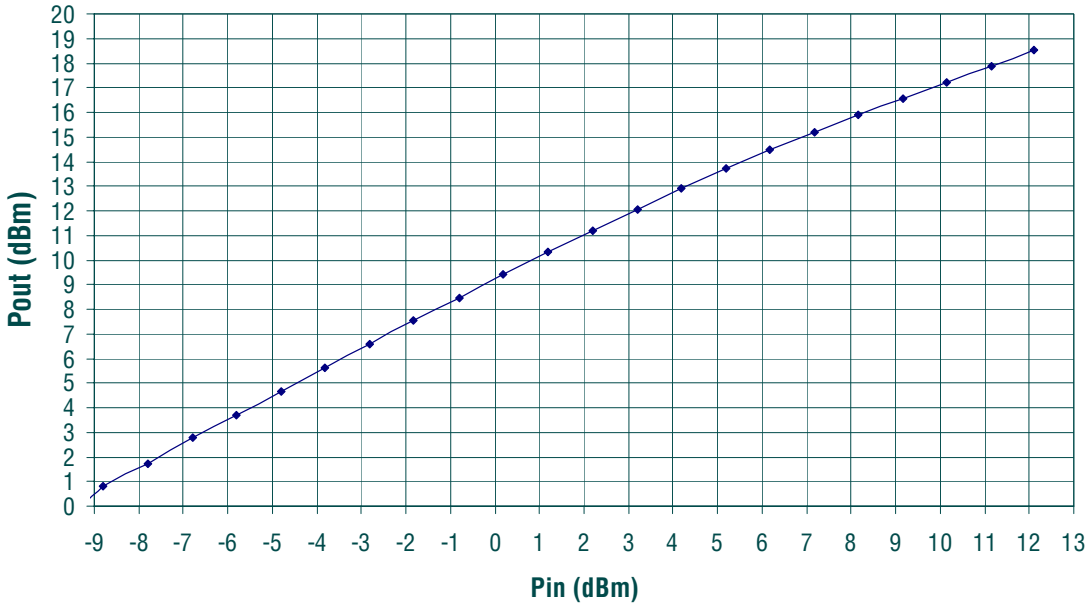
Performance Data

Small Signal Frequency Response
Vd= 8.0V, Idq= 130mA



Pin VS Pout at 30 GHz,
Vd=8.0V, Idq=130mA



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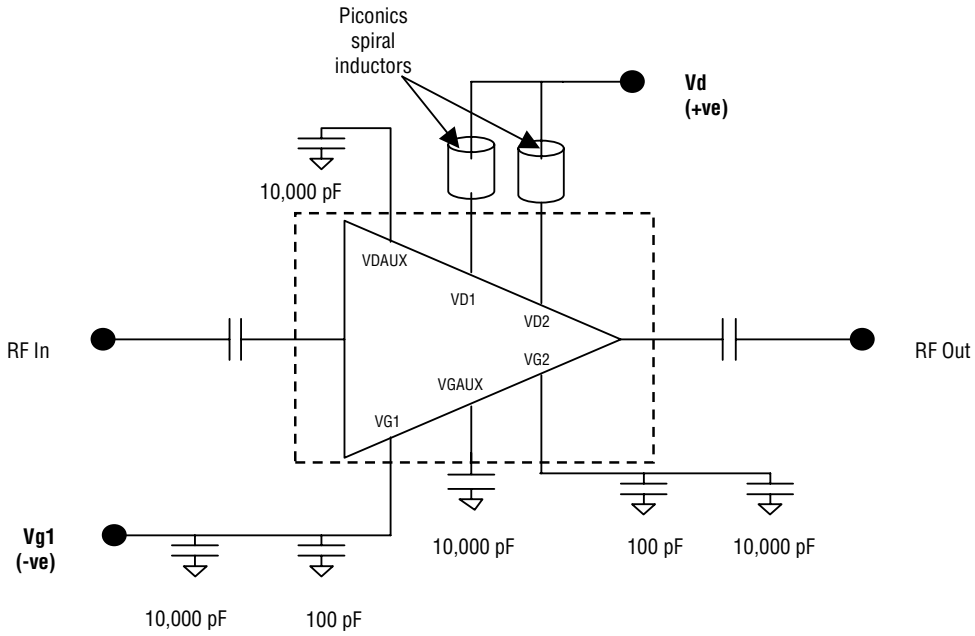
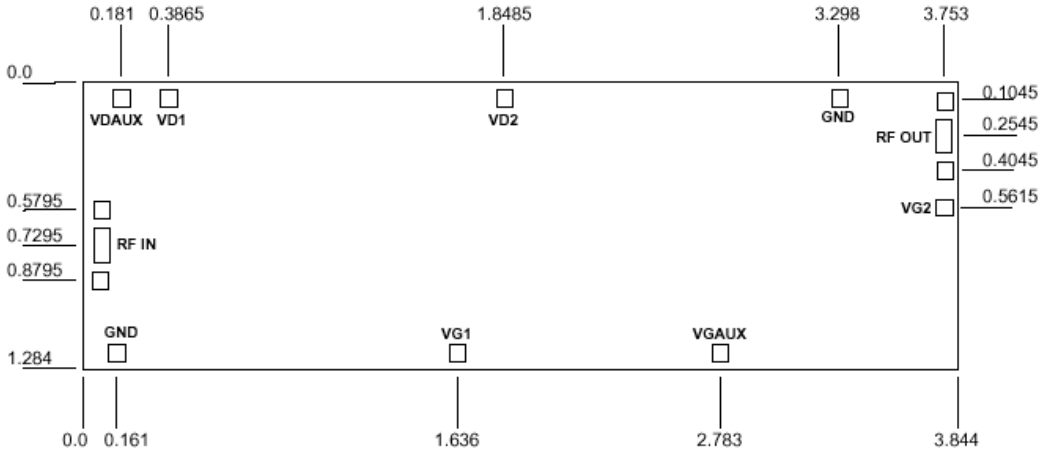
Recommended Application Schematic Circuit Diagram



Chip Layout and Bond Pad Locations

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Dimensions in mm



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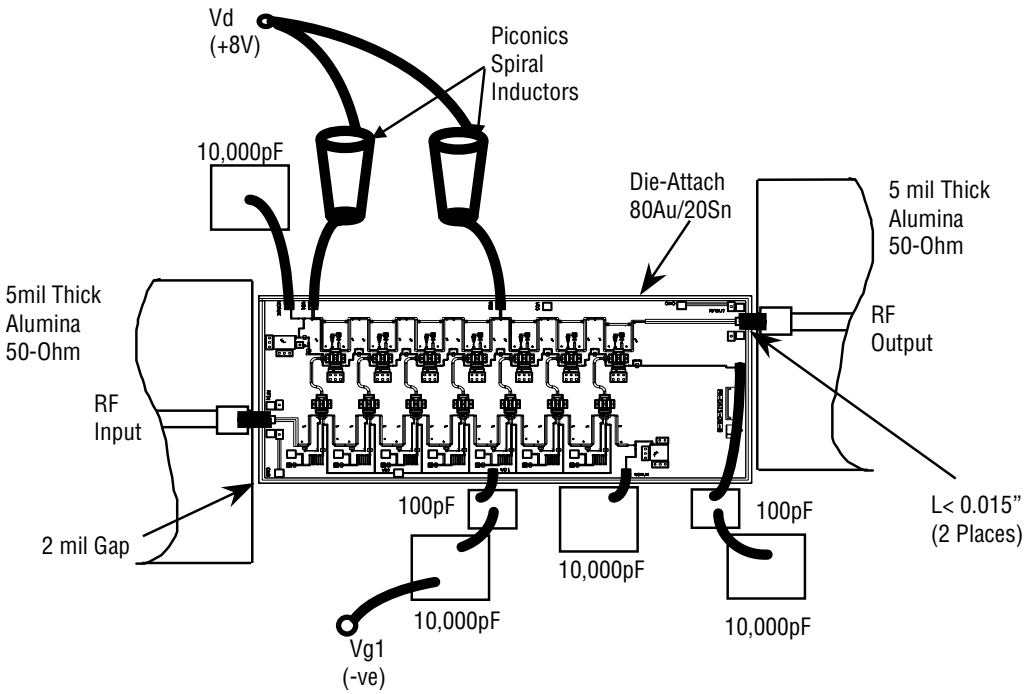
Recommended Assembly Diagram



Recommended Procedure for Biasing and Operation

CAUTION: THIS IS AN ESD SENSITIVE DEVICE. LOSS OF GATE VOLTAGE (VG1) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier.

Apply negative gate bias supply voltage of –1.0 V to Vg1.

Step 3: Apply positive drain bias supply voltage of +8.0 V to Vd, and monitor drain current Id.

Step 4: Adjust gate bias voltage Vg1 to set the quiescent current of Idq ~ 130 mA.

Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band. Adjust Vg1 for best gain flatness.

Note: When the device is under RF operation, the supply current Id will increase depending upon output power required.

Step 6: Follow turn-off sequence of:

(i) Turn off RF input power.
(ii) Turn down and off drain voltage (Vd).
(iv) Turn down and off gate bias voltage (Vg1).

Raytheon RF Components
362 Lowell Street
Andover, MA 01810

Worldwide Sales Representatives

North America

D&L Technical Sales
6139 S. Rural Road, #102
Tempe, AZ 85283
480-730-9553
fax: 480-730-9647
Nicholas Delvecchio, Jr.
dlarizona@aol.com

Hi-Peak Technical Sales
P.O. Box 6067
Amherst, NH 03031
866-230-5453
fax: 603-672-9228
sales@hi–peak.com

Spartech South
2115 Palm Bay Road, NE,
Suite 4
Palm Bay, FL 32904
321-727-8045
fax: 321-727-8086
Jim Morris
jim@spartech-south.com

TEQ Sales, Inc.
920 Davis Road, Suite 304
Elgin, IL 60123
847-742-3767
fax: 847-742-3947
Dennis Culpepper
dculpepper@teqsales.com

Cantec Representatives
8 Strathearn Ave, No. 18
Brampton, Ontario
Canada L6T 4L9
905-791-5922
fax: 905-791-7940
Dave Batten
cantec-ott@cantec-o.net

Steward Technology
6990 Village Pkwy #206
Dublin, CA 94568
925-833-7978
fax: 925-560-6522
John Steward
johnsteward1@msn.com

Europe

Sangus OY
Lunkintie 21,
90460 Oulunsalo
Finland
358-8-8251-100
fax: 358-8-8251-110
Juha Virtala
juha.virtala@sangus.fi

Sangus AB
Berghamnvagen 68
Box 5004
S–165 10 Hasselby
Sweden
Ronny Gustafson
468-0-380210
fax: 468-0-3720954

Globes Elektronik & Co.
Klarastrabe 12
74072 Heilbronn
Germany
49-7131-7810-0
fax: 49-7131-7810-20
Ulrich Blievernicht
hfwelt@globes.de

MTI Engineering Ltd.
Afek Industrial Park
Hamelacha 11
New Industrial Area
Rosh Hayin 48091
Israel
972-3-902-5555
fax: 972-3-902-5556
Adi Peleg
adi_p@mti-group.co.il

Sirces srl
Via C. Boncompagni, 3B
20139 Milano
Italy
3902-57404785
fax: 3902-57409243
Nicola Iacovino
nicola.iacovino@sirces.it

Asia

ITX Corporation
2–5, Kasumigaseki
3–Chome
Chiyoda–Ku
Tokyo 100-6014 Japan
81-3-4288-7073
fax: 81-3-4288-7243
Maekawa Ryosuke
maekawa.ryosuke@
itx–corp.co.jp

Sea Union
9F-1, Building A, No 19-3
San-Chung Road
Nankang Software Park
Taiwan, ROC
Taipei 115
02-2655-3989
fax: 02-2655-3918
Murphy Su
murphy@seaunionweb.com.tw

Worldwide Distribution

Headquarters
Avnet-MCS
6321 San Ignacio Drive
San Jose, CA 95119
408-360-4073
fax: 408-281-8802
Art Herbig
art.herbig@avnet.com

Belgium and Luxembourg
BFI Optilas
Cipalstraat
2440 GEEL
Belgium
32 14 570670
fax: 32 14 570679
sales.be@bfioptilas.avnet.com

United Kingdom
BFI Optilas
Burnt Ash Road
Aylesford, Kent
England
ME207XB
44 1622882467
fax: 44 1622882469
rfsales.uk@
bfioptilas.avnet.com

France
BFI Optilas
4 Allee du Cantal
Evry, Cedex
France
33 16079 5900
fax: 33 16079 8903
sales.fr@
bfioptilas.avnet.com

Holland
BFI Optilas
Chr. Huygensweg 17
2400 AJ ALPHEN AAN DEN
RIJN
The Netherlands
31 172 446060
fax: 33 172 443414
sales.nl@
bfioptilas.avnet.com

Spain
BFI Optilas
C/Isobel Colbrand, 6 – 4a
28050 Madrid
Spain
34 913588611
fax: 34 913589271
sales.es@
bfioptilas.avnet.com

Sales Office Headquarters

United States
(East Coast)
Raytheon
362 Lowell Street
Andover, MA 01810
978-684-8628
fax: 978-684-8646
Walter Shelmet
wshelmet@
rrfc.raytheon.com

United States
(West Coast)
Raytheon
362 Lowell Street
Andover, MA 01810
978-684-8919
fax: 978-684-8646
Rob Sinclair
robert_w_sinclair@
rrfc.raytheon.com

Europe
Raytheon
AM Teckenberg 53
40883 Ratingen
Germany
49-2102-706-155
fax: 49-2102-706-156
Peter Hales
peter_j_hales@
raytheon.com

Asia
Raytheon
Room 601, Gook Je Ctr. Bldg
191 Hangang Ro 2-GA
Yongsan-Gu, Seoul,
Korea 140-702
82-2-796-5797
fax: 82-2-796-5790
T.G. Lee
tg_lee@
rrfc.raytheon.com

Customer Support

978-684-8900 fax: 978-684-5452 customer_support@rrfc.raytheon.com

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