Raytheon

RMM5030
9-10 GHz GaAs Power Amplifier MMIC

PRODUCT INFORMATION

Description

The Raytheon RMM5030 is an X-band two-stage dual channel GaAs MMIC power amplifier operating over 9-10 GHz which can be configured to provide either 34 dBm of minimum saturated single channel power into 50 ohms or 37 dBm combined. This unique chip configuration incorporates a pair of parallel channels each containing two reactively matched stages consisting of 2x1.4 mm FETs driving 4x2.0 mm FETs for a total FET periphery of 21.6 mm. Either channel can be operated as an independent amplifier in a 50 ohm system to provide 34 dBm power output with the adjacent channel retained as a spare. Alternatively the two channels can be combined to provide 37 dBm power output. In this case an external transformer or combiner is required for operation in a 50 ohm system. The FETs are fabricated using Raytheon's proven 0.5 mm Ti/Pt/Au gate MESFET process. The RMM5030 is ideally suited for power stage applications where limited space is available. It also allows the user to bias stages individually to customize performance and maximize amplifier efficiency.

Features

- 37.8 dBm typical power into 25 Ω @ 2 dB compression
- Power added efficiency is greater than 20%
- 14 dB small signal gain
- Separate stage biasing to maximize efficiency
- Input match VSWR is less than 2.0:1
- Via hole grounding
- Chip Size: 223 mils x 213 mils x 4 mils

Performance Characteristics

Parameter	Min	Typ	Max	Unit
RF Performance Specifications[1]				
Frequency Range	9	-	10	GHz
RF Output Power @ -1 dBc	35	37.0		dBm
RF Output Power @ -2 dBc	36	37.8	-	dBm
Small Signal Gain	13	14.0	-	dB

Parameter	Min	Typ	Max	Unit
DC FET Performance Specifications[2]				
Saturation Current (Vgs = 0V)	-	7560	9072	mA
Transconductance (-1V < Vgs < 0V)	-	3456	-	mS
Pinchoff Voltage	-5.0	-3.2	-2.0	Volts
Thermal Resistance:				
Thermal Resistance @ Tbc=80°C (Tbc = Temp. @ back of chip)		3.7		°C/W

Note:

1. Bias Conditions: Vds = 7 Volts, Ids = Idss/2, and all specifications guaranteed at 25 °C.
2. Bias Conditions: Vds = 2.5V, and all specifications guaranteed at 25°C.

Application Notes

1. Devices must be solder mounted with 80/20 Au-Sn for proper heat sinking.
2. Input/output ports, when paralleled, are 25Ω. A coupler combiner or transformer is required to match to 50Ω for this configuration.
3. Electrical data is for both channels operating in parallel into 25Ω terminating impedances. Data is specified for CW operation. Under CW operation, power output and gain may be degraded by up to 0.5 dB depending on the effectiveness of heat sinking
4. DC biasing:
   a) First apply the gate bias, typically -1.5V to -2.0V is recommended. Next, increase the drain voltage to 5~7V
   b) For maximum output power, the drain voltage can be increased to 7V
   c) For maximum efficiency, use a drain voltage of 5V with a gate voltage of approximately -1.5V

Characteristic performance data and specifications are subject to change without notice.

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362 Lowell Street
Andover, MA 01810

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Figure 1
Bonding Pads

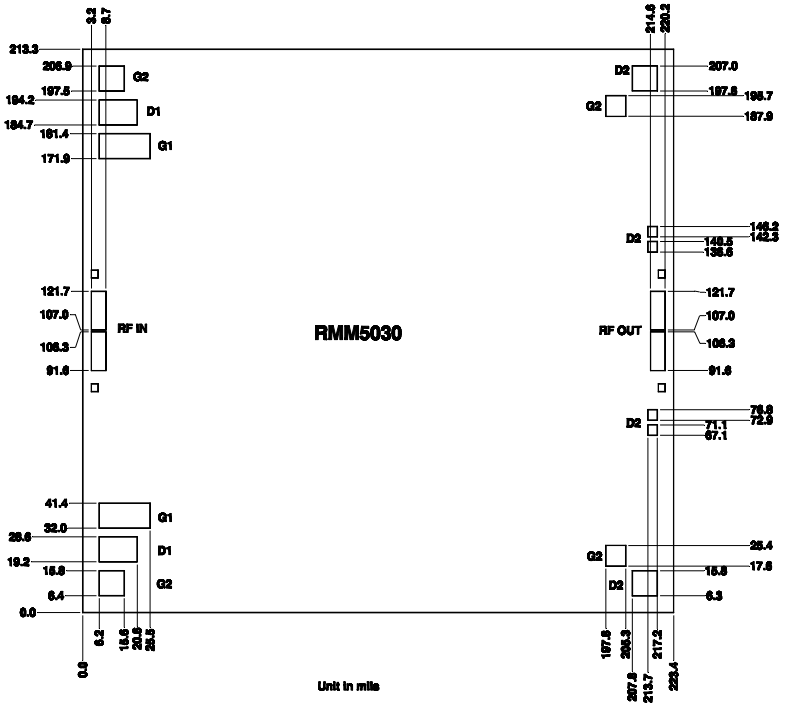
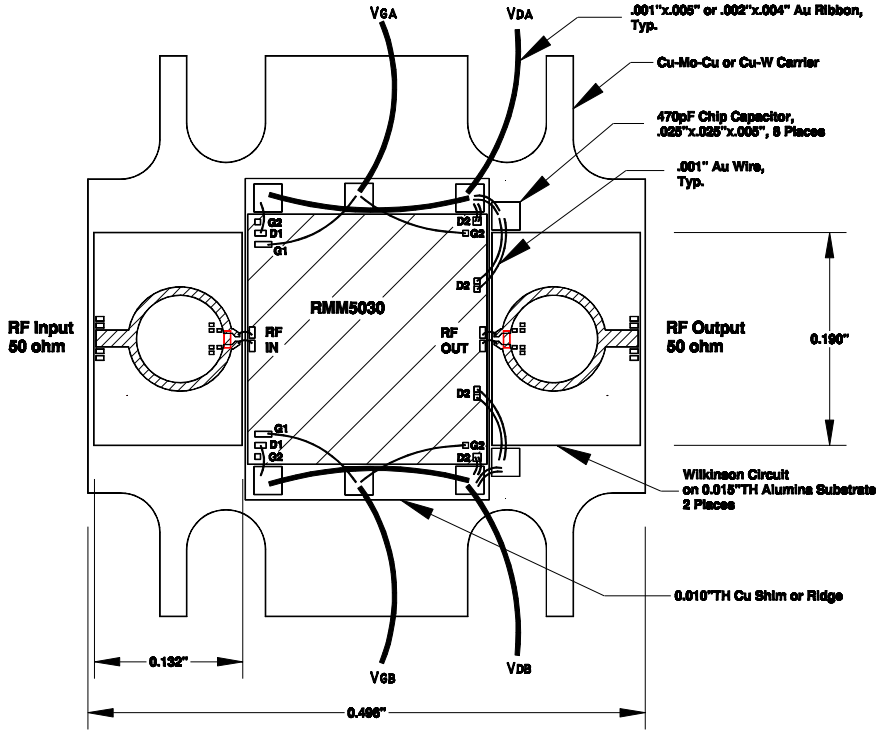


Figure 2
Example of
Wilkinson Power
Combiner Module



Notes:

1. Device is solder mounted with 80/20 Au/Sn onto Cu shim or ridge, which is in turn blazed to Cu-W or Cu-Mo-Cu carrier for proper heat sinking.
2. To bias up the device, first apply the gate bias, typically -1.5V to -2.0V is recommended. Next, increase the drain voltage to 5 ~ 7 volts. Finally readjust gate bias, VG, for proper drain current.

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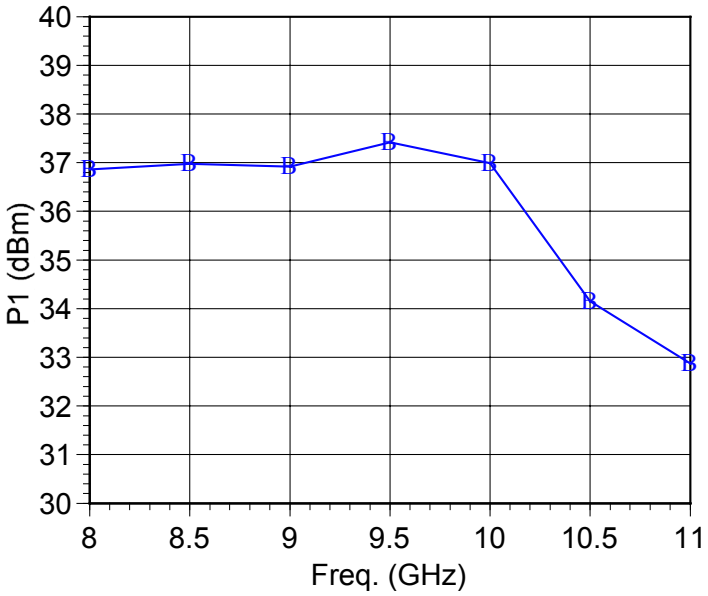
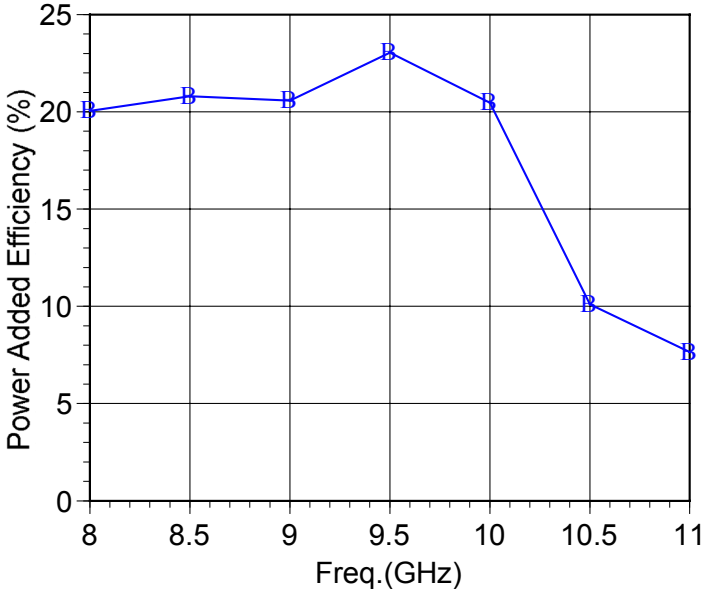
Performance Data
of Typical Wilkinson Combined CW

Combined CW Output, P1
Vd=7.0V, Idq=2.8A, Vg=1.13V



CW Power Added Efficiency @ P1
Vd=7.0V, Idq=2.8A, Vg=1.13V



The Id @ 1 dB compression increases to 3.5 A or thereabouts. The dc supply should be able to support the required current to achieve the above performance.

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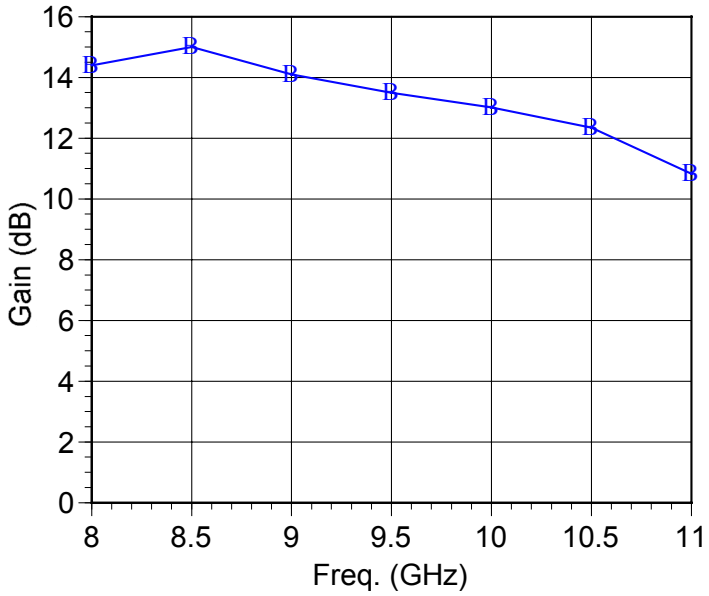
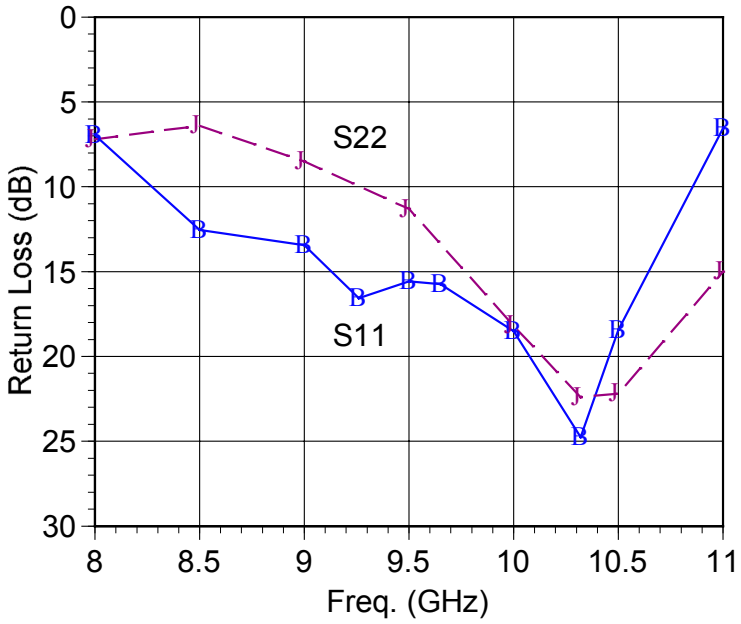
Performance Data
of Typical Wilkinson Combined CW

Combined Small Signal Gain, CW
Vd=7.0V, Idq=2.8mA, Vg=1.13V



Small Signal Return Loss
Vd=7.0V, Idq=2.8A, Vg=1.13V



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