Raytheon

RMPA1751-102
3V PCS CDMA Power Amplifier Module

ADVANCED INFORMATION

Description

The RMPA1751-102 is a small-outline, power amplifier module (PAM) for Korean-band CDMA Personal Communication System (PCS) and Wireless Local Loop (WLL) applications. ***Advanced DC power management provides an effective means to reduce current consumption during peak phone usage at backed-off RF power levels***. Analog or digital bias control enables the handset designer to optimize gain, linearity and power-added efficiency over a wide range of output powers, depending on the power-density profile of the wireless network. High power-added efficiency and excellent linearity are achieved using Raytheon's Heterojunction Bipolar Transistor (HBT) process.

Features

- ***Advanced DC power-management extends average phone-battery life!***
- Single positive-supply operation and power-down mode.
- 35% power-added efficiency at +29 dBm CDMA average output power.
- Compact LCC package: 6.0 x 6.0 x 1.5 mm^3.
- 50 ohm matched and DC blocked input/output

Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typical	Max	Units
Supply Voltage	Vcc		3.5	6	V
Reference Voltage	Vref	1.5	2.7	4.0	V
RF Input Power[2]	P_{in}		+1	+7	dBm
Load VSWR	V_{SWR}		1.2:1	10:1	
Case Operating Temperature	T_c	-40	+25	+110	°C
Storage Temperature	T_{stg}	-55	+25	+150	°C

Electrical Characteristics[3]

Parameter	Min	Typ	Max	Unit
Operating Frequency	1720		1780	MHz
Gain				
(Po=0 dBm)	21	24		dB
(Po=28 dBm)	25	27		dB
Linear Output Power	29			dBm
Power-Added Efficiency				
(Po=16 dBm)		6.0		%
(Po=28 dBm)	27	30		%
(Po=29 dBm)		33		%
ACPR (Offset ≥ 1.25 MHz)[4]		-49	-46	dBc
Noise Figure		5	6	dB
Noise Power (Po ≤ 29 dBm)			-135	dBm/Hz
Input VSWR (50Ω)		2.0:1	2.5:1	
Output VSWR (50Ω)		3.5:1		

Parameter	Min	Typ	Max	Unit
Stability (All spurious)[5]			-70	dBc
Harmonics (Po ≤ 29 dBm)				
2fo, 3fo, 4fo		-30		dBc
Quiescent Current				
(Vref=2.7V)	60	80	100	mA
(Vref=2.0V)		50		mA
(Vref=1.7V)		35		mA
Power Shutdown Current[6]		2	10	uA
Vcc	3.0	3.5	4.5	V
Vref	1.7	2.7	3.2	V
Iref		13		mA
Case Operating Temperature	-30		+85	°C

Notes:
1. No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.
2. Typical RF input power for CDMA Pout=+28 dBm.
3. All parameters met at Tc =+25°C, Vcc =+3.5V, Vref=+2.7V, f=1750 MHz and load VSWR ≤ 1.2:1.
4. Po ≤ 28 dBm at Vcc=3.5V; CDMA Waveform measured using the ratio of average power within a 1.23 MHz channel to average power within a 30 kHz bandwidth at + 1.25 MHz offset.
5. Load VSWR ≤ 6:1, all phase angles.
6. No applied RF signal. Vcc=+3.5V nominal, Vref=+0.2V maximum.

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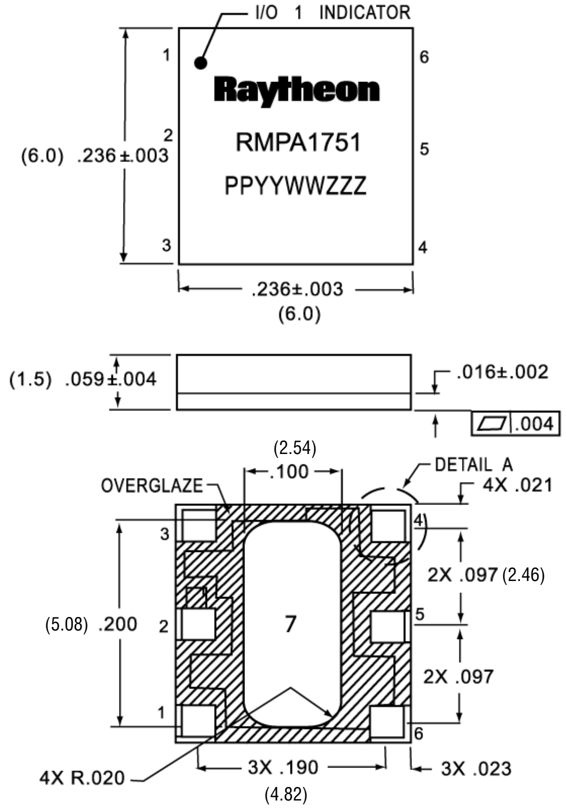
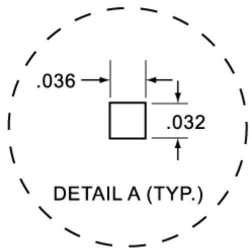
Figure 1
Package Outline and Pin Designations

Dimensions in inches (mm)



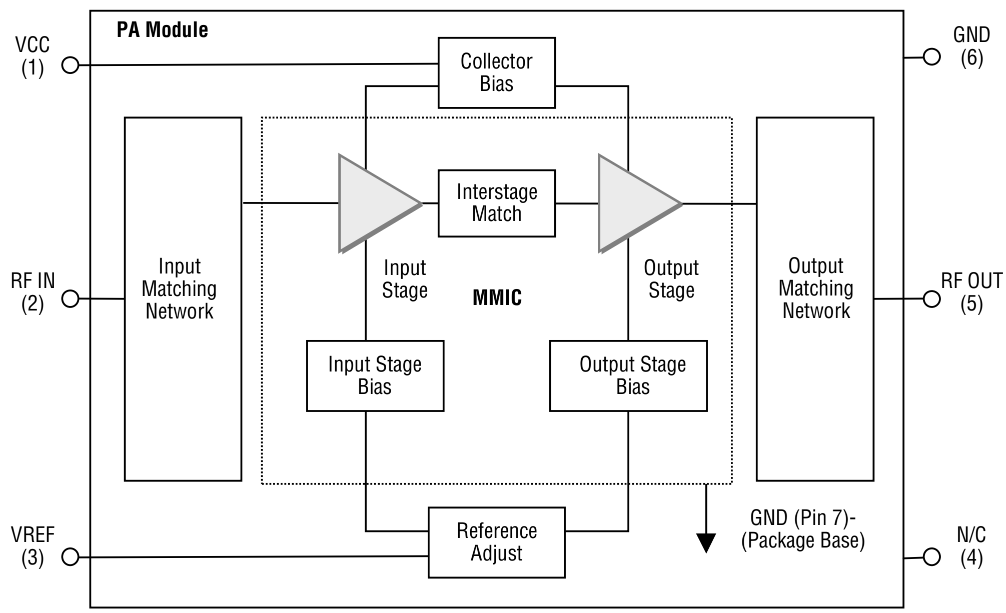


Pin #	Description
1	Vcc
2	RF In
3	VREF
4	N/C
5	RF Out
6	GND
7	GND

Figure 2
Functional Block Diagram

VCC=3.5V (nom)
VREF=2.7V (nom)
1720-1780 MHz
50 Ohms I/O

(Topside View)



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Evaluation Board Instructions

With device marking oriented right side up, RF IN is on the left and RF OUT is on the right.

Blue wire is collector DC voltage input (pin 1). VCC= +3.5V nominal.

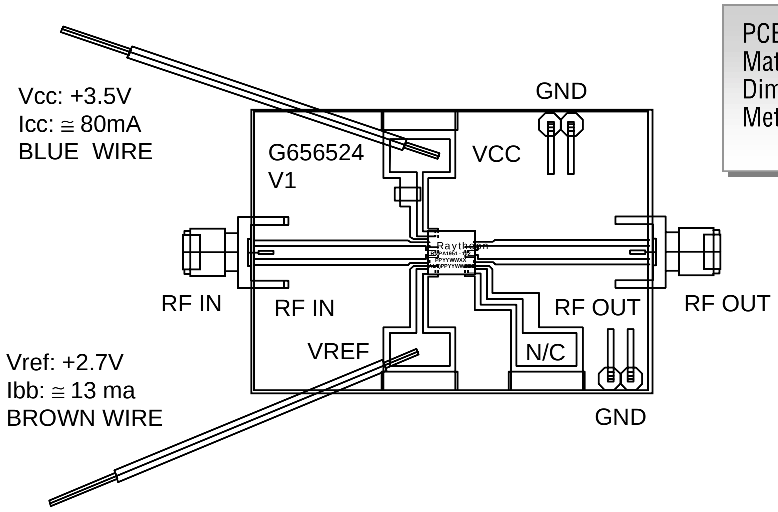
Brown wire is reference DC voltage input (pin 3). Vref=+ 2.7V nominal to obtain Iccq= 80mA. Operation at lower or higher quiescent currents can be achieved by decreasing or increasing Vref voltage relative to +2.7V.

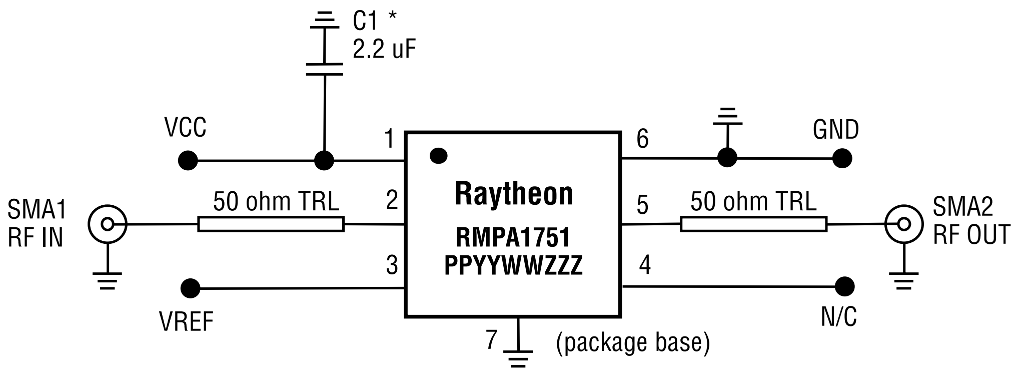
First apply +3.5V to the collector supply (blue wire). Next apply +2.7V to the reference supply to brown wire. Quiescent collector current with no RF applied will be about 80 mA. Reference supply current with or without RF applied will be about 13 mA. When turning amplifier off, reverse power supply sequence.

Apply -20dBm RF input power at Korean PCS frequency (1720 -1780MHz). After making any initial small signal measurements at this drive level, input power may be increased up to a maximum of +6dBm for large signal, single-tone or digital CDMA measurements. Do not exceed +6dBm input power.

Figure 3
Evaluation Board
Layout and Schematic

PCB Specifications:
Material: Rogers RO4003
Dimensions: 2.0”x1.5”x0.032”
Metallization: 1/2 OZ Copper Cladding





* Minimum VCC bypass capacitance recommended for best RF performance.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

◆ **Precautions to Avoid Permanent Device Damage:**

– Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.

– Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.

– Static Sensitivity: Follow ESD precautions to protect against ESD damage:

- A properly grounded static-dissipative surface on which to place devices.
- Static-dissipative floor or mat.
- A properly grounded conductive wrist strap for each person to wear while handling devices.

– General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.

– Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

◆ **Device Usage:** Raytheon recommends the following procedures prior to assembly.

– Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.

– Assemble the dry-baked devices within 7 days of removal from the oven.

– During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C

– If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

◆ **Solder Materials & Temperature Profile:** Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

– **Reflow Profile**

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

◆ **Solder Joint Characteristics:** Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

◆ **Rework Considerations:** Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

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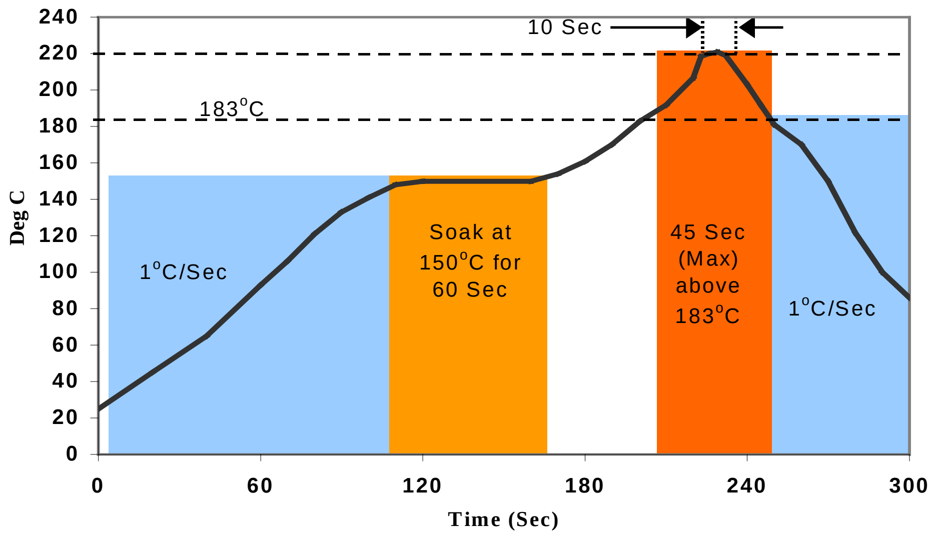
Figure 4

Recommended Solder Reflow Profile



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Performance Data
Figure 5

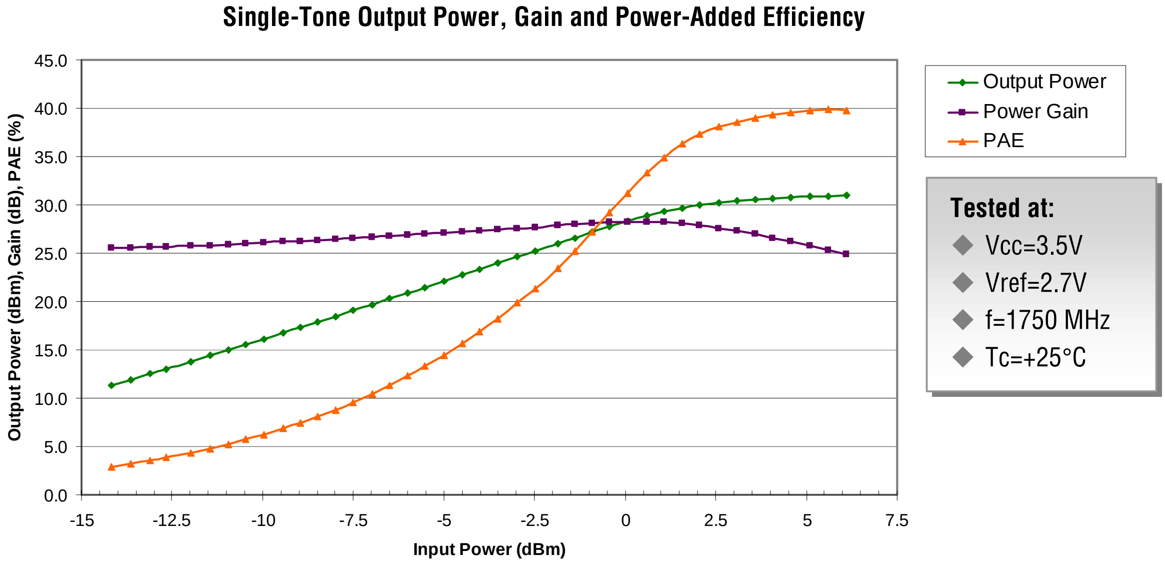

Figure 6

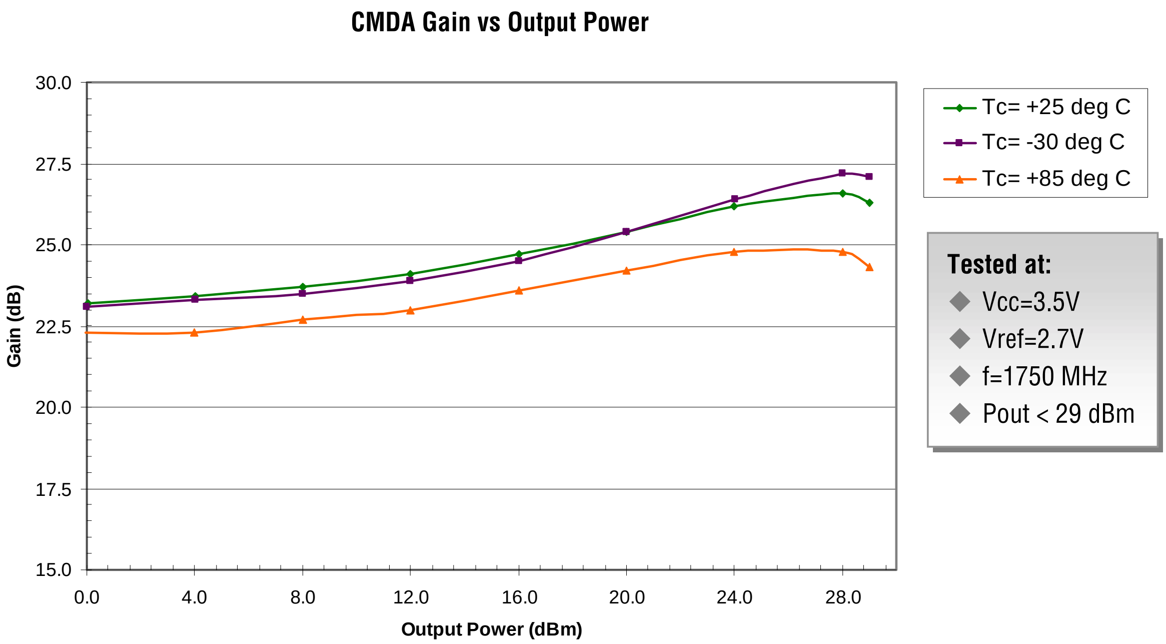

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Figure 7

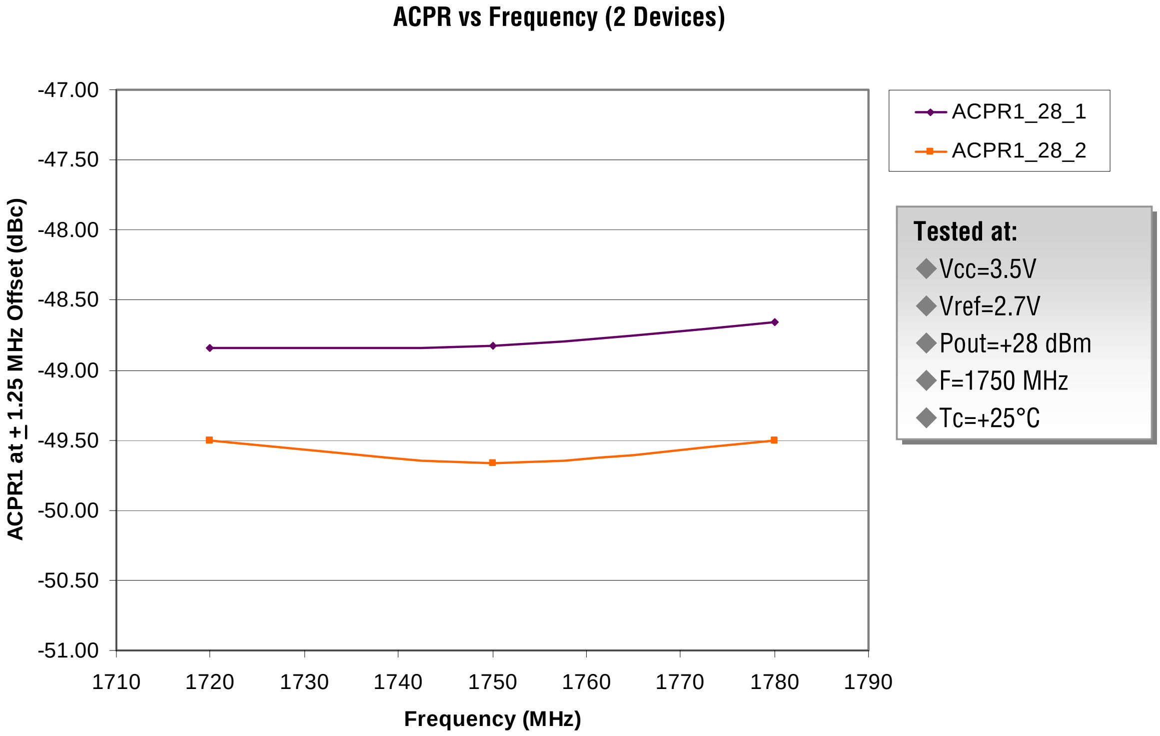

Figure 8

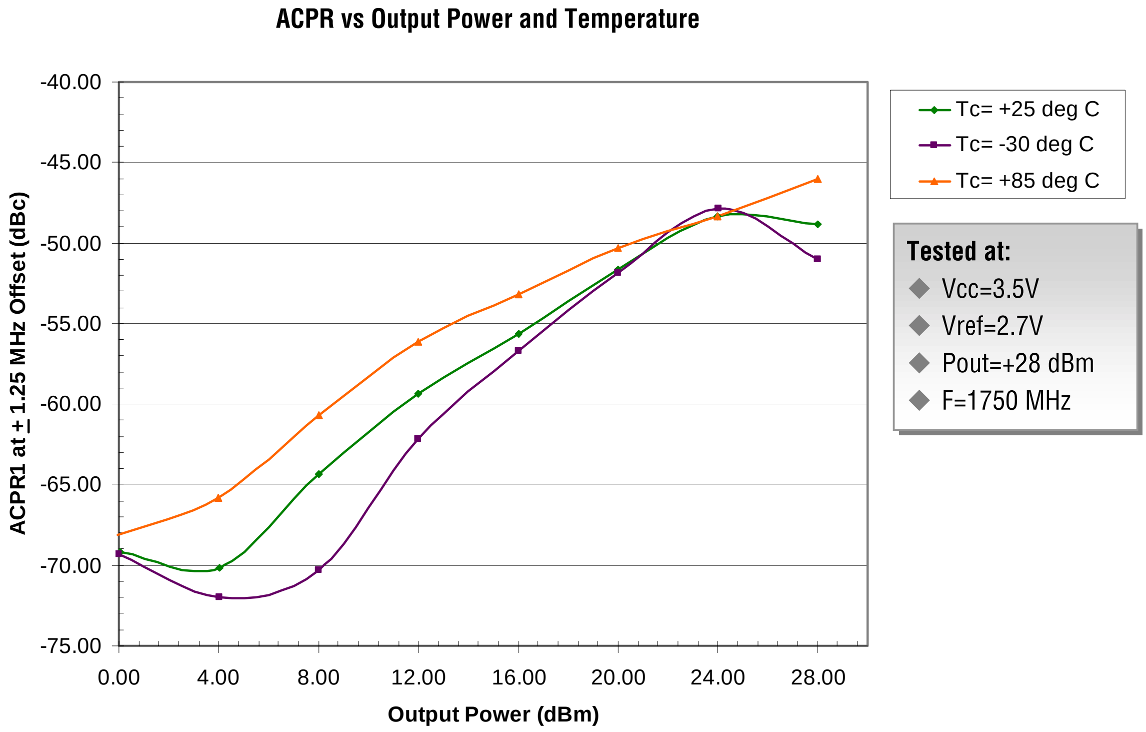

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Figure 9

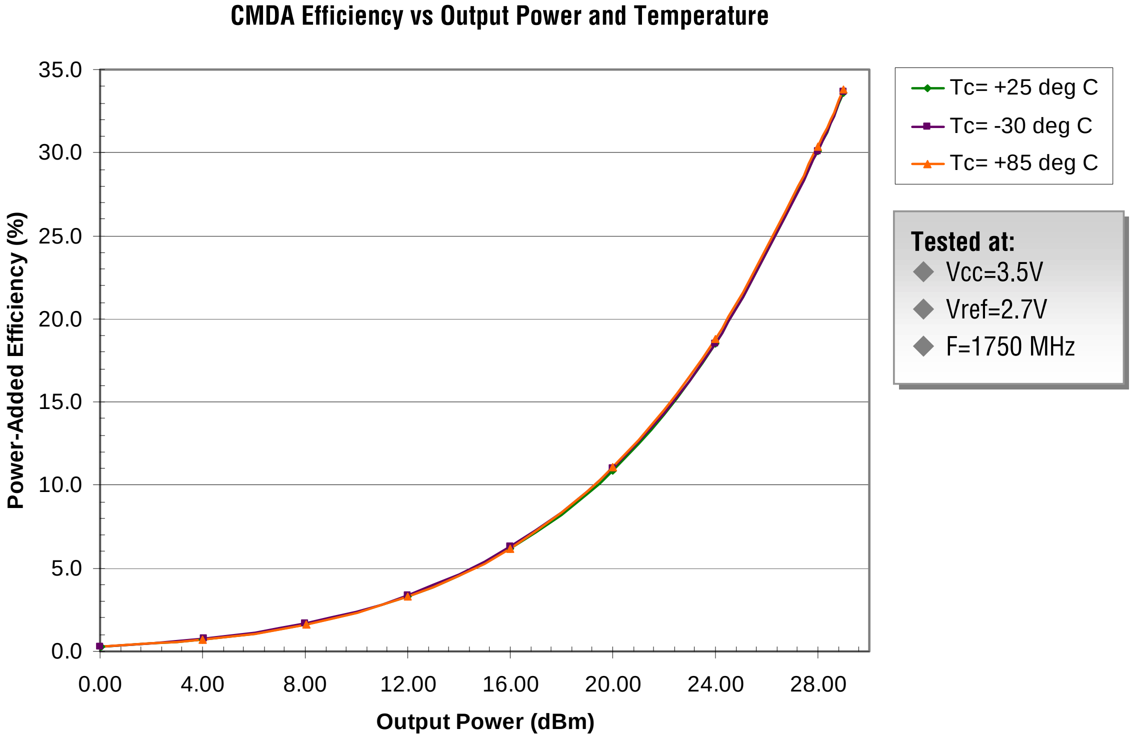
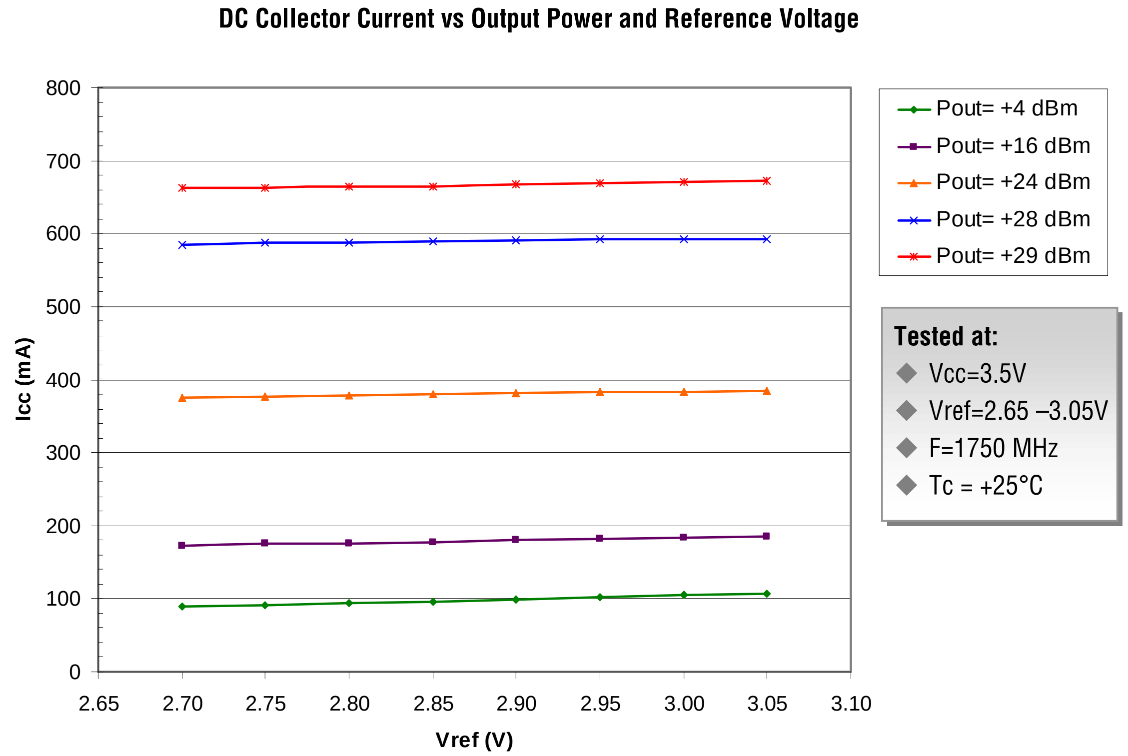


Figure 10



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DC Power Management
for Reduced-Power Operating Modes

Many Cellular/PCS handsets can benefit from gain control and DC power management to optimize transmitter performance while operating at backed-off output power levels. Oftentimes, cellular systems will operate at 10-20 dB back-off from maximum-rated linear power and peak power-added efficiency. The ability to reduce current consumption under these conditions, without sacrificing linearity, is critical to extending battery life in next-generation handheld phones.

The RMPA1751-102 PA offers the ability to lower quiescent current by more than 60 percent and small-signal gain by up to 10 dB using a single control voltage (Vref). Even with the amplifier biased for lowest current consumption, high linearity is maintained over the full operating temperature range and at output power levels up to +16 dBm. Bias and gain control through Vref provides complete flexibility for the handset designer, allowing the user to define the operation by either an analog (continuously-variable) or digital (discrete-step) voltage input. As an example, reducing the Vref voltage from 2.7V (nominal) to 1.7V (minimum) can lower PA current consumption by more than 20 percent at an output power of +16 dBm.

The following charts demonstrate analog and digital control techniques for minimizing DC power consumption at reduced RF output power levels. Figures 11 through 19 characterize analog control over a reference voltage (Vref) range of 1.7V to 2.7V. Quiescent current is reduced to less than 30 mA and small-signal gain is reduced by 10 dB at Vref=1.7V. Operating current at +16 dBm is also reduced by 20 percent, or 35 mA, at the lowest reference voltage. Figures 20 through 23 feature digital control using three discrete voltage levels (2.7V, 2.0V, 1.8V) to optimize linear PA performance over three output power ranges (< +4 dBm, +4 dBm to +16 dBm, >+16 dBm). Alternate output power ranges can be selected depending on the power-probability use in the cellular system.

DC Power Management
Application of Digital Control Technique

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Low-Power Range	P04			+4	dBm	Vref=1.8V typ
Current	Icc4			55	mA	
Gain	G4		13.5		dB	
Linearity	ACPR4		-50		dBc	
Mid-Power Range	P16	+4	+10	+16	dBm	Vref=2.0V typ
Current	Icc16			160	mA	
Gain	G16		19		dB	
Linearity	ACPR16		-50		dBc	
High-Power Range	P28	+16		+28	dBm	Vref=2.7V typ
Current	Icc28		560	660	mA	Pout=+28 dBm
Gain	G28		26		dB	
Linearity	ACPR28		-50		dBc	

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Figure 11

Enhanced PAE vs Reference Voltage at Pout=+16 dBm (Analog Control)

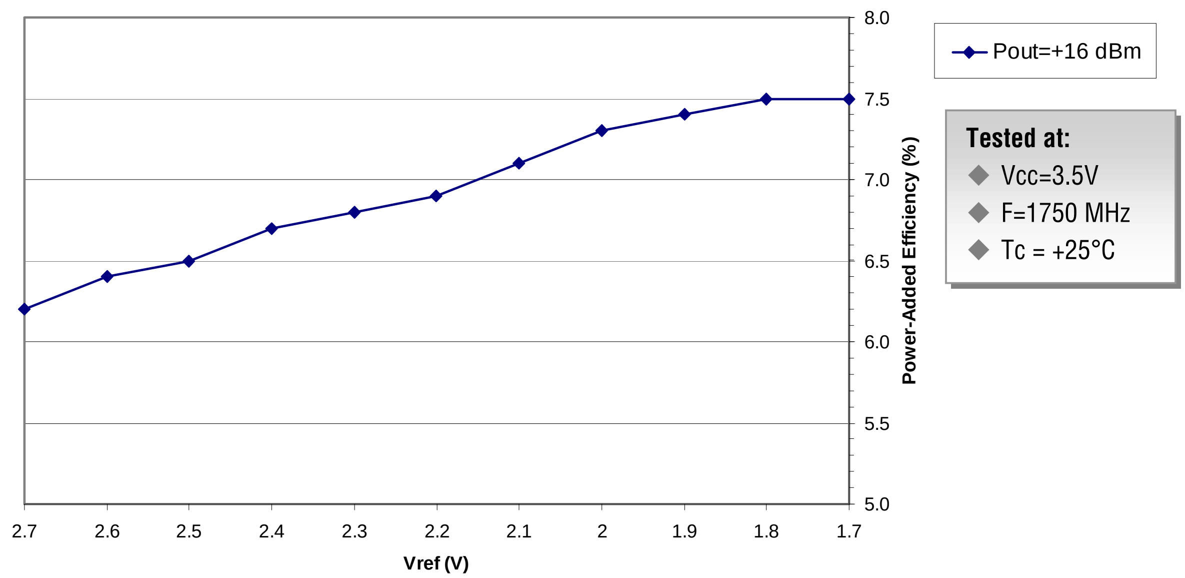

Figure 12

Total Quiescent Current vs Reference Voltage (Analog Control)

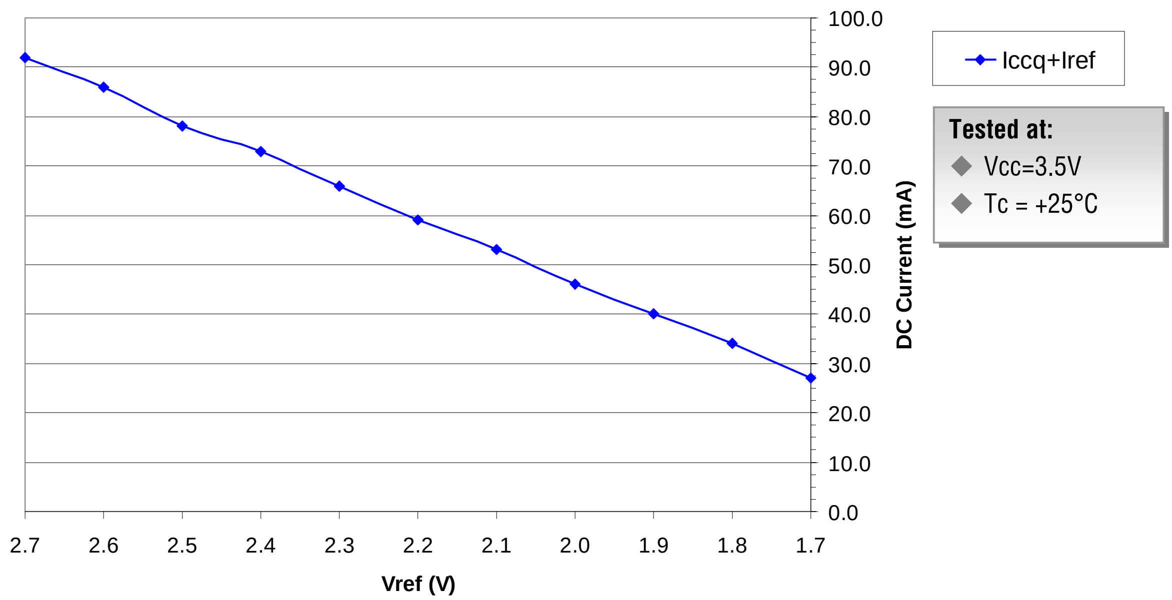

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Figure 13

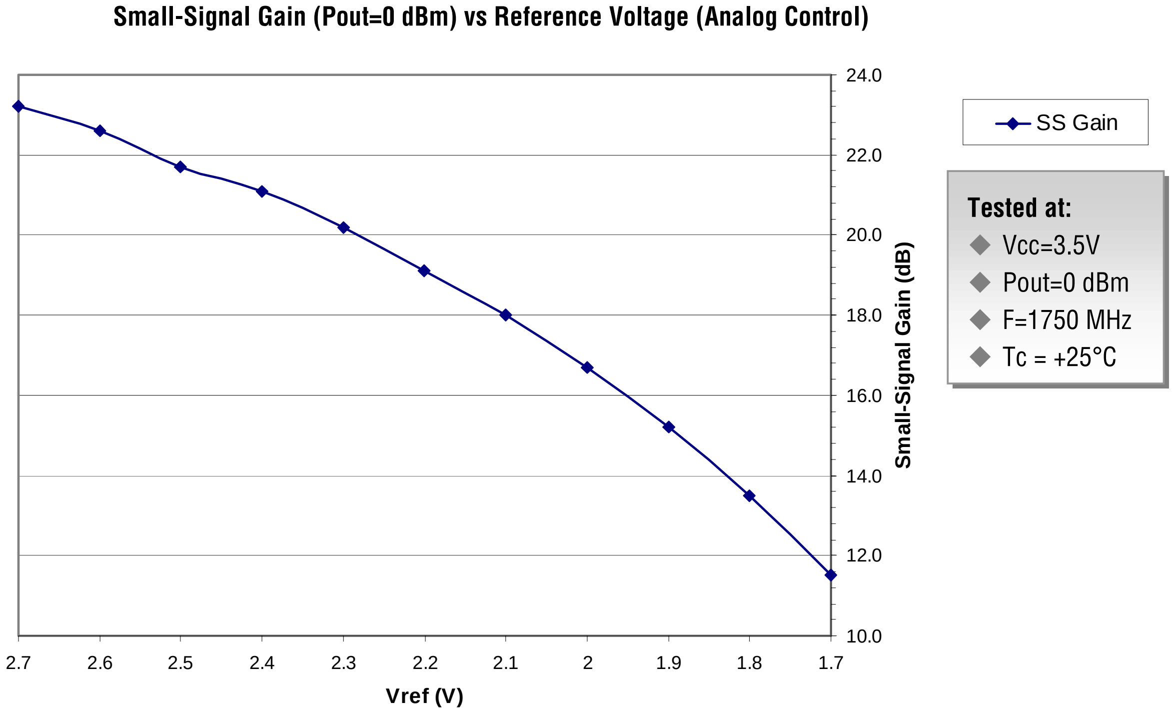

Figure 14

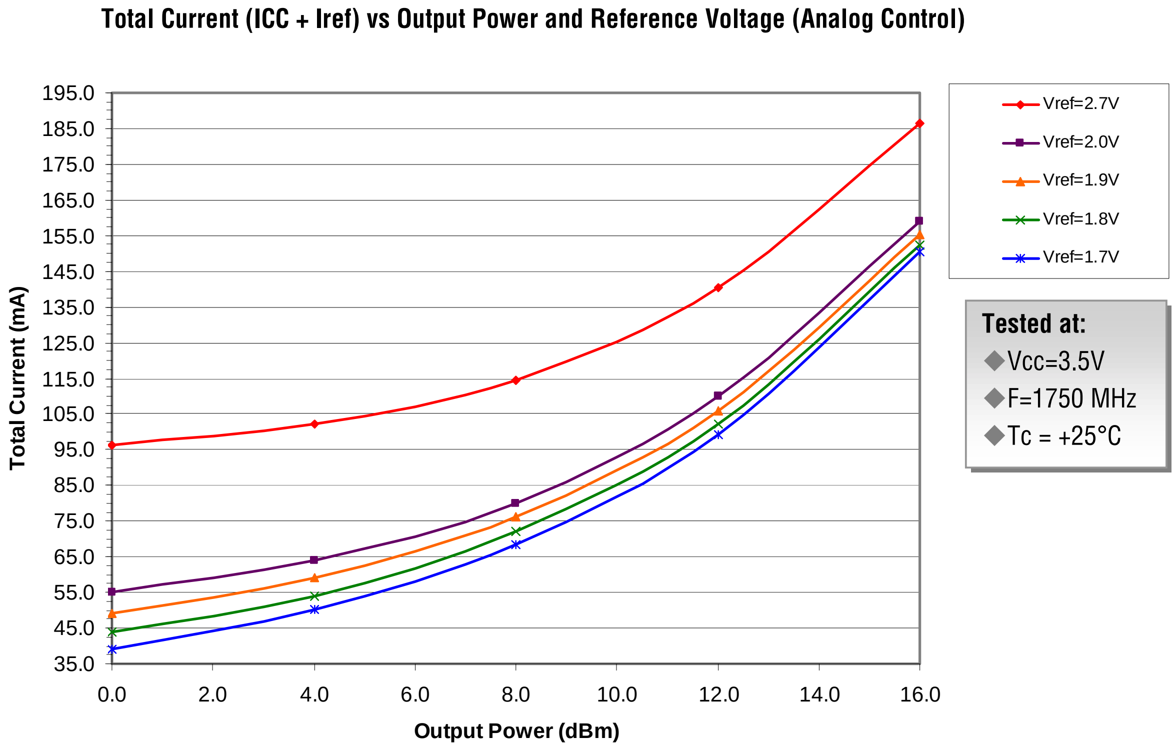

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Figure 15

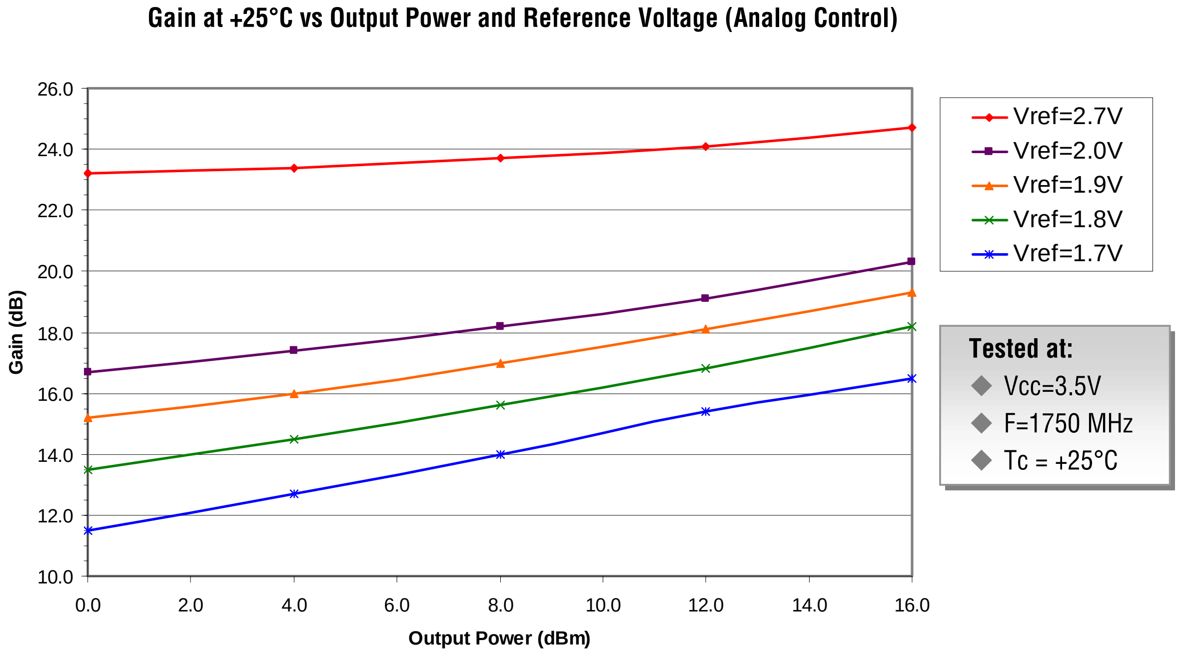

Figure 16

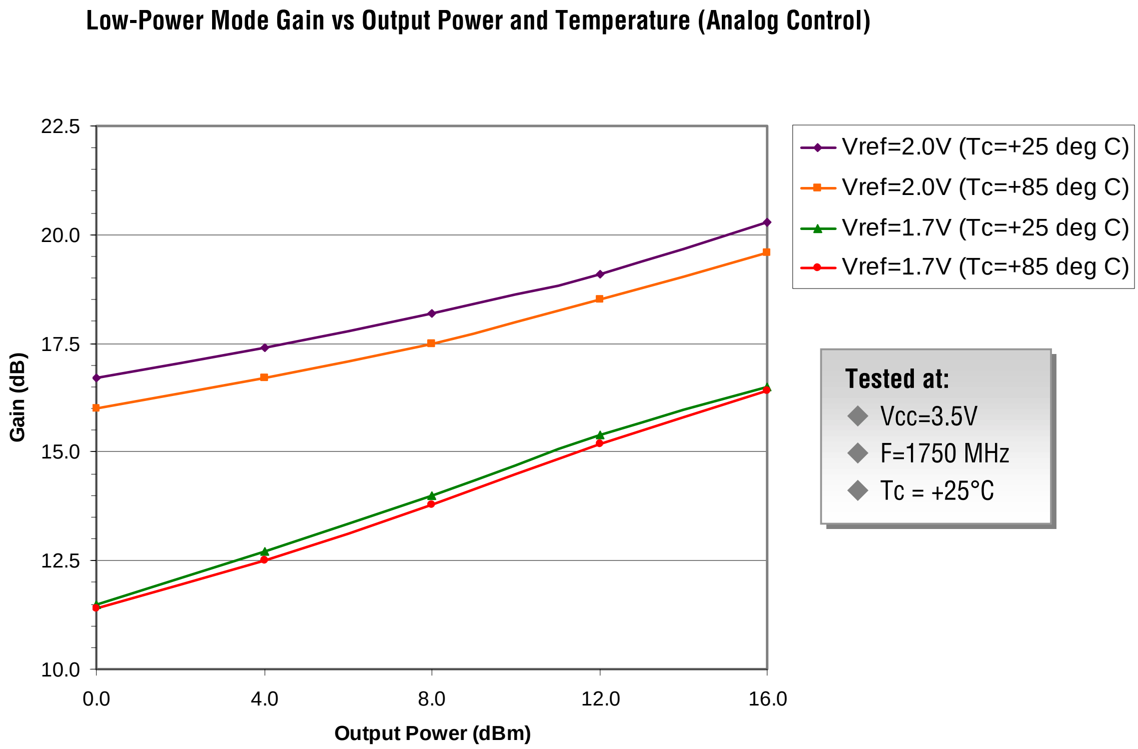

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Figure 17

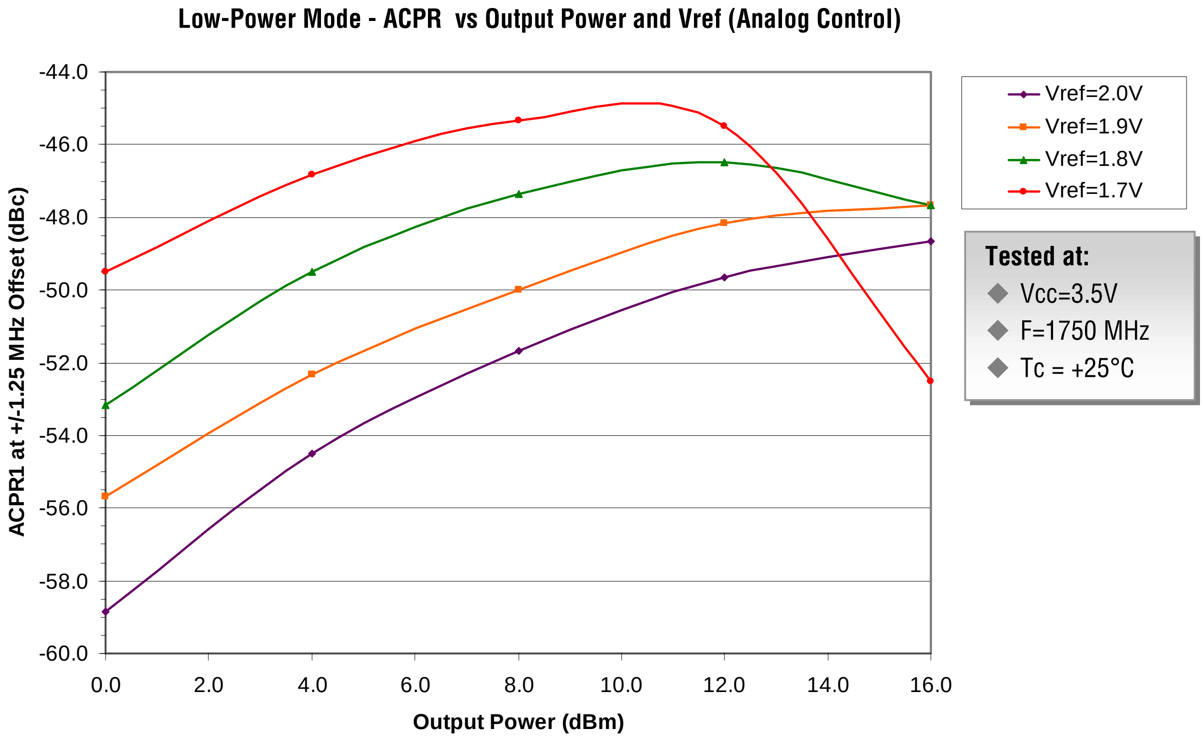

Figure 18

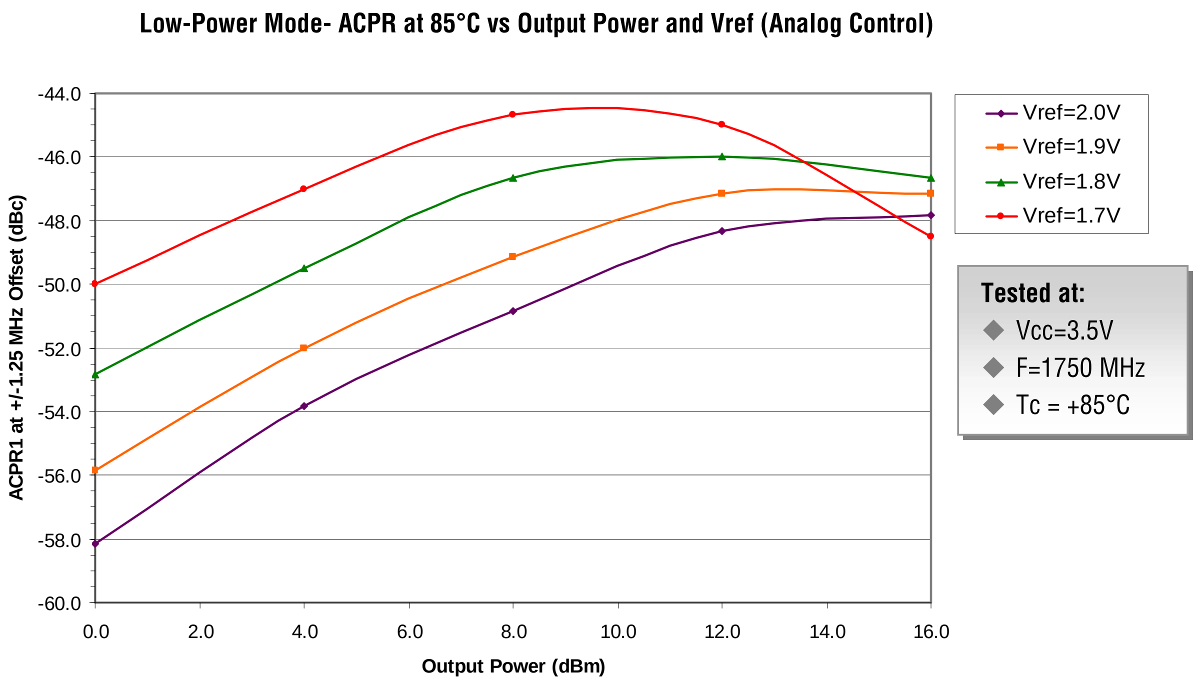

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Figure 19

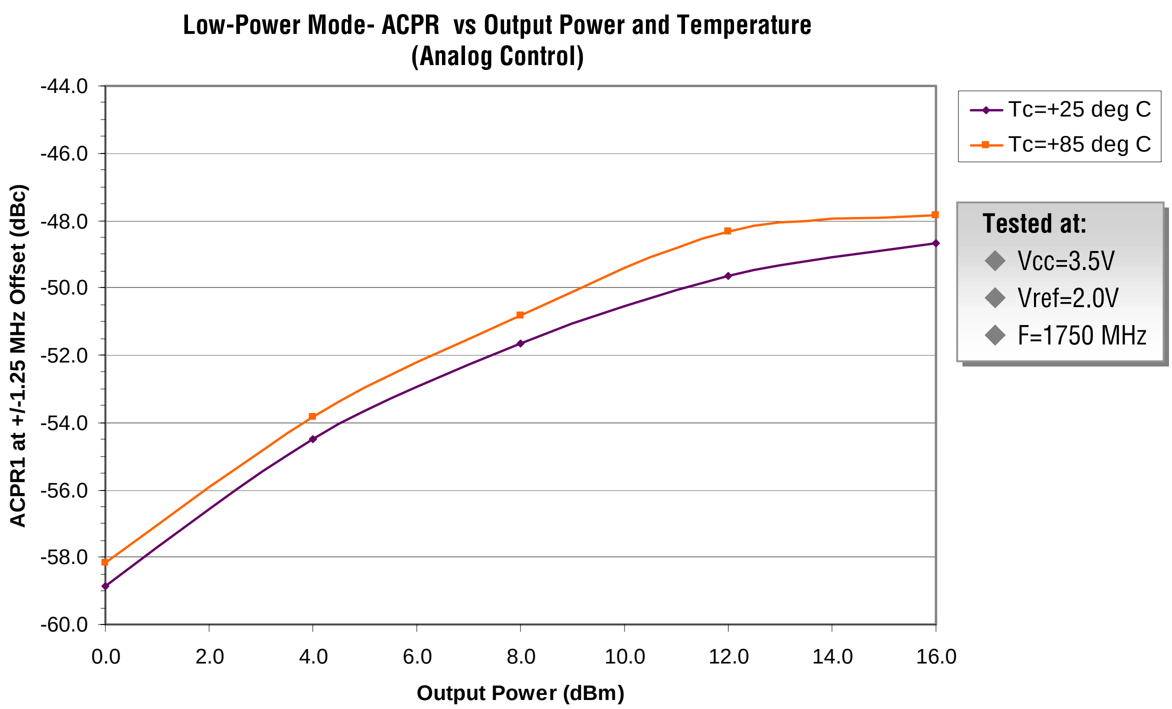

Figure 20

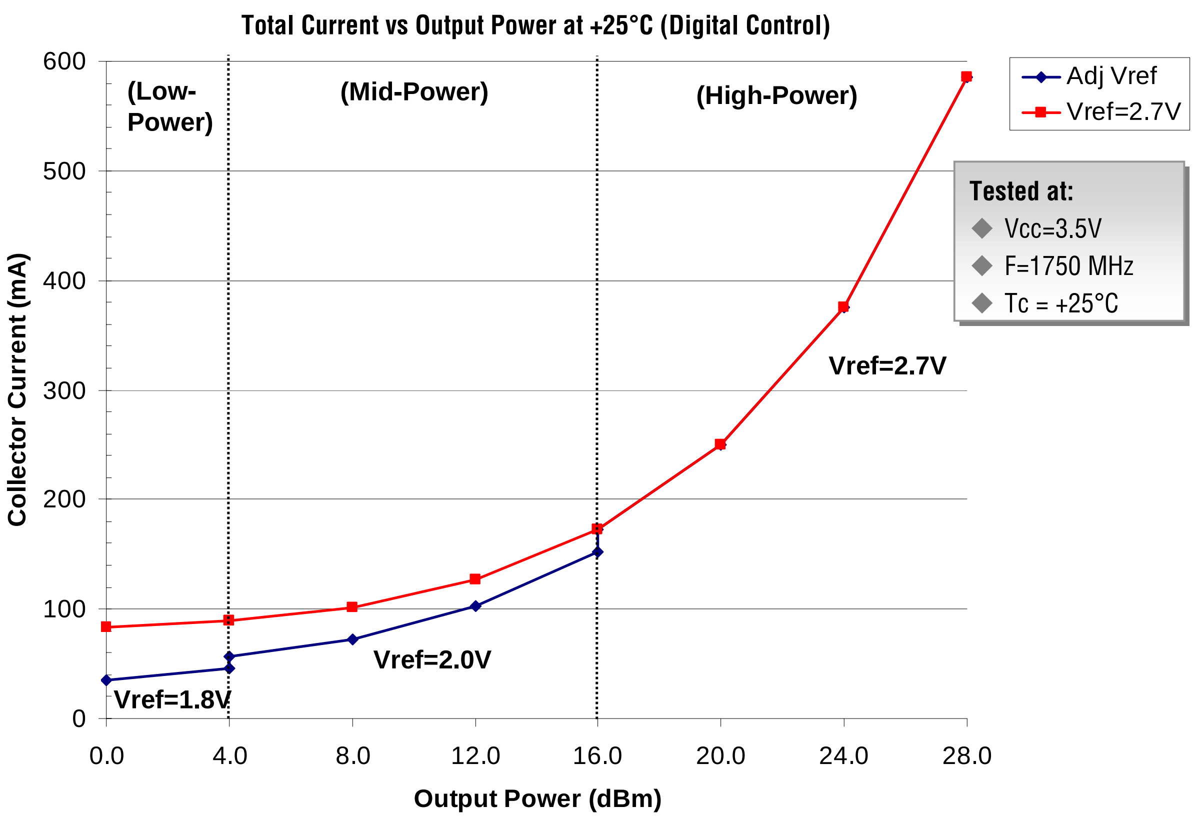

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Figure 21

Total Current vs Output Power (Pout ≤+16 dBm) at +25°C (Digital Control)

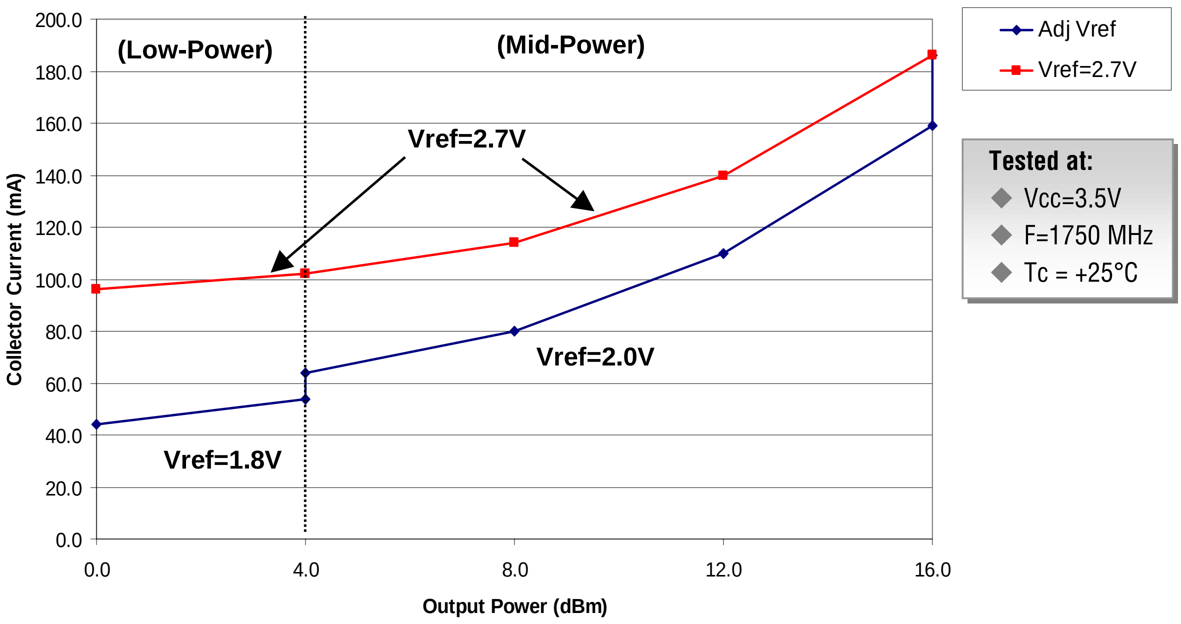

Figure 22

Small-Signal Gain (Pout ≤+28 dBm) vs Output Power at +25°C (Digital Control)

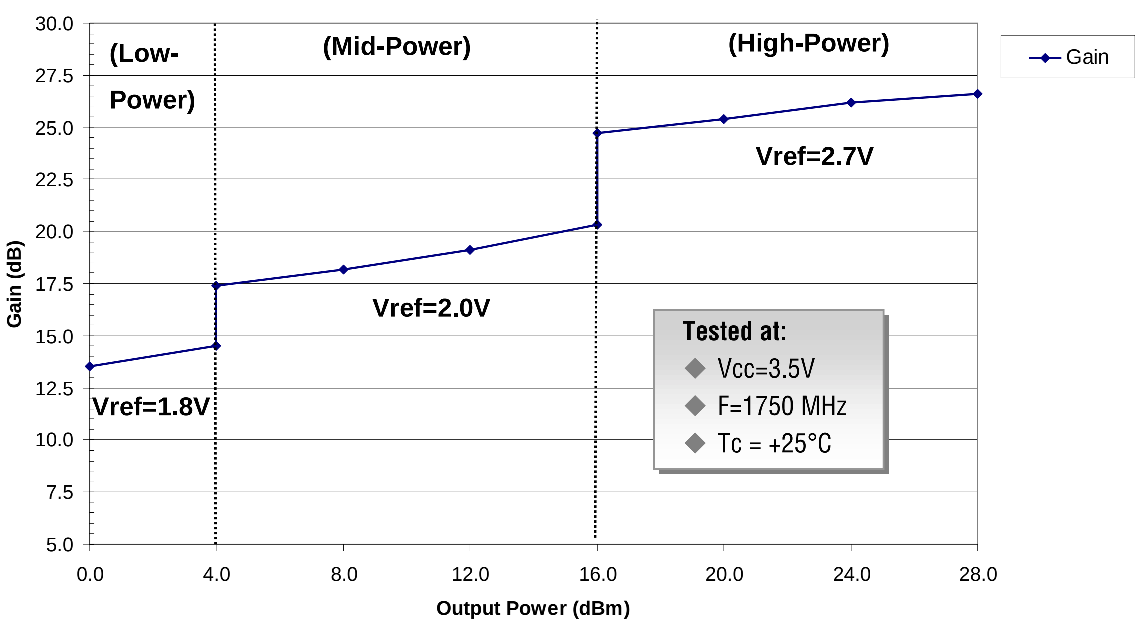

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Figure 23

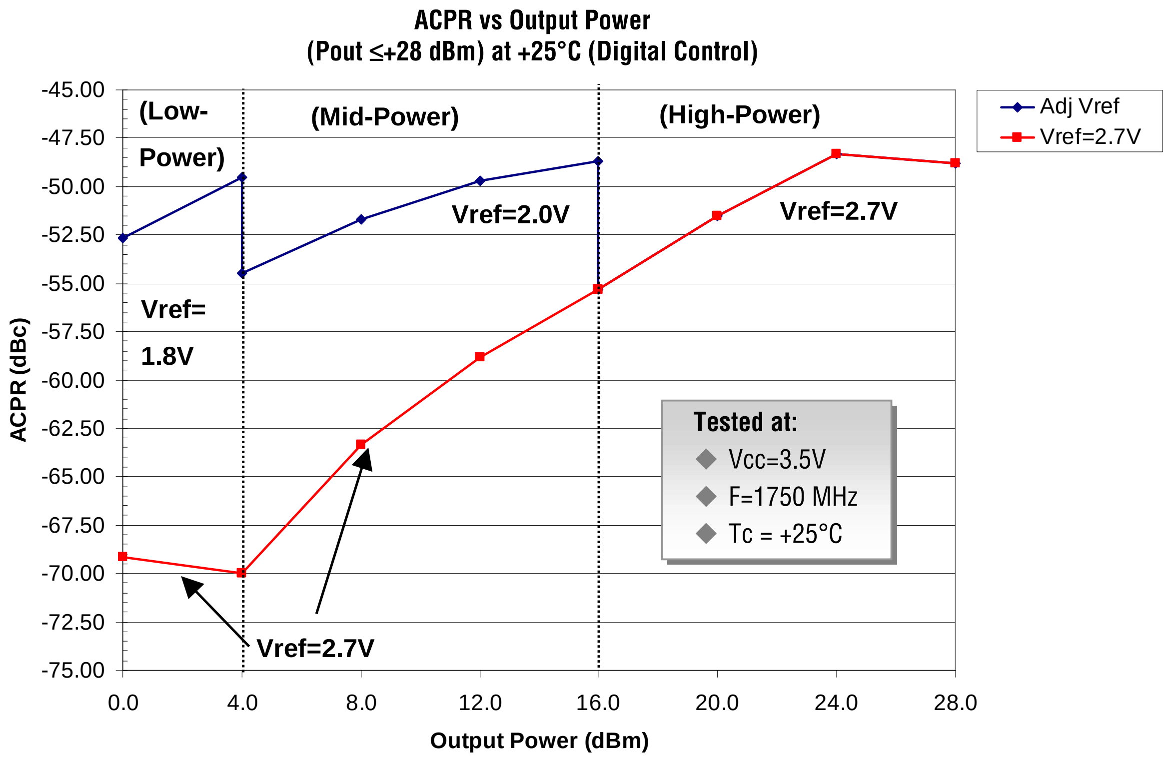
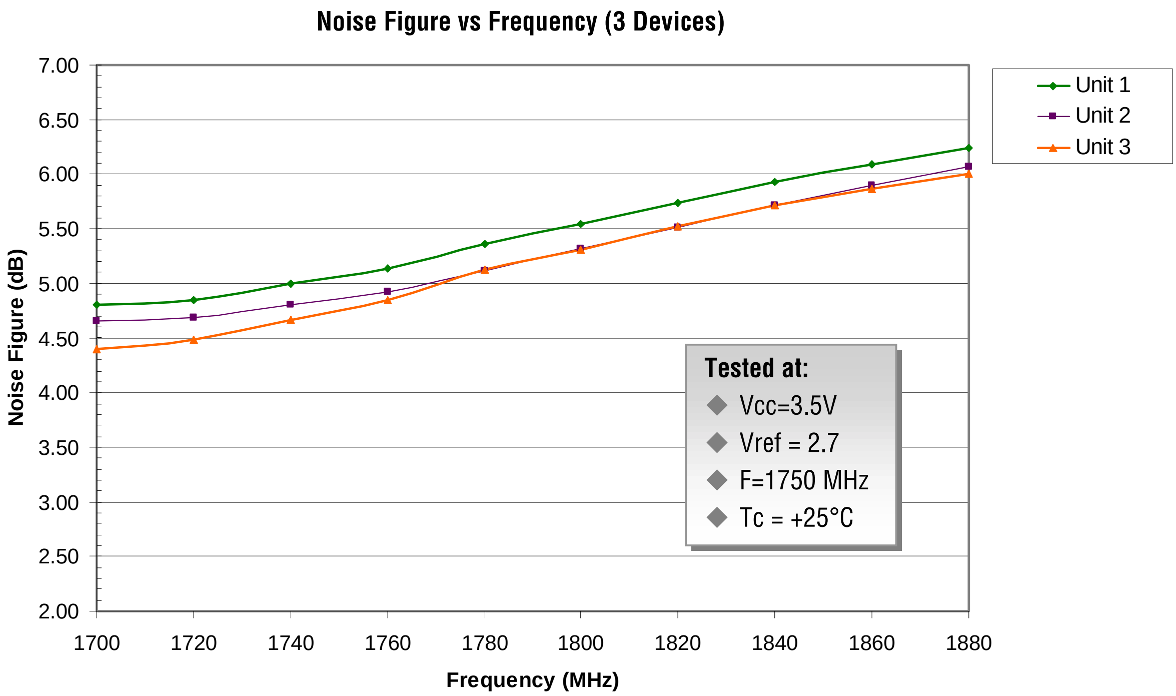


Figure 24



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