Raytheon

RMPA2051-102
3V WCDMA/CDMA2000 Power Amplifier Module

ADVANCED INFORMATION

Description

The RMPA2051-102 is a small outline, power amplifier module (PAM) for WCDMA and CDMA2000 applications. The Power Amplifier Module (PAM) is internally matched to 50 ohms and DC blocked to minimize the use of external components and reduce circuit complexity for system designers. High power-added efficiency and excellent linearity are achieved using Raytheon's Heterojunction Bipolar Transistor (HBT) process.

Features

- Single positive-supply operation
- 32% power-added efficiency at +28 dBm WCDMA average output power
- Compact LCC package: 6.0 x 6.0 x 1.5 mm3
- 50-ohm matched and DC blocked input/output
- Adjustable quiescent current and power-down mode

Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typical	Max	Units
Supply Voltage	Vcc		3.4	6.0	V
Reference Voltage	Vref	1.5	2.7	4.0	V
RF Input Power[2]	Pin		+2	+7	dBm
Load VSWR	VSWR		1.2:1	10:1	
Case Operating Temperature	Tc	-40	+25	+110	°C
Storage Temperature	Tstg	-55	+25	+150	°C

Electrical Characteristics[3]

Parameter	Min	Typ	Max	Unit
Operating Frequency	1920		1980	MHz
Gain (Po=0 dBm)		24		dB
(Po=28 dBm)		26		dB
Linear Output Power	28			dBm
Power-Added Efficiency				
(Po=27 dBm)		30		%
(Po=28 dBm)		32		%
ACLR1 (Offset ± 5MHz)				
Po=27 dBm		-40		dBc
Po=28 dBm		-38		dBc
ACLR2 (Offset ± 10 MHz)				
Po=27 dBm		-60		dBc
Po=28 dBm		-58		dBc
Noise Figure		5		dB
Input VSWR (50 Ω)		2.0:1	2.5:1	---
Output VSWR (50 Ω)		3.5:1		

Parameter	Min	Typ	Max	Unit
Noise Power (Po≤28 dBm)			-135	dBm/Hz
Stability (All spurious)[4]			-70	dBc
Harmonics (Po ≤ 28 dBm)				
2fo, 3fo, 4fo			-30	dBc
Quiescent Current				
(Vref=2.7V)		80	100	mA
(Vref=2.0V)		50		mA
(Vref=1.7V)		35		mA
Power Shutdown Current[5]		2	10	uA
Vcc	3.0	3.5	4.5	V
Vref	1.7	2.7	3.2	V
Iref		13		mA
Case Operating Temp.	-30		+85	°C

Notes:

1. No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.
2. Typical RF input power for WCDMA P_{out} = +28dBm.
3. All parameters met at Tc =+25°C, Vcc =+3.5V, Vref=+2.7V, f=1950 MHz and load VSWR ≤ 1.2:1.
4. Load VSWR ≤ 6:1, all phase angles.
5. No applied RF signal. Vcc=+3.5V nominal, Vref=+0.2V maximum.

Characteristic performance data and specifications are subject to change without notice.

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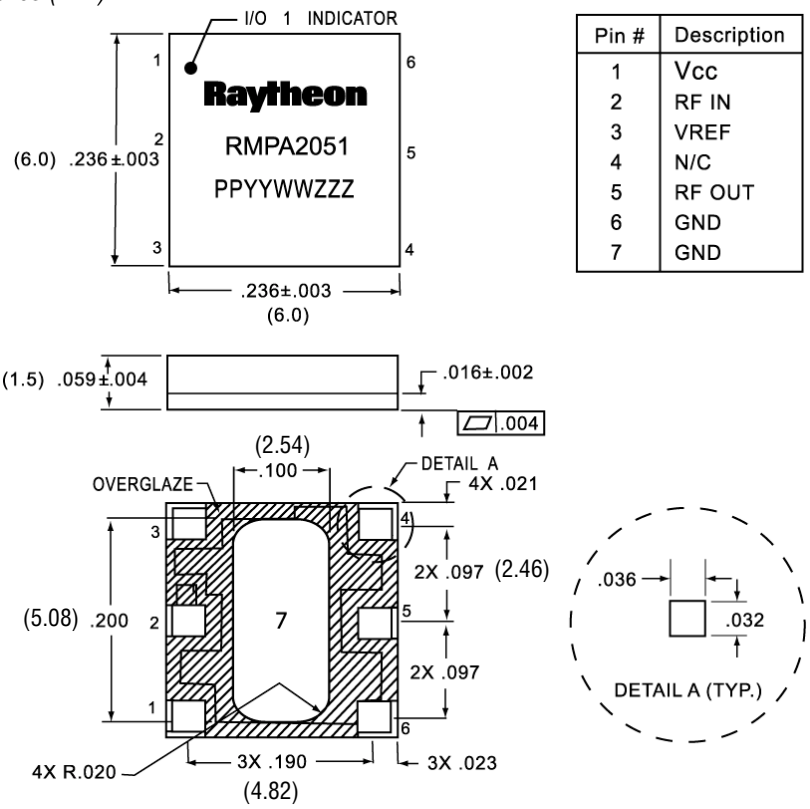
Figure 1
Package Outline and Pin Designations

Dimensions in inches (mm)

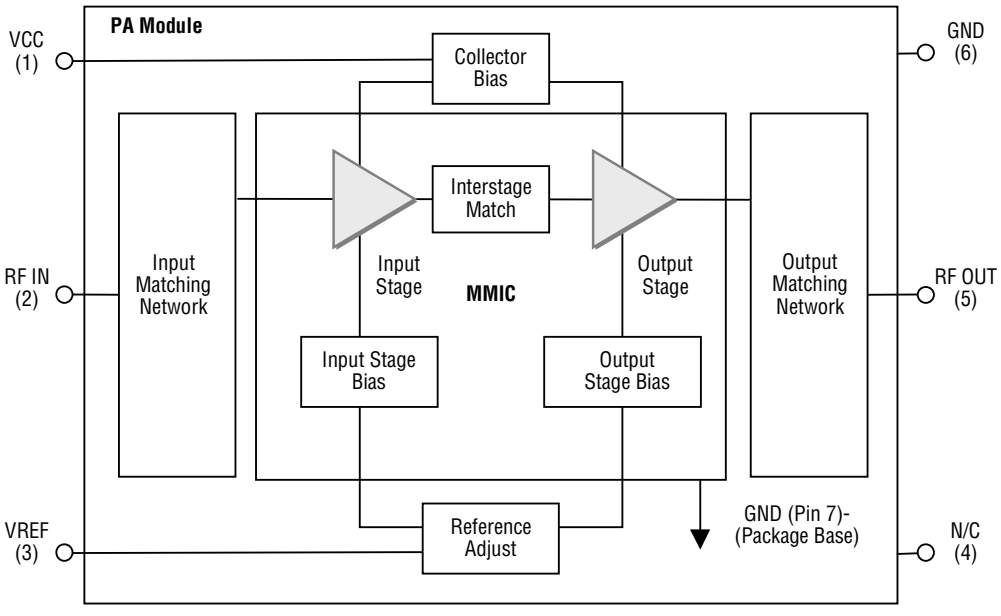


Pin #	Description
1	Vcc
2	RF IN
3	VREF
4	N/C
5	RF OUT
6	GND
7	GND

Figure 2
Functional Block Diagram of Packaged Product

VCC=3.5V (nom)
VREF=2.7V (nom)
1920-1980 MHz
50 Ohms I/O

(Topside View)



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Evaluation Board Layout, Schematic and Instructions

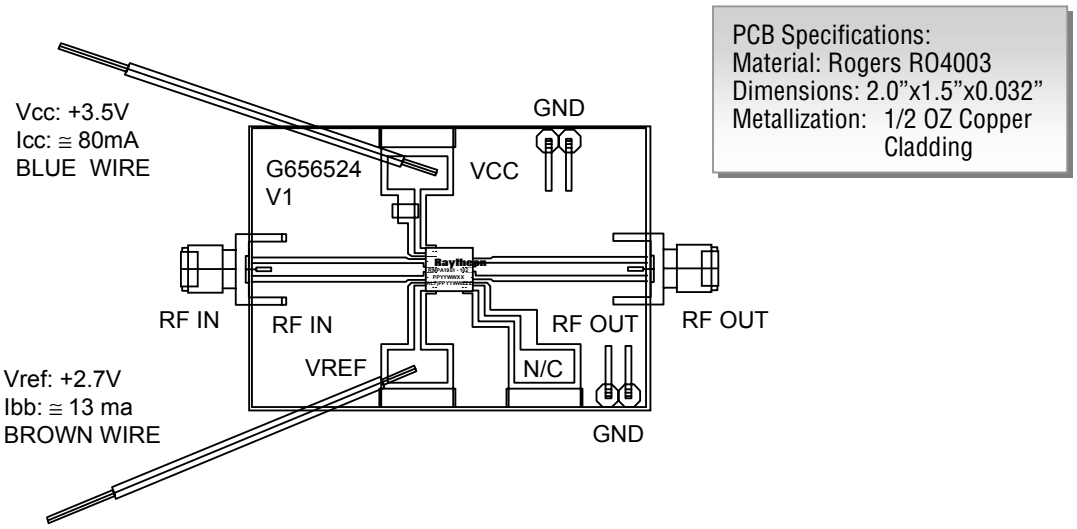
With device marking oriented right side up, RF IN is on the left and RF OUT is on the right. Blue wire is collector DC voltage input (pin 1). VCC= +3.5V nominal.

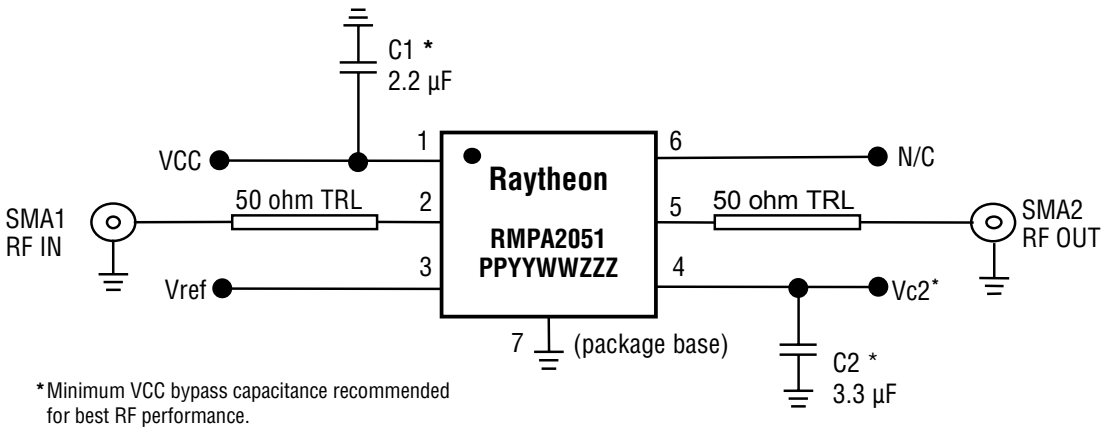
Brown wire is reference DC voltage input (pin 3). Vref=+ 2.7V nominal to obtain Iccq= 80 mA. Operation at lower or higher quiescent currents can be achieved by decreasing or increasing Vref voltage relative to +2.7V.

First apply +3.5V to the collector supply (blue wire). Next apply +2.7V to the reference supply to brown wire. Quiescent collector current with no RF applied will be about 80 mA. Reference supply current with or without RF applied will be about 13 mA. When turning amplifier off, reverse power supply sequence.

Apply -20 dBm RF input power at WCDMA frequency (1920-1980 MHz). After making any initial small signal measurements at this drive level, input power may be increased up to a maximum of +6 dBm for large signal, single-tone or digital WCDMA measurements. Do not exceed +6 dBm input power.

Figure 3
Evaluation Board Layout and Schematic





*Minimum VCC bypass capacitance recommended for best RF performance.

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Application Information

- **Precautions to Avoid Permanent Device Damage:**
  - Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.
  - Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
  - Static Sensitivity: Follow ESD precautions to protect against ESD damage:
    - A properly grounded static-dissipative surface on which to place devices.
    - Static-dissipative floor or mat.
    - A properly grounded conductive wrist strap for each person to wear while handling devices.
  - General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
  - Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.
- **Device Usage:** Raytheon recommends the following procedures prior to assembly.
  - Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
  - Assemble the dry-baked devices within 7 days of removal from the oven.
  - During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
  - If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.
- **Solder Materials & Temperature Profile:** Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.
  - **Reflow Profile**
    - Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
    - Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
    - Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
    - Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. Figure 1 indicates the recommended soldering profile.
- **Solder Joint Characteristics:** Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.
- **Rework Considerations:** Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

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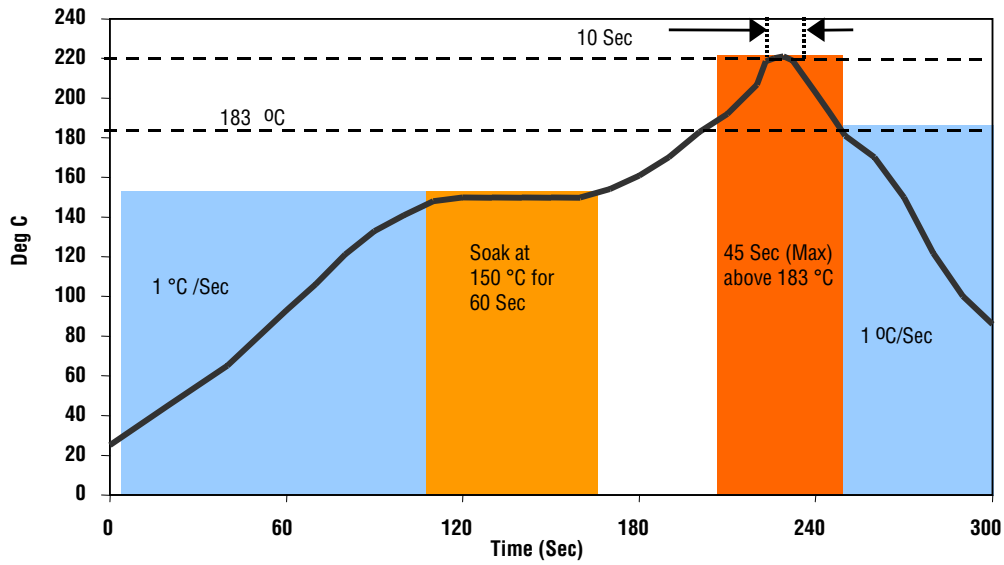
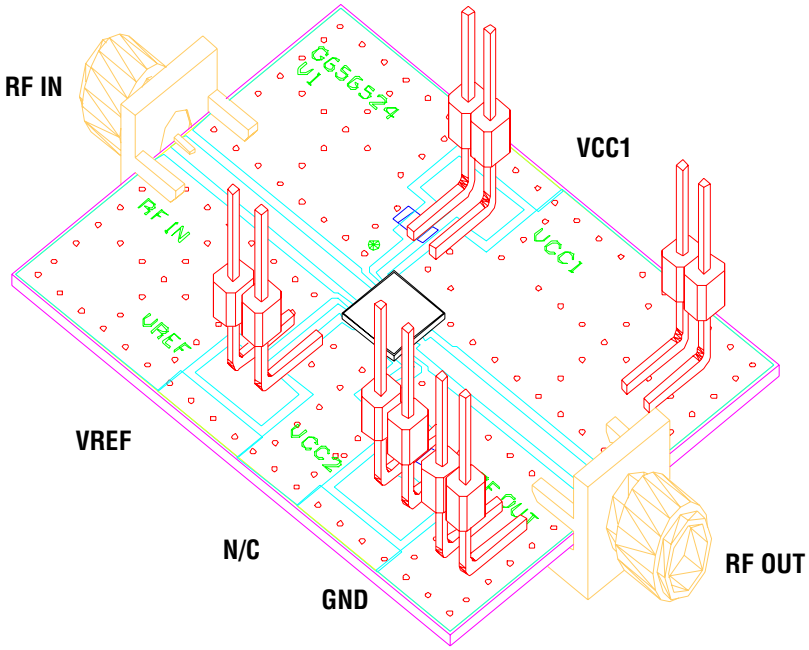
Figure 4
Recommended Solder Reflow Profile



Alternate Evaluation Board Layout

An alternate configuration for the sample evaluation board is shown below. One of the five test terminals is not required for product testing. Test conditions and instructions are otherwise the same.



WCDMA Test Conditions:

ACLR1 Offset:	± 5.0 MHz	Modulation:	OCQPSK
ACLR2 Offset:	± 10 MHz	Chip Rate:	3.84 Mcps
Resolution BW:	30 kHz	Filter:	WCDMA (RRC)
Uplink;DPCCH+1 DPDCH			

PCB Specifications:

Material:	Rogers RO4003
Dimensions:	2.0"x1.5"x0.032"
Metallization:	1/2 OZ Copper Cladding

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Figure 5
Performance Data

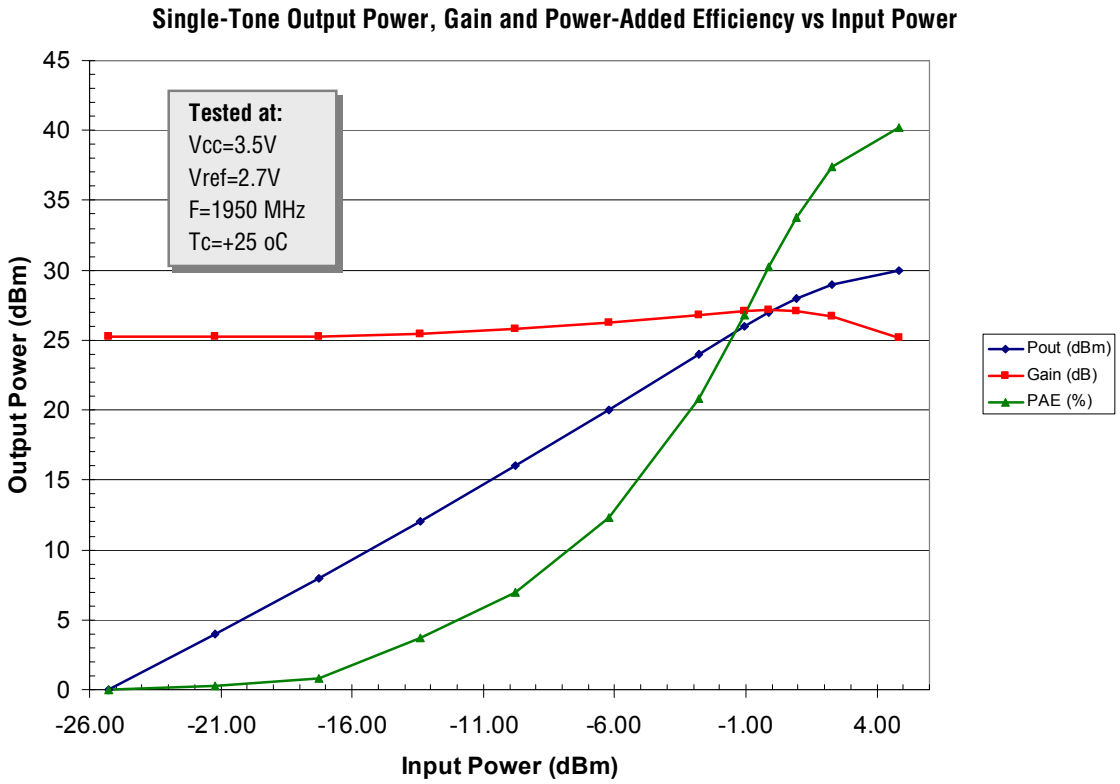

Figure 6

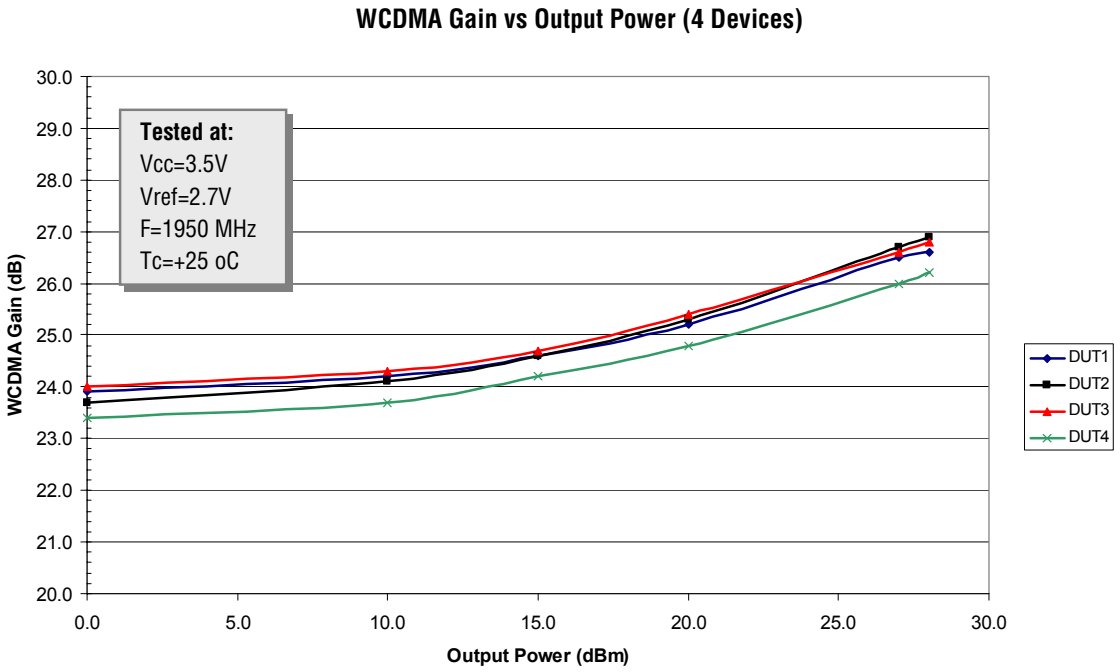

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Figure 7

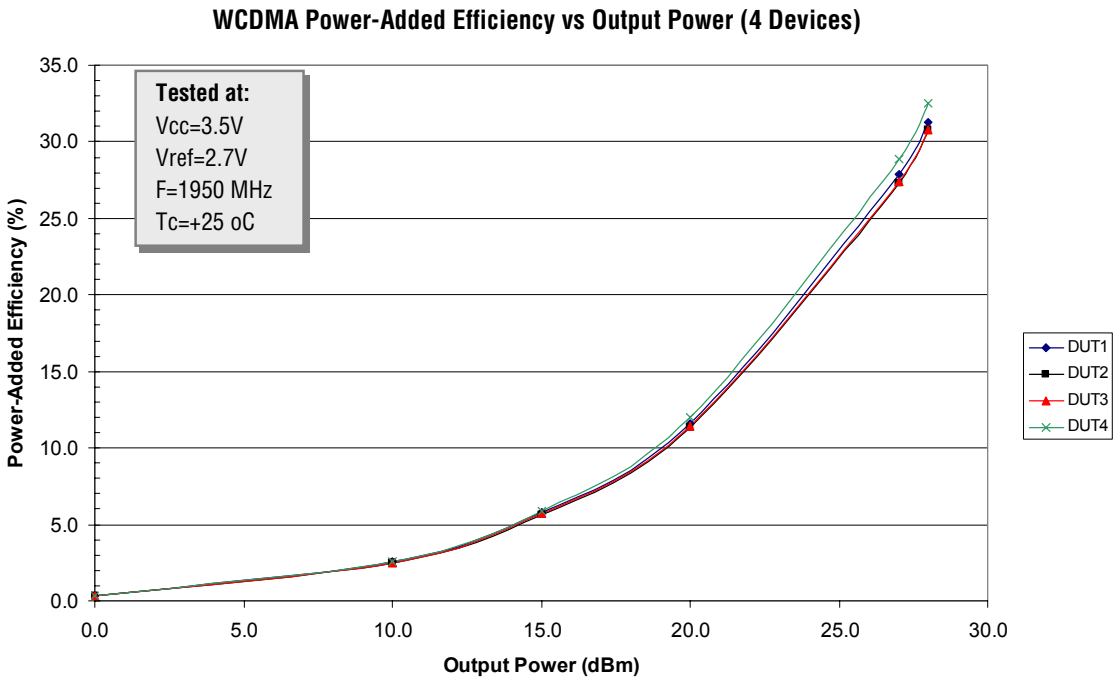

Figure 8

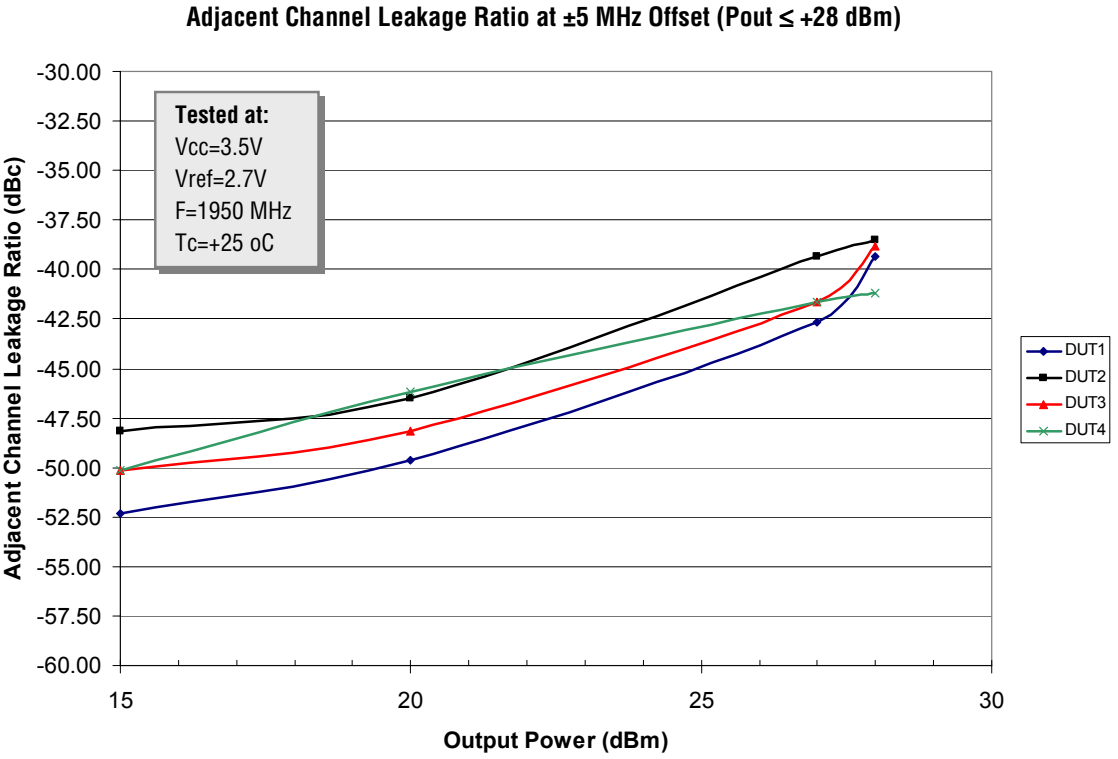

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Figure 9

Adjacent Channel Leakage Ratio at ±10 MHz Offset (Pout ≤ +28 dBm)

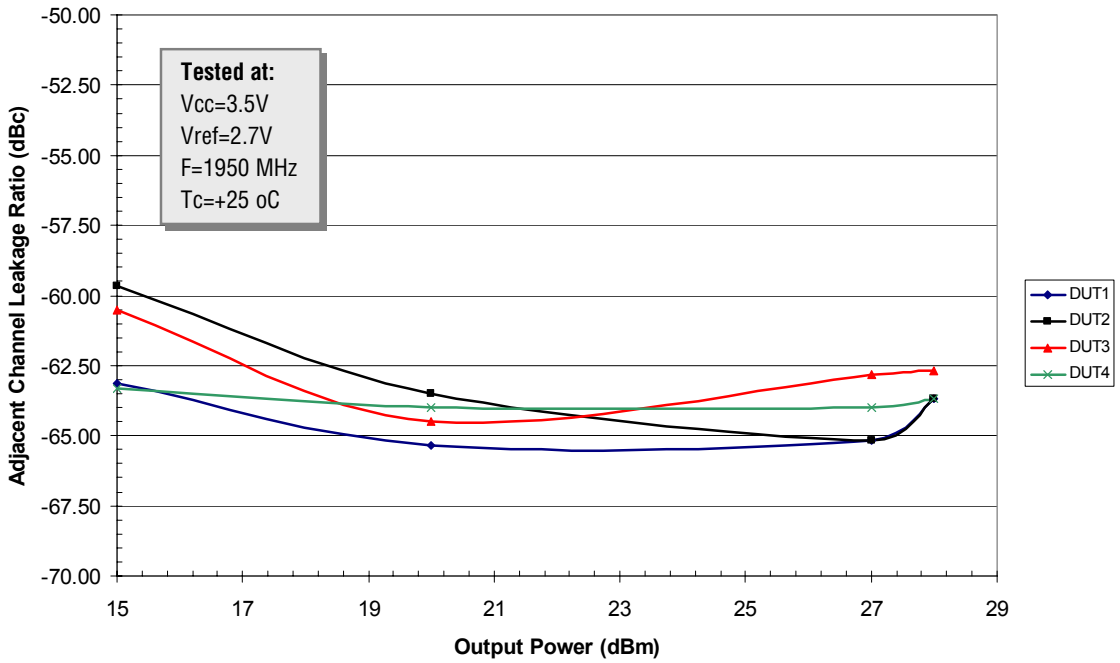
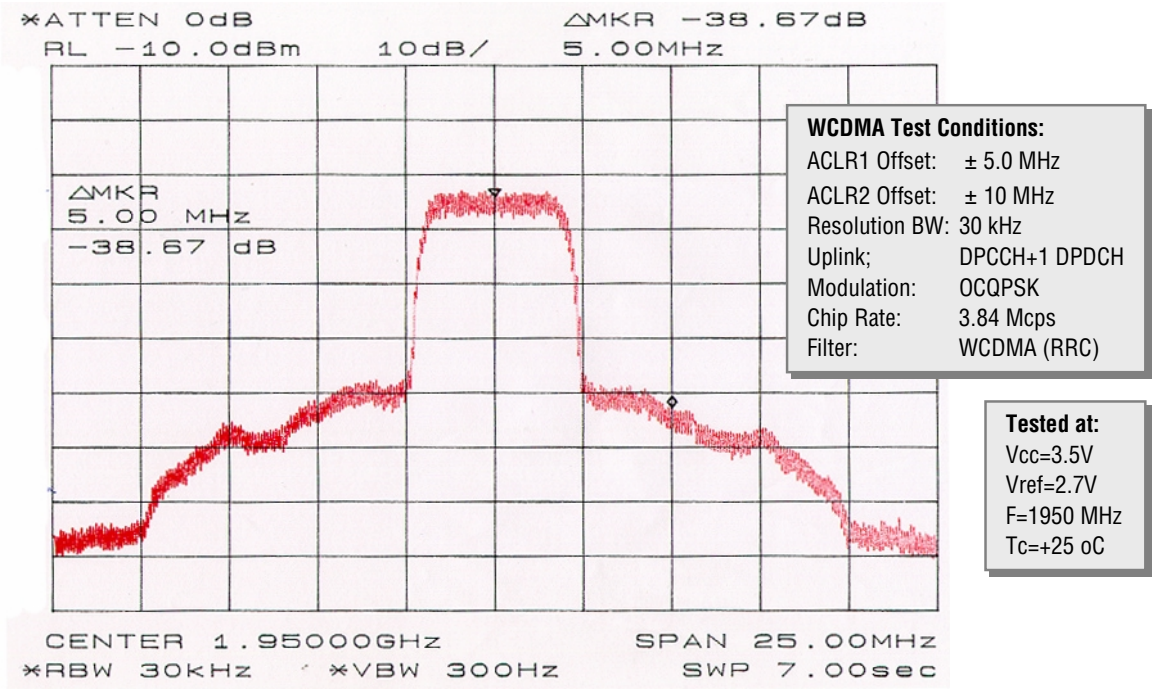


Figure 10

Typical WCDMA Spectral Output and ACLR at ±5.00 MHz Offset



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