Raytheon RMPA39200 **37-40 GHz 1.6 Watt Power Amplifier MMIC**

PRODUCT INFORMATION

Decemption multi-point communications, LMDS and other millimeter wave applications. The RMPA93200 is a 3-stage G MMC amplifier utilizing Raytheon's advanced 0.15 gum gate length Power PHEME process and can be used conjunction with other driver or power amplifiers to achieve the required total power output. Features • 19 dB small signal gain (typ.) • 32 dBm power out (typ.) • 23 dBm power out (typ.) • Gircuit to instains individual source vias • • Chrip Size 4.28 mm x 3.19 mm • <th< th=""><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>-</th><th></th><th></th><th></th><th></th></th<>									-				
$\begin{array}{c} \textbf{9} \textbf{32} \text{ dBm power out (typ.)}\\ \textbf{9} \textbf{32} \text{ dBm power out (typ.)}\\ \textbf{9} \textbf{Circuit contains individual source vias}\\ \textbf{9} \textbf{Chip Size 4.28 mm x 3.19 mm}\\ \hline \textbf{10} \textbf{10}$	Description	The Raytheon RMPA39200 is a high efficiency power amplifier designed for use in point to point radio, point to multi-point communications, LMDS and other millimeter wave applications. The RMPA39200 is a 3-stage GaAs MMIC amplifier utilizing Raytheon's advanced 0.15µm gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.											
Maximum RatingsMaximum Positive DC Voltage (+5 V Typical) Negative DC Voltage Simultaneous (Vd - Vg) Positive DC Voltage Simultaneous (Vd - Vg) Positive DC Current RF Input Power (from 50 Ω source) Operating Base plate Temperature Storage Temperature Range Tc -30 to +85 °C Storage Temperature Range Tstg -55 to +125 °C Rjc 8 °C/WVistor Vdg -2 Volts Vdg Positive DC Voltage Pin Tc -30 to +85 °C Storage Temperature Range Rjc 8 °C/WElectrical Characteristics (At 25°C) 50 Ω system, Vd=+5 V, Quiescent current (Idq) = 1600 mAParameter Min Typ (Fa3.5-40 GHz) Tf 10 (Pin-0 dBm) (Gain Variation vs. Frequency Ric 1.35.5.40 GHz)Parameter A do V H-1.5 A db MBParameter Min Typ Max Va H-1.5 MBParameter Min Typ Max Max Min Max Max Drain Current at Pin-0 dBm Drain Current at Pin-0 dBm 100 1700 1700 1700 1700 16 177 190 16 177 190 116 177 190 116 117 117 119 116 117 111 119 116 117 110 11	Features	 32 dBm power out (ty Circuit contains individual 	/p.) idual so	ource vias									
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(Pin=+16 dBm)		(f=38.5-40 GHz)											
		(Pin=+16 dBm)											
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Note:

1. Typical range of the negative gate voltages is -0.5 to 0.0V to set typical Idq of 1600 mA.

Characteristic performance data and specifications are subject to change without notice.

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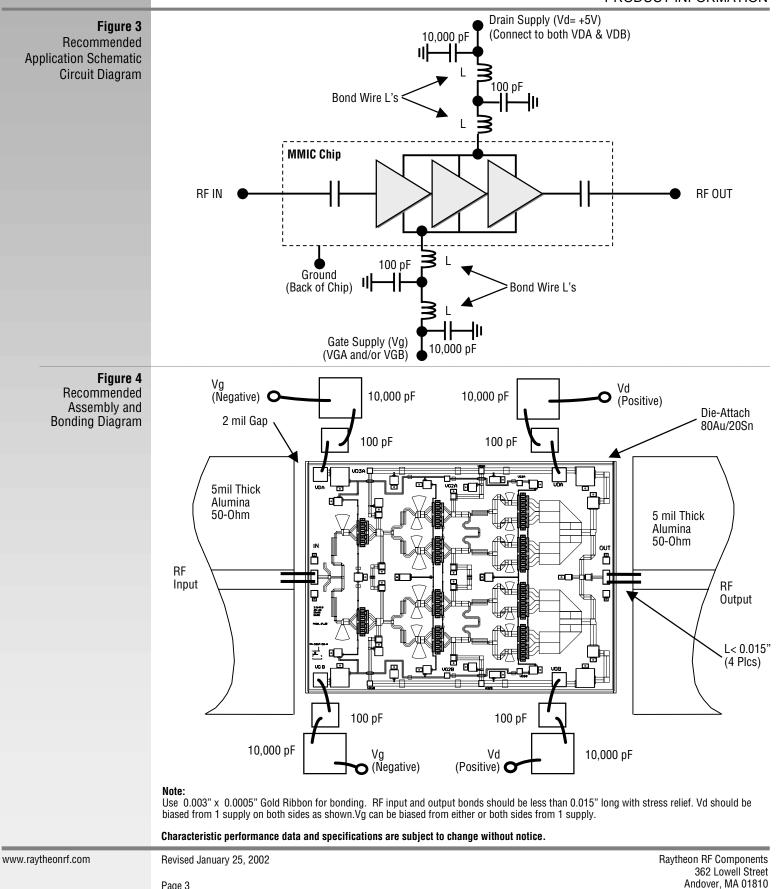
PRODUCT INFORMATION

Application Information	CAUTION: THIS IS AN ESD SENSITIVE DEVICE Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal									
	conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.									
	Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground.									
	These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.									
	Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.									
Figure 1 Functional Block Diagram	Drain Supply (VDA & VDB)									
, and the second s	MMIC Chip									
	· · · · · · · · · · · · · · · · · · ·									
	Ground Gate Supply (Back of Chip) (VGA & VGB)									
Figure 2	Dimensions in mm									
Chip Layout and Bond Pad Locations										
(Chip Size=4.282 mm x 3.194 mm x 50 um.										
Back of Chip is RF and DC Ground)										
and Do dround)										
	0.0 0.205 0.889 1.954 2.426 2.954 3.500 4.282									
	Characteristic performance data and specifications are subject to change without notice.									
www.raytheonrf.com	Characteristic performance data and specifications are subject to change without notice. Revised January 25, 2002 Raytheon RF Componer 362 Lowell Street									



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Recommended Procedure for Biasing and Operation

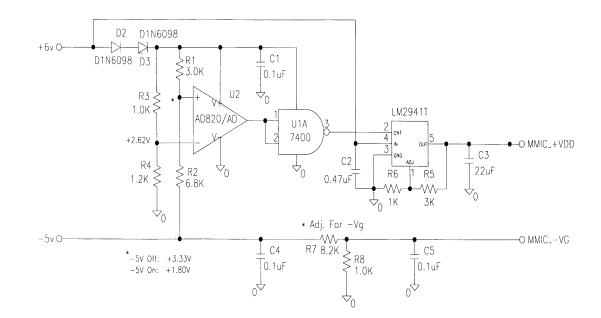
CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

- Step 1: Turn off RF input power.
- **Step 2:** Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to Vg.
- **Step 3:** Slowly apply positive drain bias supply voltage of +5 V to Vd.
- Step 4: Adjust gate bias voltage to set the quiescent current of Idq=1600 mA.
- **Step 5:** After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.
- Step 6: Follow turn-off sequence of:
 - (i) Turn off RF input power.
 - (ii) Turn down and off drain voltage (Vd).
 - (iii) Turn down and off gate bias voltage (Vg).

Note:

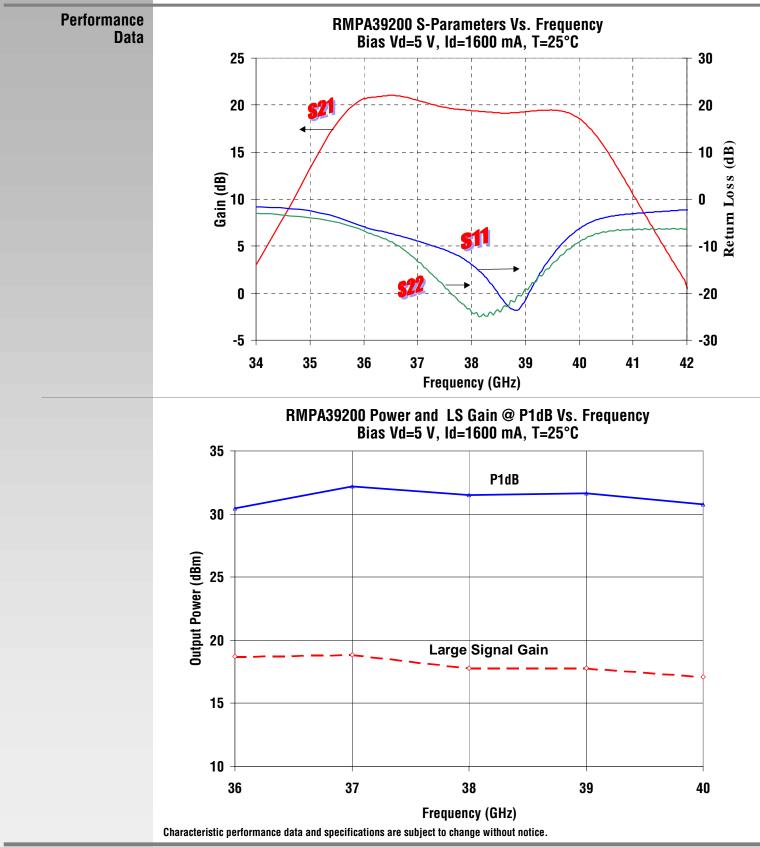
An example auto bias sequencing circuit to apply negative gate voltage and positive drain voltage for the above procedure is shown below.



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