Raytheon

RMPA1902A-58
PCS GaAs MMIC Power Amplifier

PRODUCT INFORMATION

Description

The RMPA1902-58 is a monolithic high efficiency power amplifier for PCS CDMA personal communication system applications. The MMIC requires off-chip matching. The amplifier circuit design is a single ended configuration that utilizes harmonic tuning for increased power added efficiency and linearity. The device uses Raytheon's Pseudomorphic High Electron Mobility Transistor (pHEMT) process.

Features

- Positive supply voltage of 3.5 V, nominal
- Efficiency of 36%, typical, for CDMA average power out of 29 dBm
- Small outline quad package

Absolute Maximum Ratings[4]

Parameter	Symbol	Value	Unit
Positive DC Voltage	Vd1,Vd2, Vd3	+ 9	Volts
Negative DC Voltage	Vg1,Vg2, Vg3	- 6	Volts
Simultaneous (Vd-Vg)	Vdg	+12	Volts
RF Input Power (from 50-Ohm source)	P_{IN}	+10	dBm
Operating Case Temperature	T_C	-30 to +90	°C
Storage Temperature Range	T_{Stg}	-35 to +110	°C
Thermal Resistance (Channel to case)	R_{jc}	+18	°C/W

Electrical Characteristics[1]

Parameter	Min	Typ	Max	Unit
Frequency Range	1850		1910	MHz
Gain (Small Signal)		30		dB
Gain Variation vs Temp		-0.02		dB/°C
Noise Power (1930-1990 MHz) (All Power Levels)			-137	dBm/Hz
Input VSWR (50Ω)			2.0:1	---
Stability (All spurious)[2]			-70	dBc
Harmonics (Po ≤ 29 dBm) 2fo, 3fo, 4fo		-40		dBc

Parameter	Min	Typ	Max	Unit
Power Out	29			dBm
Efficiency at Pout = 29 dBm		36		%
ACPR (Offset ≤ ± 1.25 MHz)[3]		49		dBc
Noise Figure (over temp.)			5.5	dB
Quiescent Current			135	mA
Vdd		3.5		Volts
Vgg (<4 mA)[4]	-2.0		-0.3	Volts
Case Operating Temp	-40		+85	°C

Notes:

1. Specifications are valid for Vdd = 3.5V, load = 50 Ω, and Tc = 25°C as measured in Raytheon's test fixture unless otherwise stated.
2. Source/Load VSWR ≤ 3:1 (All Angles, -50 dBm<Po<29 dBm) or Load VSWR ¤20:1 (Out of Band, All Angles, Tc=-30 to +90°C).
3. Po ≤ 29.0 dBm at Vdd=3.5V; CDMA Waveform measured using the ratio of the average power within the 1.23 MHz channel and within a 30 kHz bandwidth at a 1.25 MHz offset.
4. Vgg adjusted for quiescent current. $I_{dq1,2}$=50+/-1 mA, I_{dq3}=85+/-2 mA

Characteristic performance data and specifications are subject to change without notice.

Raytheon RF Components
362 Lowell Street
Andover, MA 01810

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

The following describes a procedure for evaluating the RMPA1902-58, a monolithic high efficiency power amplifier, in a surface mount package, designed for use in Personal Communication Systems (PCS) utilizing Code Division Multiple Access (CDMA). Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. It should be noted that RMPA1902-58 requires external passive components for DC bias and RF output matching circuits. A recommended schematic circuit is shown in Figure 3. The gate biases for the three stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of Figure 3. The following designations should be noted:

(1) Pin designations are as shown in Figure 2.

(2) Vg1 and Vg2 are the Gate Voltages (negative) applied at the pins of the package

(3) Vgg1 and Vgg2 are the negative supply voltages at the evaluation board terminals

Note: The 3 terminals of Vgg1, Vgg2 and Vgg3 may be tied together.

(4) Vd1 and Vd2 are the Drain Voltages (positive) applied at the pins of the package

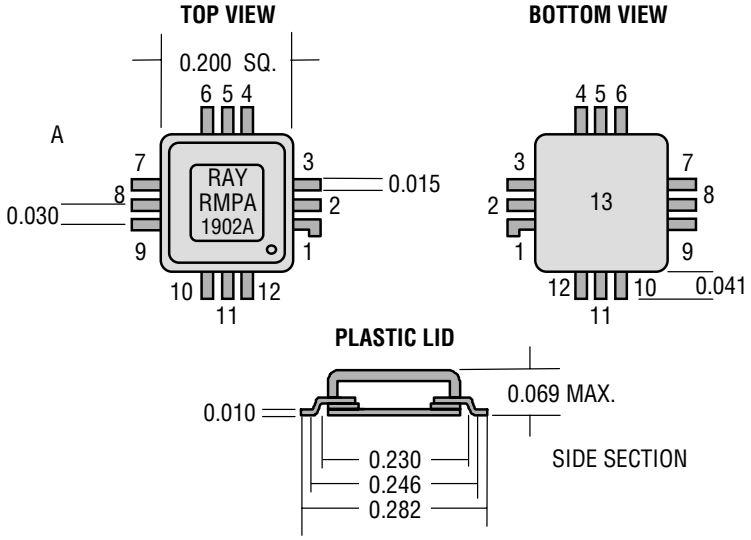
(5) Vdd1 and Vdd2 are the positive supply voltages at the evaluation board terminals

Note: The 2 terminals of Vdd1 and Vdd2 may be tied together.

The base of the package must be soldered on to a heat sink for proper operation.

Figure 1
Package Outline and Pin Designations

Dimensions in inches



Pin #	Description
1	RF Out/Vd3
2	RF Out/Vd3
3	RF Out/Vd3
4	VD1
5	GND
6	VG1
7	RF Input
8	GND
9	VG2
10	VD2
11	GND
12	VG3
13	GND

Figure 2
Functional Block Diagram of Packaged Product

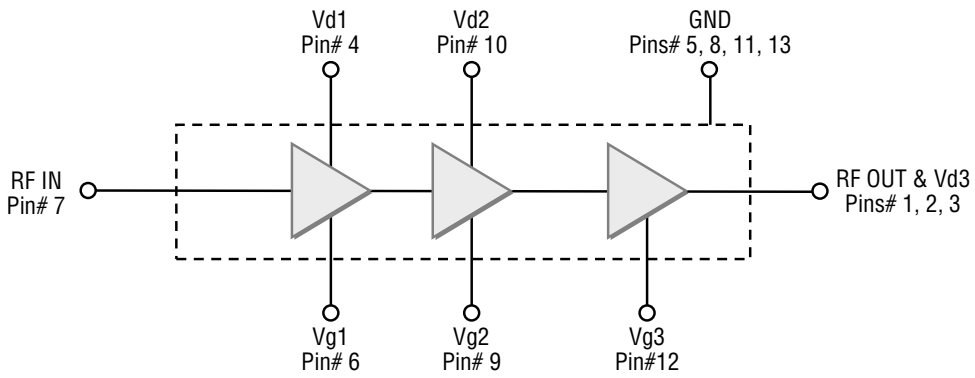


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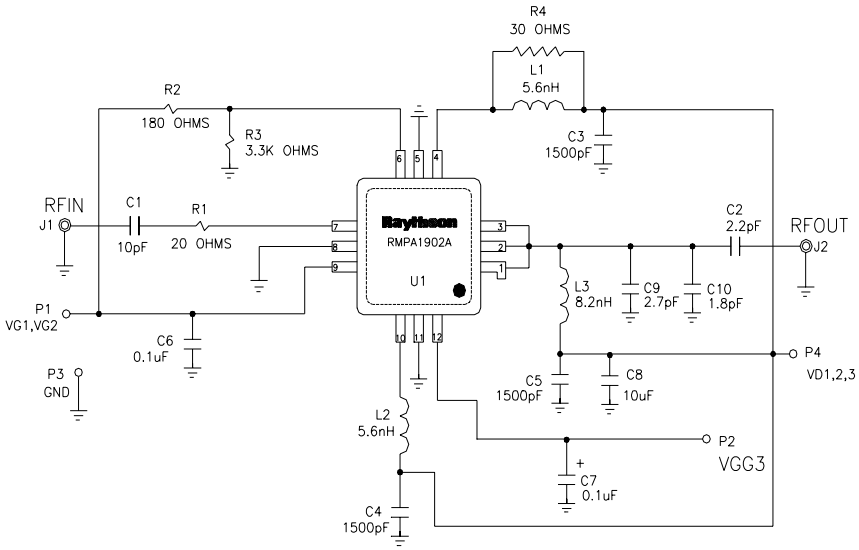
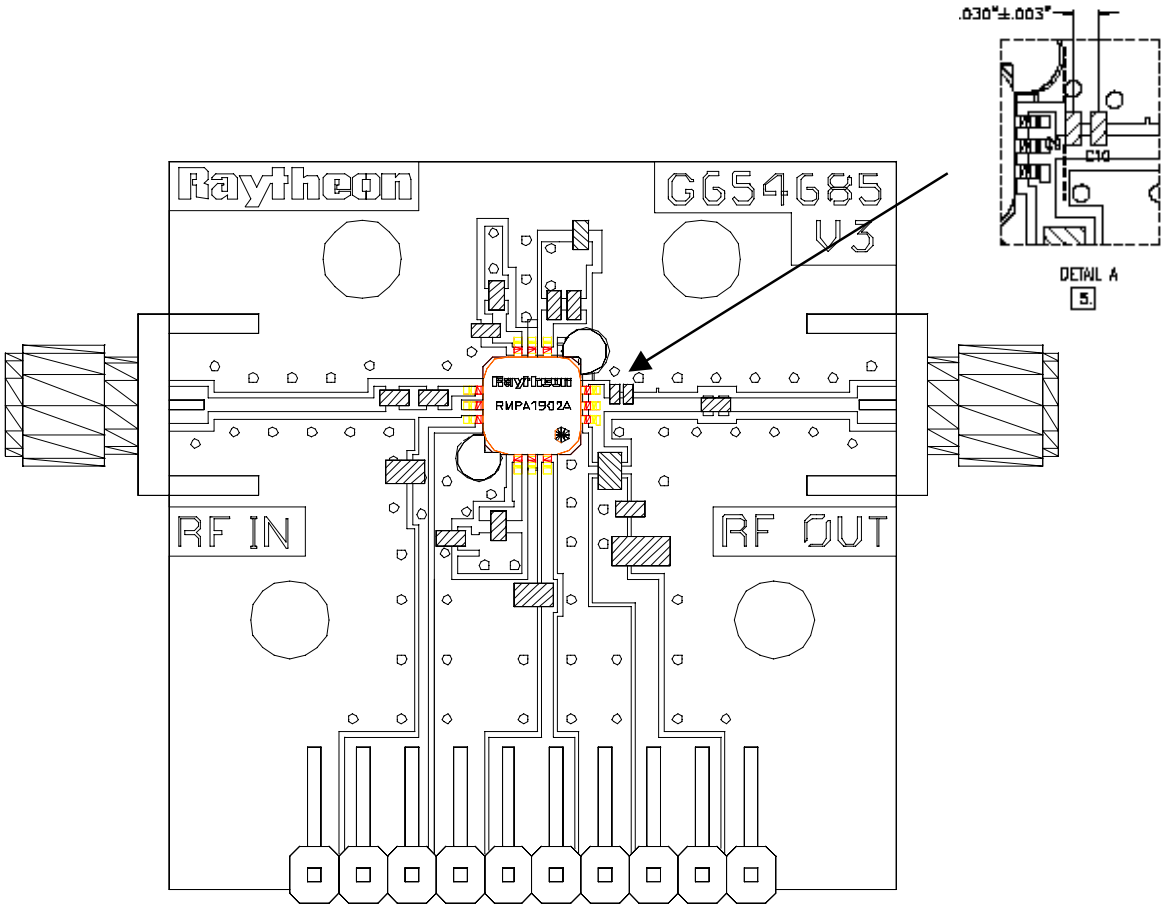
Figure 3
Schematic of Application Circuit showing external components



MATERIAL LIST

QTY	ITEM NO.	PART NUMBER	DESCRIPTION	DESG.
2	①	TOKO LL1608-FSN6	5.6nH MULTILAYER CHIP INDU. 0603	L1,L2
1	②	COILCRAFT 0603HT-8N2TKBC	8.2nH WIREWOUND CHIP INDU. 0805	L3
1	③	MURATA ELECTRONICS GRM39C0G100J050AD	10pF COG CAPACITOR 0603	C1
1	④	MURATA ELECTRONICS GRM39C0G2R2J050BD	2.2pF COG CAPACITOR 0603	C2
3	⑤	MURATA ELECTRONICS GRM39Y5V152Z50V	1500pF COG CAPACITOR 0603	C3,C4,C5
1	⑥	MURATA ELECTRONICS GRM36C0G2R7J050BD	2.7pF COG CAPACITOR 0402	C9
1	⑦	TDK CC1206JKSR10KM	10uF CAPACITOR .12" X .06"	C8
2	⑧	MURATA ELECTRONICS GRM39Y5V104Z	0.1uF CAPACITOR 0805	C6,C7
1	⑨	IMS RCI-0603-30R0J	30 OHM CHIP RESISTOR 0603	R4
1	⑩	IMS RCI-0603-20R0J	20 OHM CHIP RESISTOR 0603	R1
1	⑪	IMS RCI-0603-180J	180 OHM CHIP RESISTOR 0603	R2
1	⑫	IMS RCI-0603-3301J	3.3K OHM CHIP RESISTOR 0603	R3
1	⑬	MURATA GRM36C0G1R8J050BD	1.8pF CAPACITOR 0402	C10
2	⑭	JOHNSON COMPONENTS 142-0701-841	BRASS SMA PC MOUNT	J1,J2
1/4	⑮	3M 2340-5211TN	SINGLE ROW RIGHT ANGLE PIN HEADER; GOLD FLASH	P1-P4
1	⑯	RAYTHEON G455687	RMPA1902A-58 POWER AMPLIFIER ASSEMBLY	U1
1	⑰	RAYTHEON G654685, V3	PRINTED WIRING BOARD	PWB
A/R	⑱	INDIUM CORP. SN63	SOLDER PASTE	
2	⑲	RAYTHEON G653750-1	PUCK	PU1,PU2
A/R	⑳	DEVCON S-208	5 MIN. EPOXY ADHESIVE	
A/R	㉑	INDIUM CORP. INDALLOY #290	SOLDER	

Figure 4
Layout of Test Evaluation Board (RMPA1902-58-TB)



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Test Procedure
for the
evaluation board
(RMPA1902-58-TB)

CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2, VG3) WHILE CORRESPONDING DRAIN VOLTAGES (VD1,VD2,VD3) ARE PRESENT MAY DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies.

Slowly apply gate supply voltages of typical -2.0 V to the board terminals Vgg=Vgg1=Vgg2=Vgg3

Step 3: Slowly apply drain supply voltages of +3.5 V to the board terminals Vdd=Vdd1=Vdd2=Vdd. Adjust Vgg to set the total quiescent current (with no RF applied) Idq to nominal 135 mA. [Gate supply voltages (Vgg i.e. Vgg1, Vgg2, Vgg3) may be adjusted, only if quiescent current (Idq1 to Idq3) values desired are different from those noted on the data summary supplied with product samples]

Step 4: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.

Step 5: Follow turn-off sequence of:

(i) Turn off RF Input Power

(ii) Turn down and off drain voltages Vdd=Vdd1=Vdd2=Vdd3

(iii) Turn down and off gate voltages Vgg=Vgg1=Vgg2=Vgg3

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