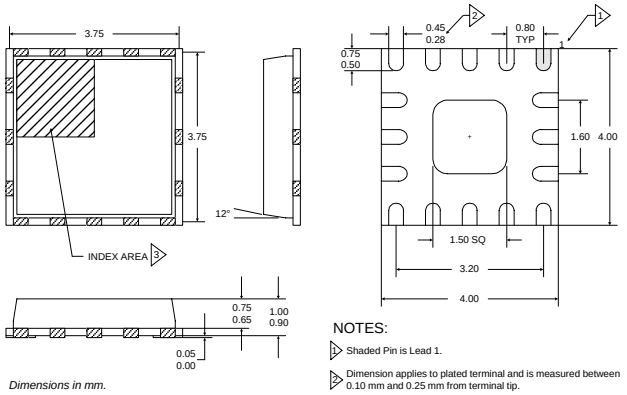
Typical Applications

- 3V CDMA/AMPS Cellular Handsets
- 3V JCDMA/TACS Cellular Handsets
- 3V TDMA/AMPS Cellular Handsets
- Spread-Spectrum Systems
- CDPD Portable Data Cards
- Portable Battery-Powered Equipment

Product Description

The RF2162 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS hand-held digital cellular equipment, spread-spectrum systems, and other applications in the 800MHz to 960MHz band. The RF2162 has an analog bias control voltage to maximize efficiency. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics. The device is packaged in a compact 4mmx4mm, 16-pin, leadless chip carrier.



Dimensions in mm.

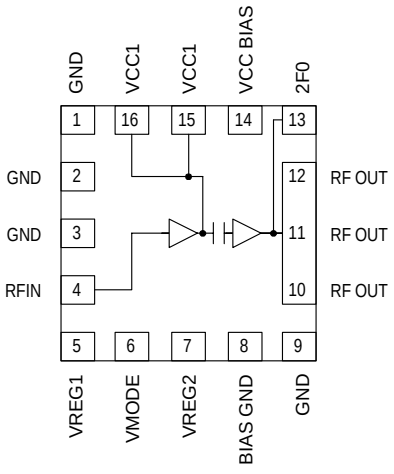
NOTES:

1. Shaded Pin is Lead 1.
2. Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.
3. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.
4. Pins 1 and 9 are fused.
5. Package Warpage: 0.05 max.

Package Style: LCC, 16-Pin, 4x4

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 29dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 960MHz Operation

Ordering Information

RF2162	3V 900MHz Linear Amplifier
RF2162 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA

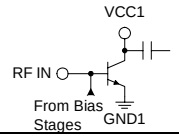
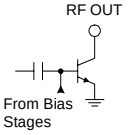
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

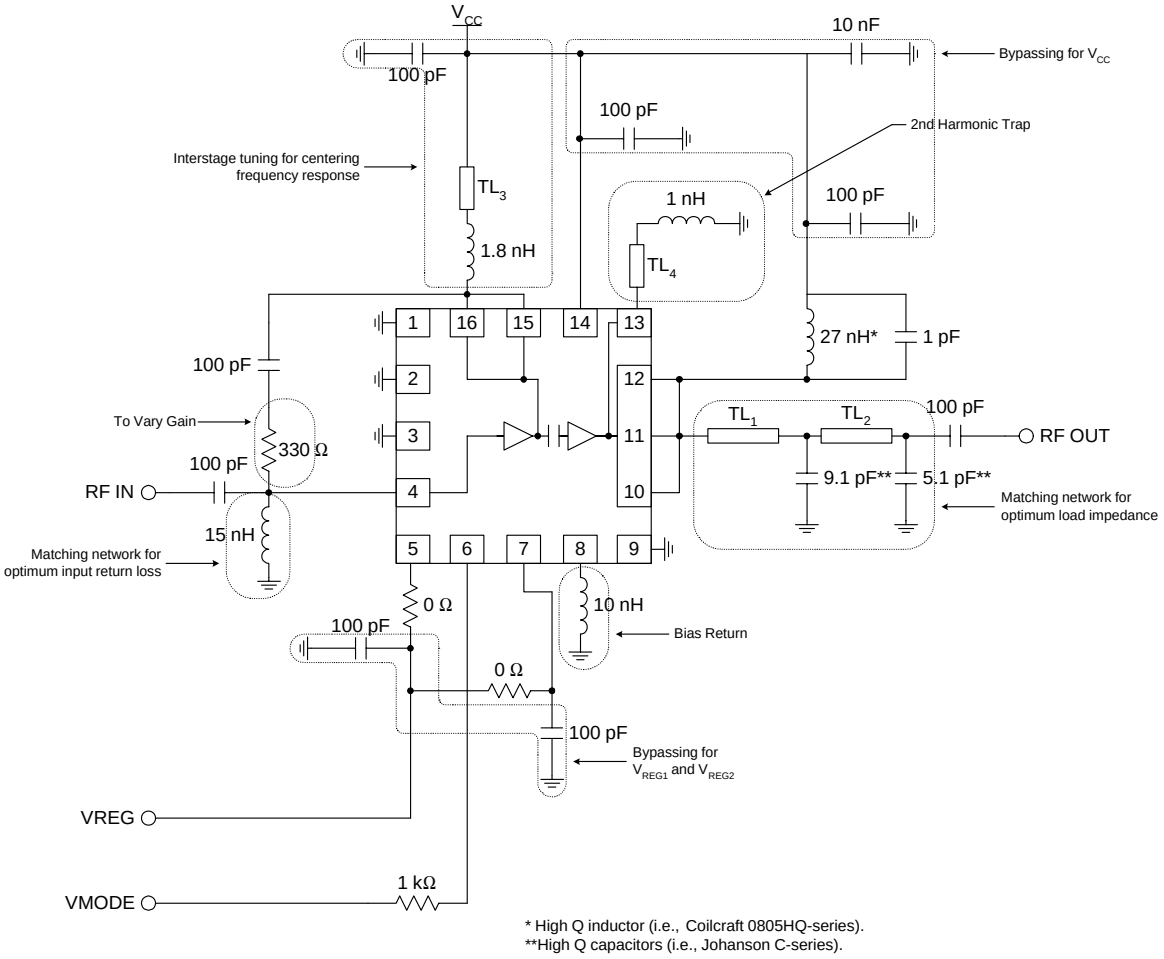
Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+4.5	V_{DC}
Mode Voltage (V_{MODE})	+3.0	V_{DC}
Control Voltage (V_{PD})	+3.0	V_{DC}
Input RF Power	+12	dBm
Operating Case Temperature	-30 to +110	℃
Storage Temperature	-30 to +150	℃
Moisture Sensitivity	Modified JEDEC Level 2	

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, Freq=824MHz to 849MHz unless otherwise specified
Usable Frequency Range	800		960	MHz	
Typical Frequency Range		824-849		MHz	
Linear Gain	28	29	31	dB	
Second Harmonic (including second harmonic trap)		-30		dBc	
Max CW Output Power		31.5		dBm	
Total Efficiency (AMPS mode)		50		%	
Maximum Linear Output Power (CDMA Modulation)		29		dBm	
Total Linear Efficiency	30	35		%	
Adjacent Channel Power Rejection		-46	-44	dBc	ACPR @ 885kHz
		-58	-56	dBc	ACPR @1980kHz
Noise Power		-90	-89	dBm	V_{CC}=3.4V; BW=30kHz; RX Band NF measure from TX center band to RX center band.
Maximum Linear Output Power (CDMA Modulation)		29		dBm	V_{CC}=3.0V
Total Efficiency (AMPS mode)		50		%	
Max CW Output Power	30	30.5	31	dBm	
Total Linear Efficiency	30	36		%	
Adjacent Channel Power Rejection		-46	-44	dBc	ACPR @ 885kHz
		-58	-56	dBc	ACPR @ 1980kHz
Input VSWR		<2:1			
Output Load VSWR			10:1		No damage.
TDMA					
Linear Output Power		30		dBm	
Linear ACP		-29	-28		30kHZ offset
Linear ALT CP		-49	-48		60kHZ offset
Efficiency	45	46			O/P=30dBm
Power Supply					
Power Supply Voltage	3.0	3.4	4.5	V	
Idle Current		135	200	mA	V_{MODE}=0V to 0.5V
V_{REG} Current		10	15	mA	Total pins 6 and 7, V_{REG}=2.8V
Turn On/Off time			<100	ns	
Total Current (Power down)			10	µA	V_{PD}=Low
V_{REG} "Low" Voltage		0	0.2	V	
V_{REG} "High" Voltage	2.7	2.8	2.9	V	
VMODE Bias Control Voltage Range		0 to 2.5		V	

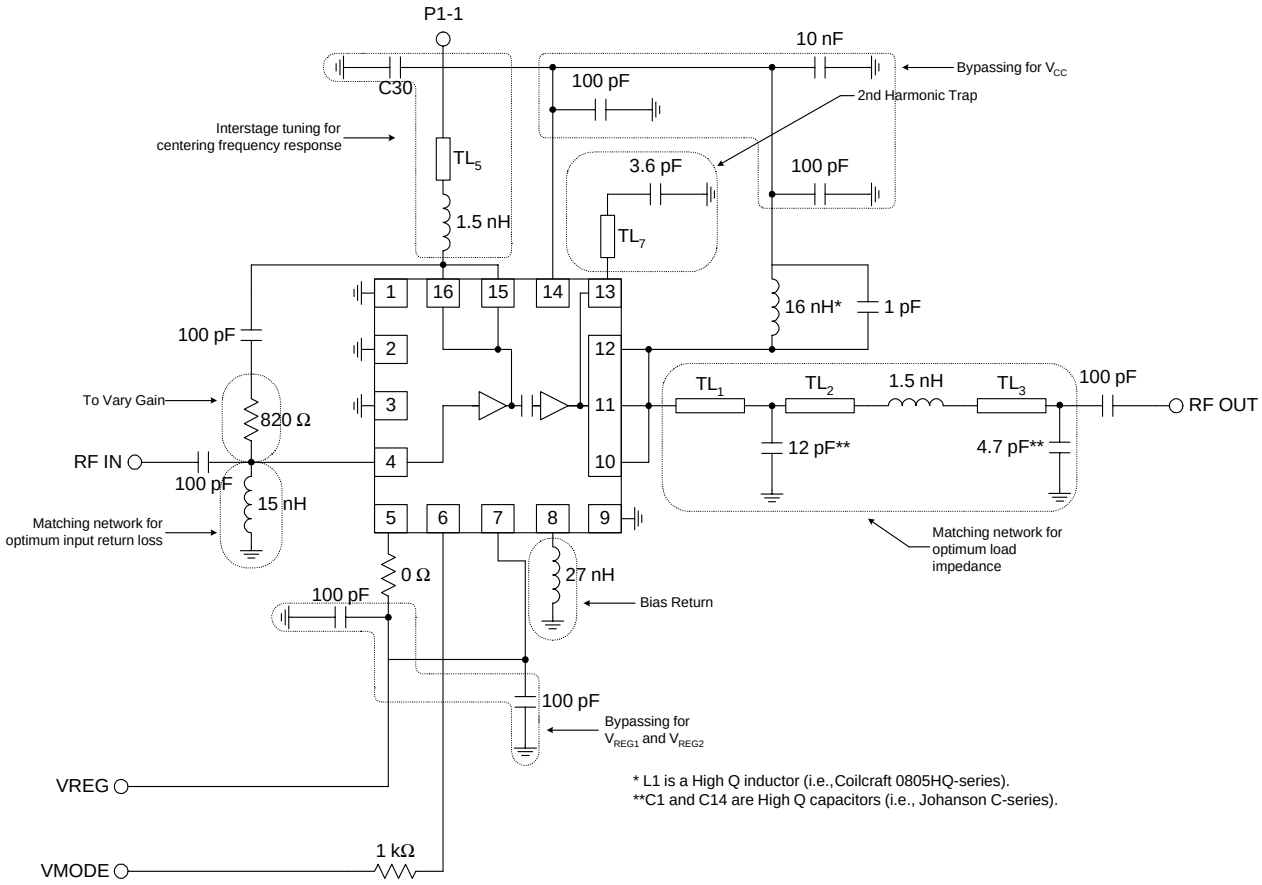
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Connect to package base ground. This ground should be isolated from the backside ground contact on top metal layer.	
2	GND1	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact on top metal layer.	
3	GND1	Same as Pin 2.	
4	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
5	VREG1	Enable voltage for first stage. When this pin is “low”, all circuits are shut off. When this pin is 2.8V, all circuits are operating normally. V_{REG} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 100pF high frequency bypass capacitor is recommended.	
6	VMODE	This is an analog bias current control pin. The range is 0V for minimum bias to 3.0 for maximum bias.	
7	VREG2	Enable voltage for second or output stage. When this pin is “low”, all circuits are shut off. When this pin is 2.8V, all circuits are operating normally. V_{REG} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 100pF high frequency bypass capacitor is recommended.	
8	GND	Bias circuitry ground. See application schematic.	
9	GND	Ground connection. Connect to package base ground. This ground should be isolated from the backside ground contact on top metal layer.	
10	RF OUT	RF output and power supply for the output stage. The bias for the output stage is provided through this pin and pin 13. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT	Same as pin 10.	
13	2FO	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with an on chip capacitor at 2fo is required at this pin.	
14	VCC BIAS	Power supply for bias circuitry. A 100pF high frequency bypass capacitor is recommended.	
15	VCC1	Interstage tuning and bias supply for first stage.	
16	VCC1	Interstage tuning and bias supply for first stage.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic - US CDMA



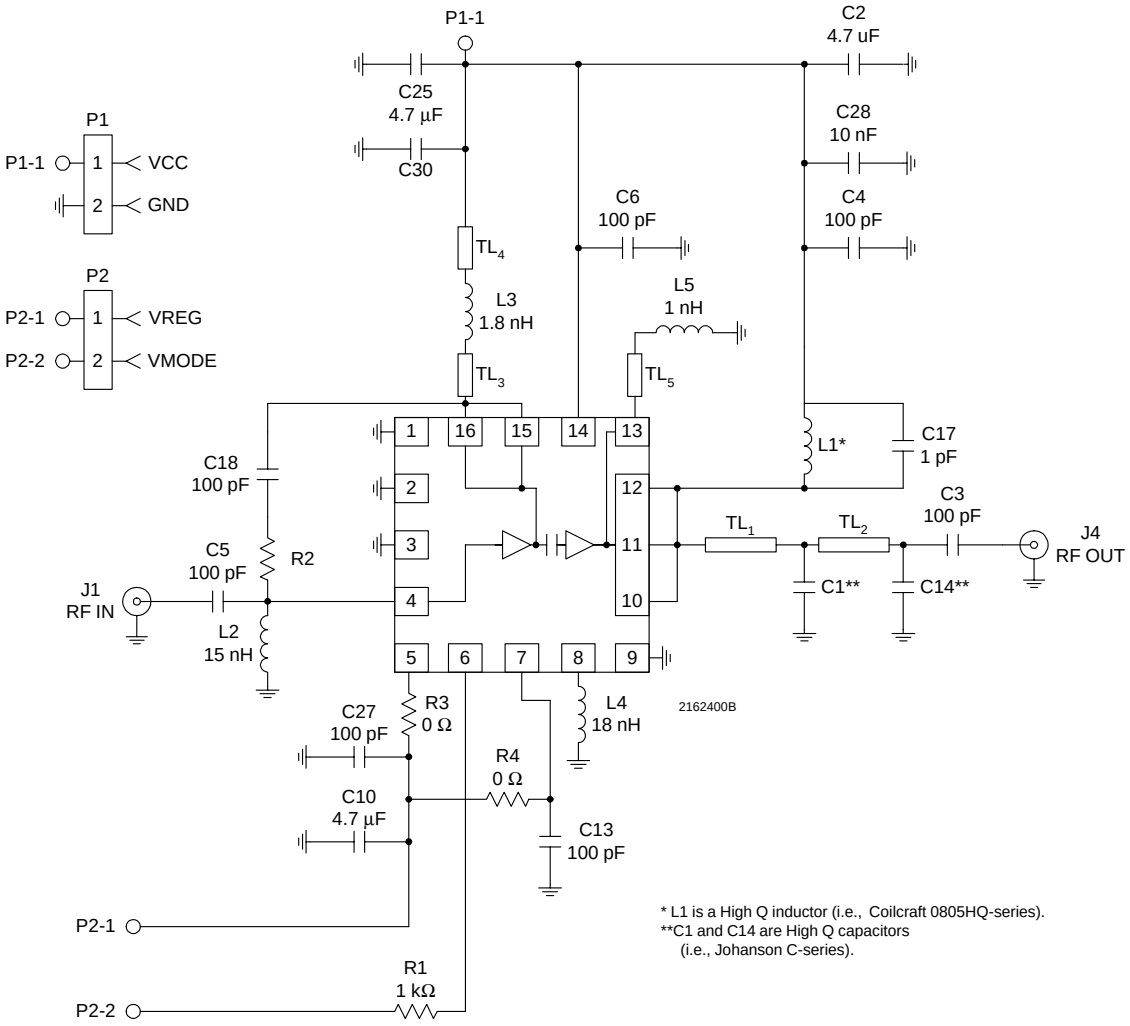
* High Q inductor (i.e., Coilcraft 0805HQ-series).
**High Q capacitors (i.e., Johanson C-series).

Application Schematic - US TDMA



Evaluation Board Schematic - US CDMA

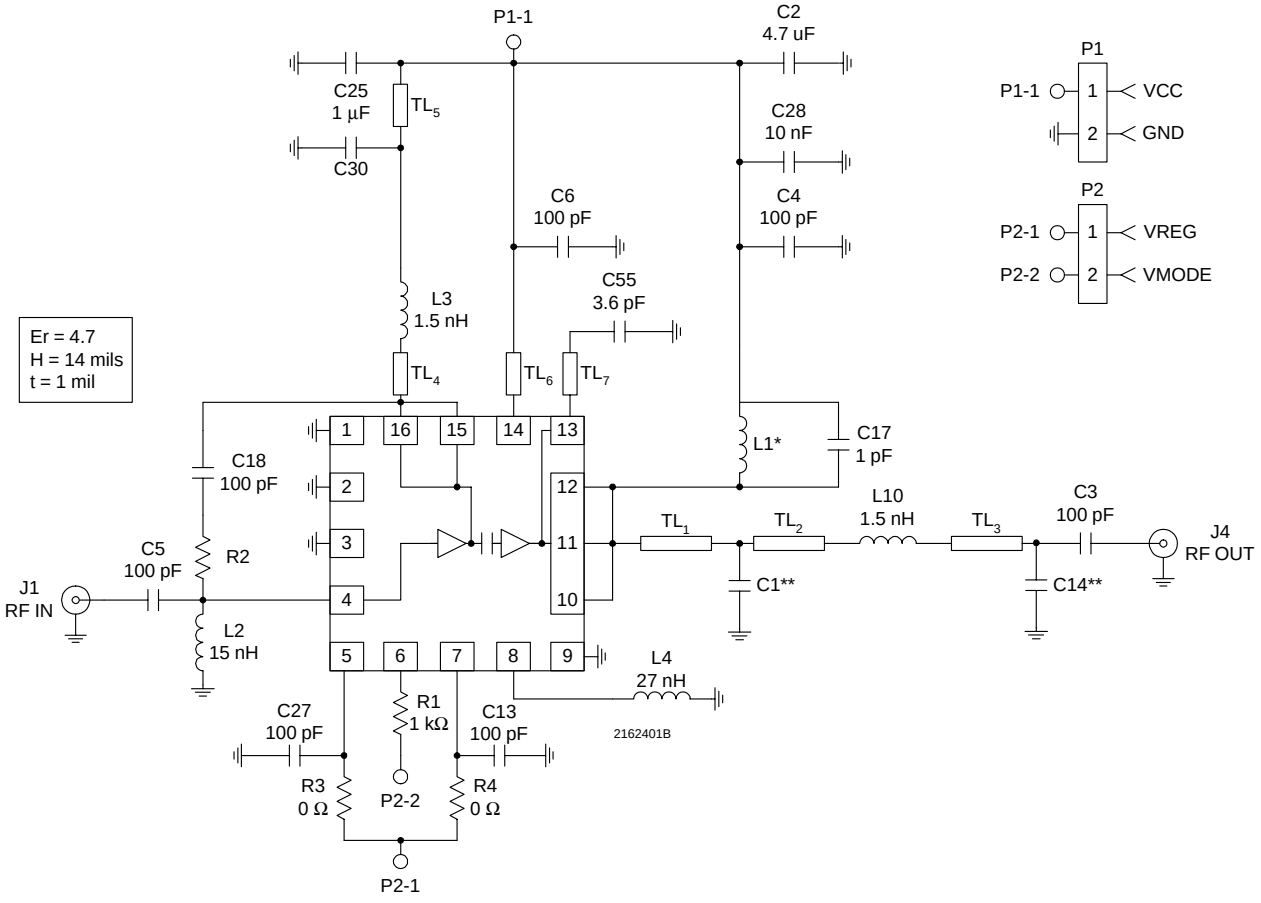
(Download Bill of Materials from www.rfmd.com.)



Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	330	100	9.1	27	5.1

Transmission Line Length	TL_1	TL_2	TL_3	TL_4	TL_5
CDMA (US)	175 mils	165 mils	L=15 mils W=16 mils	L=40-45 mils from L3 W=16 mils	L=15-20 mils W=14 mils

Evaluation Board Schematic - US TDMA

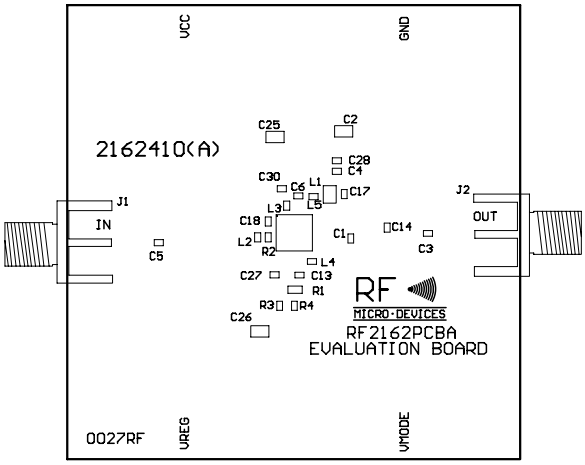


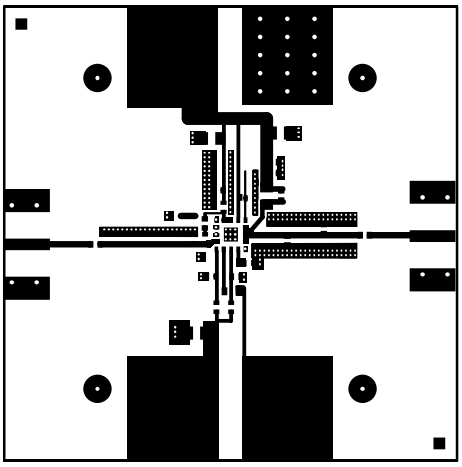
* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors (i.e., Johanson C-series).

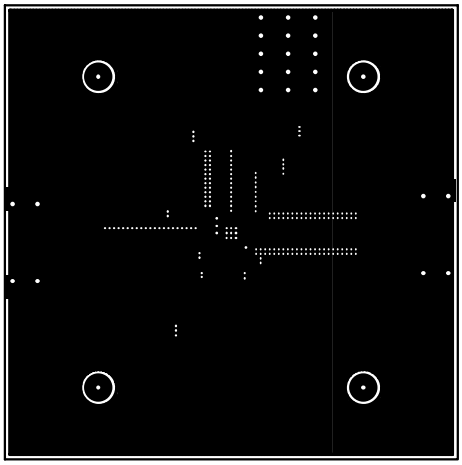
Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
TDMA (US)	820	56	12	16	5.6

Transmission Line Length	TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7
TDMA (US)	90 mils	82 mils	135 mils	L=12 mils W=16 mils	L=49 mils W=16 mils	L=12 mils	L=12 mils W=14 mils

Evaluation Board Layout - CDMA
Board Size 2.0" x 2.0"
Board Thickness 0.031", Board Material FR-4







Evaluation Board Layout - TDMA