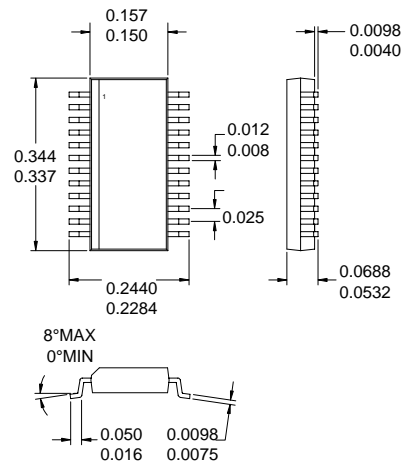


Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode CDMA/AMPS
- Supports Dual-Mode CDMA/TACS
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

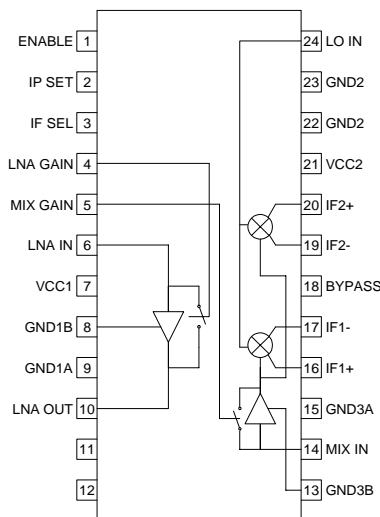
The RF2449 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and downconvert RF signals, while providing 30dB of stepped gain control range. Features include digital control of LNA gain, mixer gain, LNA IIP3, and power down mode. Another feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. The LNA IIP3 can be digitally controlled between two levels to reduce current draw in CDMA standby and other conditions where high IIP3 is not required. Noise Figure, IP3, and other specs are designed to be compatible with the IS-98 specification for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-24.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- | | | |
|--|-----------------------------------|--------------------------------------|
| <input type="checkbox"/> Si BJT | <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET |
| <input checked="" type="checkbox"/> Si Bi-CMOS | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si CMOS |



Functional Block Diagram

Features

- Complete Receiver Front-End
- Stepped LNA/Mixer Gain Control
- Adjustable LNA/Mixer Bias Current
- Adjustable LNA/Mixer IIP3
- Digital LNA IIP3 Control
- Meets IS-98 IMD and Single Tone

Ordering Information

- | | |
|-------------|--|
| RF2449 | CDMA/FM Low Noise Amplifier/Mixer 900MHz Downconverter |
| RF2449 PCBA | Fully Assembled Evaluation Board |

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
<http://www.rfmd.com>

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V _{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



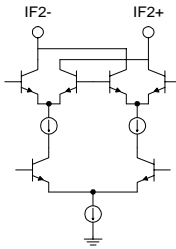
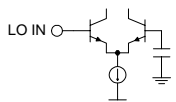
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

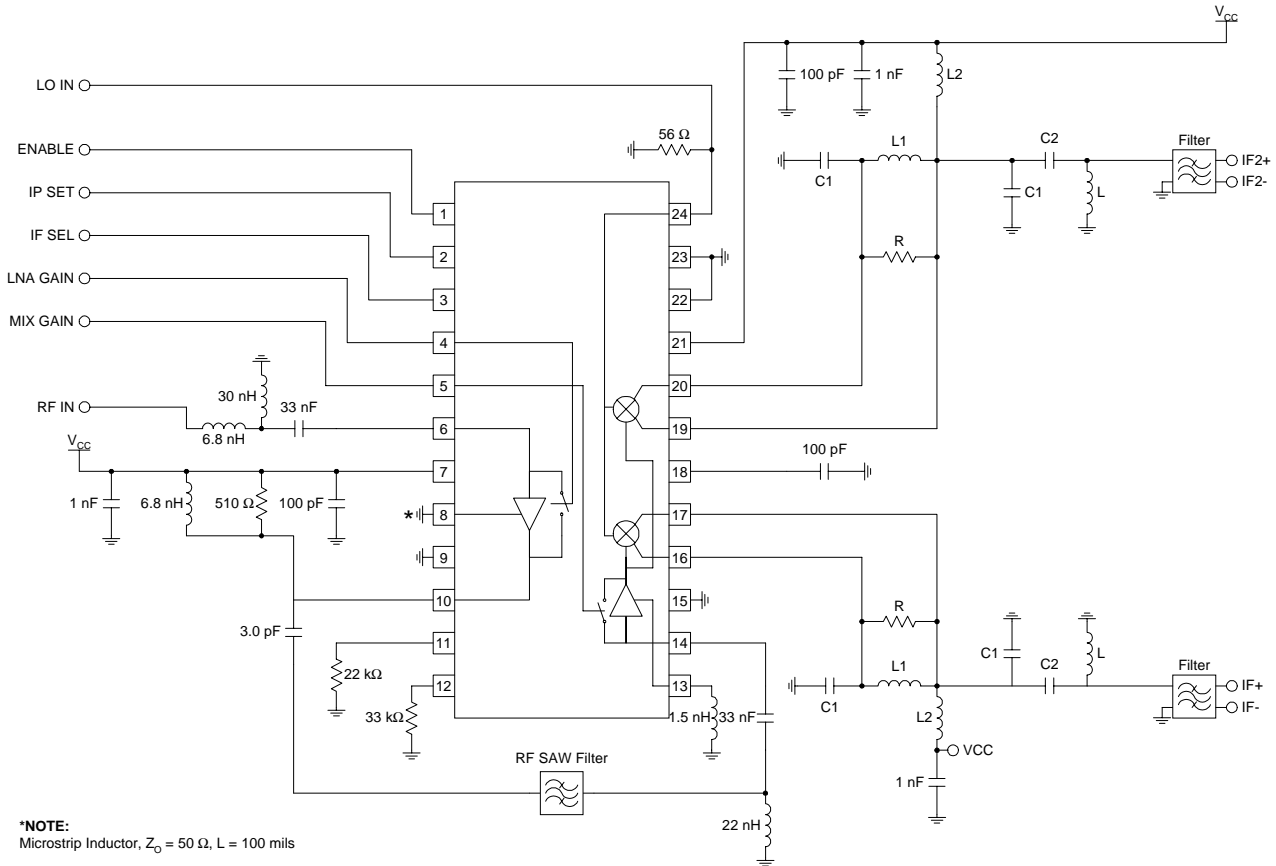
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T = 25°C, V _{CC} =2.75V, RF=880MHz, LO=990MHz @ 0dBm, IF = 110MHz, V _{IPSET} <1.0V
RF Frequency Range		869 to 894		MHz	
LO Frequency Range		760 to 1010		MHz	
IF Frequency Range		0.1 to 250		MHz	
LNA - High Gain Mode					
Gain	14	15		dB	IIP3 is adjustable.
Noise Figure		2.3	2.5	dB	
IIP3		+6		dBm	
LNA Out to Mixer in Isolation		40		dB	
Current		3.5		mA	
LNA Bypass					
Gain		-6.3		dB	
Noise Figure		6.3		dB	
IIP3		20		dBm	
Current		0		mA	
Mixer - High Gain Mode					3kΩ balanced load.
Gain	12	13		dB	IIP3 is adjustable - See Data Plots.
Noise Figure		6.5	7.5	dB	
IIP3	+2	+3		dBm	
RF to IF Isolation	29			dB	
Current		21		mA	
Mixer - Low Gain Mode					3kΩ balanced load.
Gain	3	4		dB	IIP3 is adjustable - See Data Plots.
Noise Figure		13	14	dB	
IIP3	+12	+13		dBm	
RF to IF Isolation	35.5			dB	
Current		16		mA	
Local Oscillator Input					
Input Level	-10	-3	0	dBm	Any gain state.
LO to IF Isolation	40			dB	
LO to RF Isolation	40			dB	
LO to LNA Input Isolation	35			dB	
Cascade (Mode 1)					(LNA Gain High, Mix Gain High) With -3dB image rejection filter.
Gain	24	25	27	dB	3kΩ balanced IF load. Single sideband.
Noise Figure		2.9		dB	
IIP3	-10	-9		dBm	
Cascade (Mode 2)					(LNA Gain High, Mix Gain Low) With -3dB image rejection filter.
Gain		16.0		dB	3kΩ balanced IF load. Single sideband.
Noise Figure		4.7		dB	
IIP3		0		dBm	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Cascade (Mode 3) Gain Noise Figure IIP3		3.5 16 +11.8		dB dB dBm	(LNA Gain Low, Mix Gain High) With -3dB image rejection filter. 3k Ω balanced IF load. Single sideband.
Cascade (Mode 4) Gain Noise Figure IIP3		-5 22.5 +18.0		dB dB dBm	(LNA Gain Low, Mix Gain Low) With -3dB image rejection filter. 3k Ω balanced IF load. Single sideband.
Power Supply Voltage Power Down Current	2.65	2.75	3.9	V μ A	Enable < 1.0V

Pin	Function	Description	Interface Schematic
1	ENABLE	This pin is used to enable or disable the RF2449. A logic high (>2.0V) enables the circuitry. A logic low (<1.0V) disables the circuitry.	
2	IP SET	Controls the setting of the LNA current. A logic low (<1.0V) selects the internal resistance (49.5kΩ), resulting in an LNA current of 3.5mA. A logic high (>2.0V) selects the external resistance at pin 12.	
3	IF SEL	Determines which IF port is active. A logic low (<1.0V) activates IF1 and deactivates IF2. A logic high (>2.0V) activates IF2 and deactivates IF1.	
4	LNA GAIN	Controls the bypass feature of the LNA. A logic low (<1.0V) selects the bypass mode. A logic high (>2.0V) turns on the LNA.	
5	MIX GAIN	Controls the bypass feature of the mixer pre-amp. A logic low (<1.0V) selects the bypass mode. A logic high (>2.0V) turns on the pre-amp.	
6	LNA IN	LNA input pin.	
7	VCC1	VCC pin for all circuits except the LO.	
8	GND1B	LNA ground pin.	See pin 6.
9	GND1A	Package ground pin.	
10	LNA OUT	LNA output pin.	See pin 6.
11	ISET2	An external resistor connected to this pin sets the current of the pre-amp and the mixer.	
12	ISET1	An external resistor connected to this pin sets the current of the LNA when IP SET is high (see pin 2).	
13	GND3B	Ground pin for pre-amp circuit.	
14	MIX IN	Mixer pre-amp input pin.	See pin 13.
15	GND3A	Ground pin for the mixer circuits.	
16	IF1+	First differential output pin for the first mixer.	

Pin	Function	Description	Interface Schematic
17	IF1-	Second differential output pin for the first mixer.	See pin 16.
18	BYPASS	Bypass pin for the LO bias reference.	
19	IF2+	First differential output pin for the second mixer.	
20	IF2-	Second differential output pin for the second mixer.	See pin 20.
21	VCC2	VCC pin for the LO circuits.	
22	GND2	Ground pin for the LO circuits.	
23	GND2	Ground pin for the LO circuits.	
24	LO IN	Local oscillator input pin.	

Application Schematic



***NOTE:**
Microstrip Inductor, $Z_0 = 50 \Omega$, $L = 100$ mils
Suggested component values for 85.38 MHz IF and $R_{OUT} = 1 \text{ k}\Omega$:
 $L1 = 470 \text{ nH}$ $C1 = 10 \text{ pF}$ $R = 7.5 \text{ k}\Omega$

Output Interface Network

$L1$, $C1$ and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi \sqrt{\frac{L1}{2}(C1 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 16 and 17. An average value to use for C_{EQ} is 2.5pF.

R may then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_p} \right)^{-1}$$

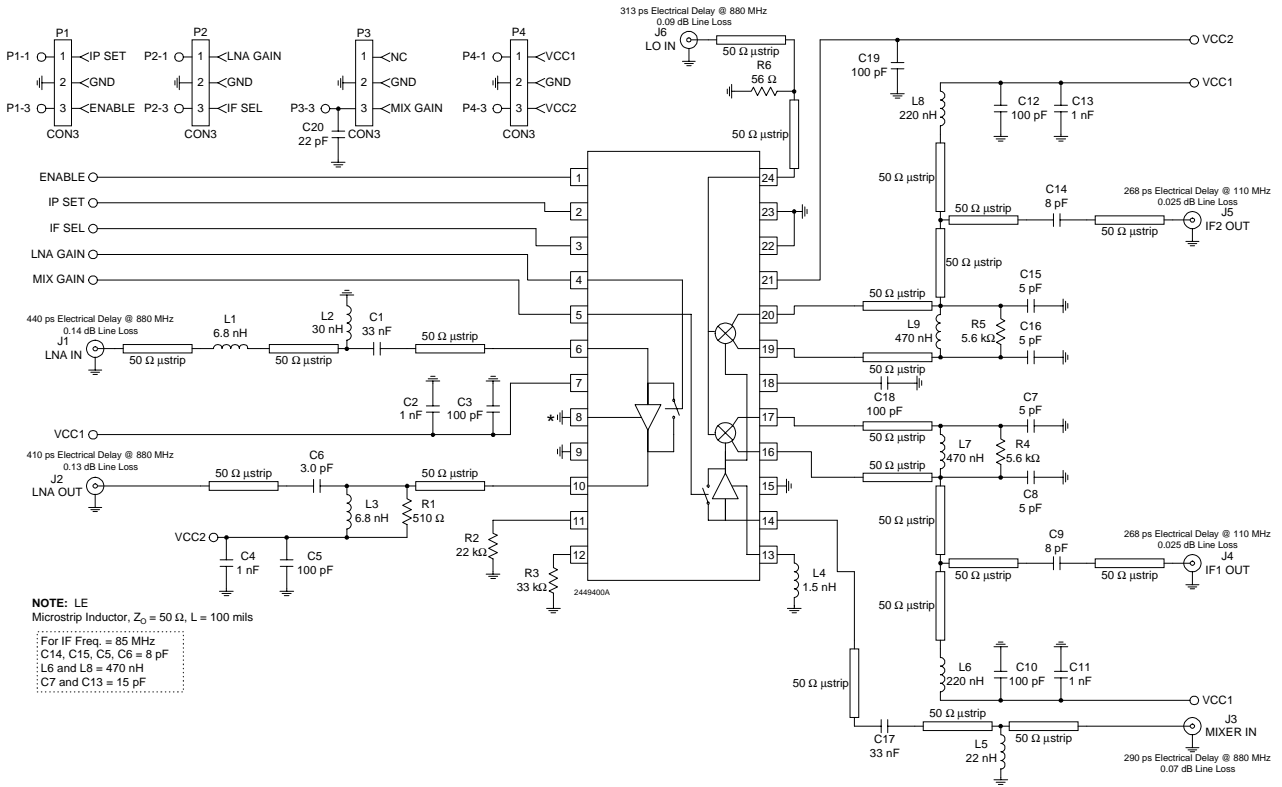
where R_{OUT} is the desired output impedance and R_p is the parasitic equivalent parallel resistance of $L1$.

$C1$ should be chosen as high as possible, while maintaining an R_p of $L1$ that allows for the desired R_{OUT} .

$L2$ and $C2$ serve dual purposes. $L2$ serves as an output bias choke, and $C2$ serves as a series DC block.

In addition, $L2$ and $C2$ may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to R_{OUT} . Otherwise, $L2$ is chosen to be large and $C2$ is chosen to be large if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.

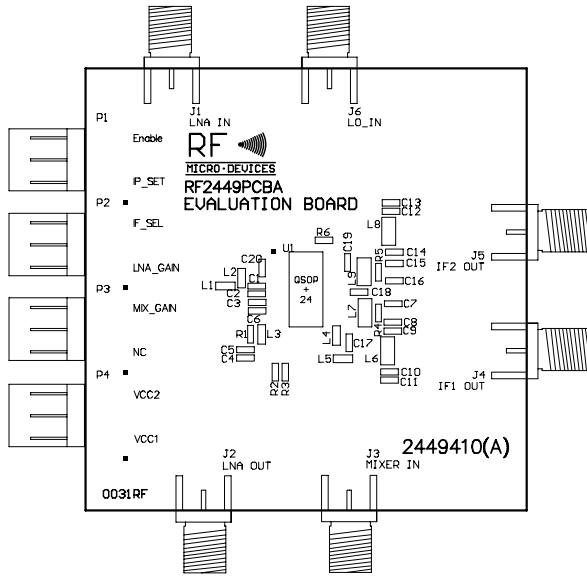
Evaluation Board Schematic (Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)



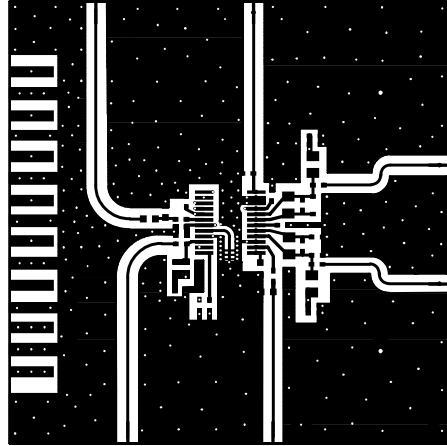
Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.040", Board Material FR-4, Multi-Layer

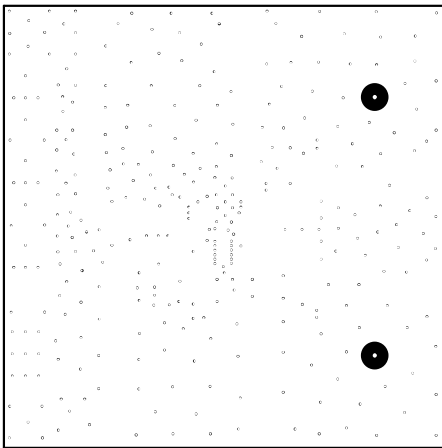
Assembly



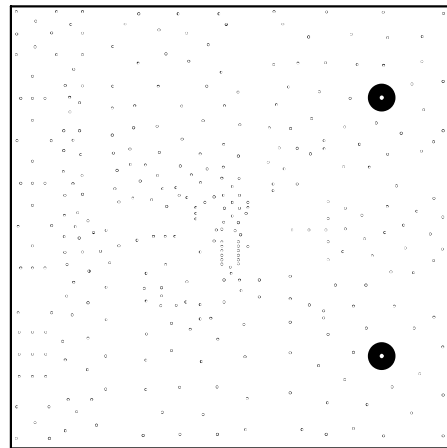
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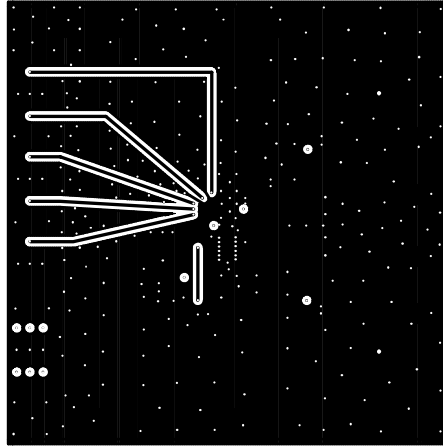
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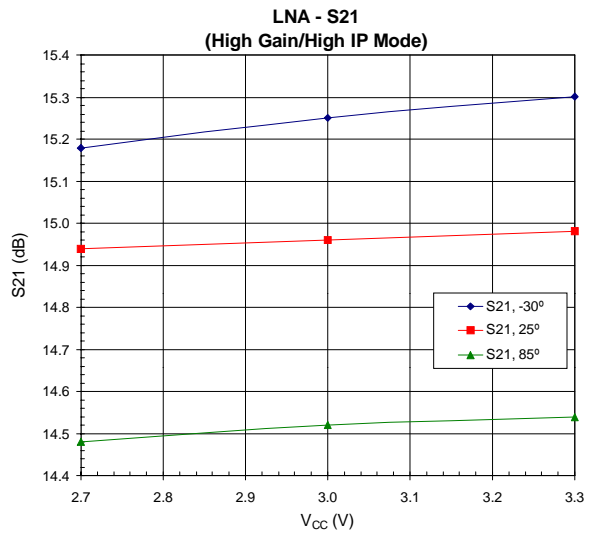
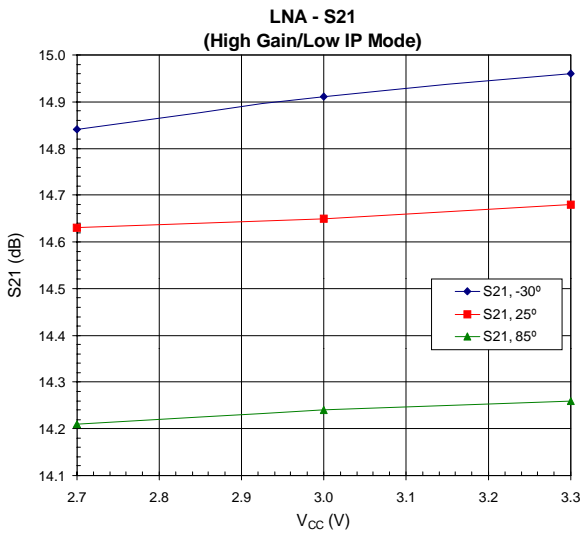
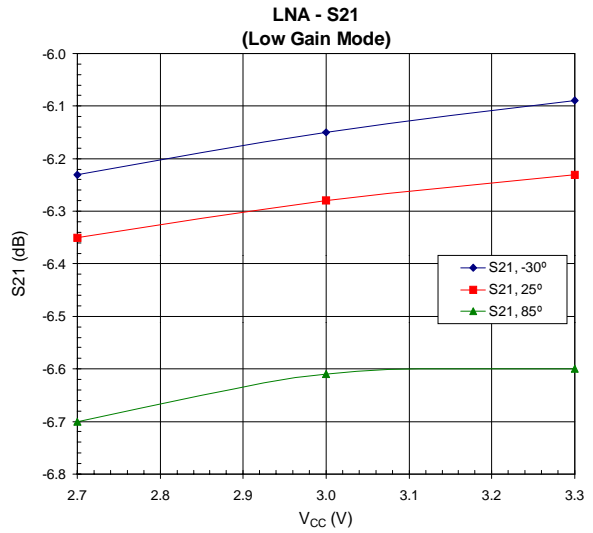
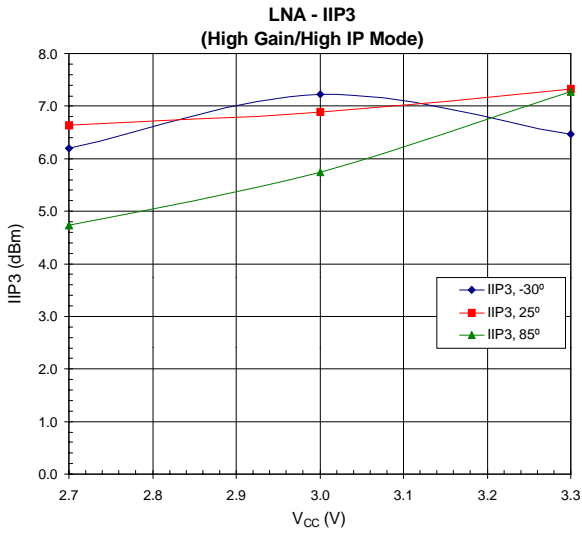
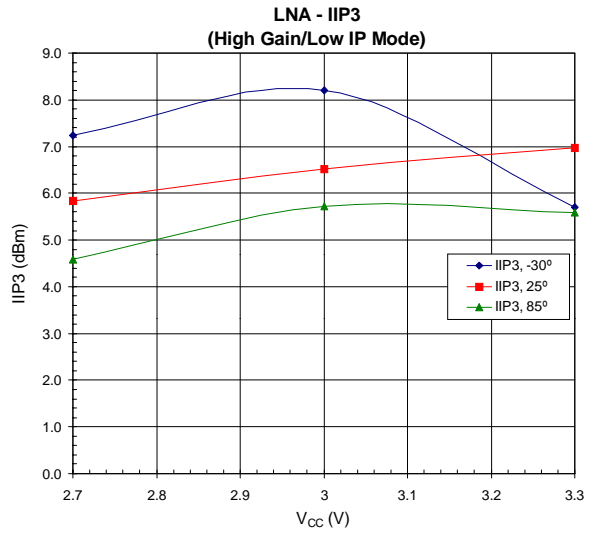
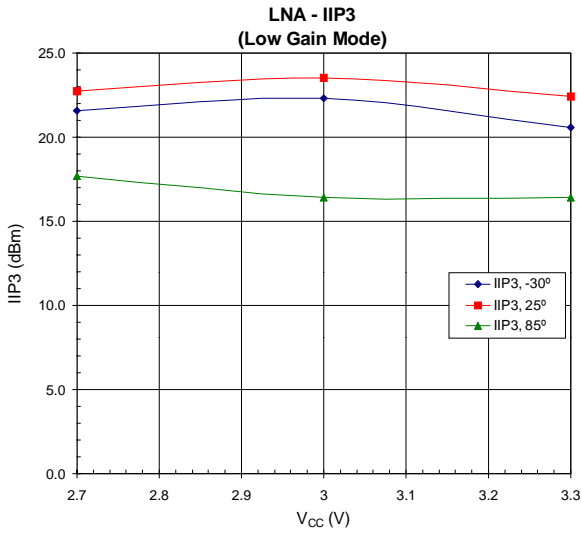


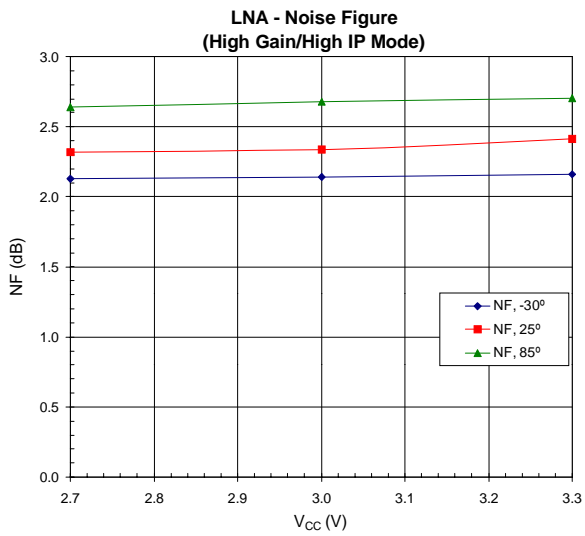
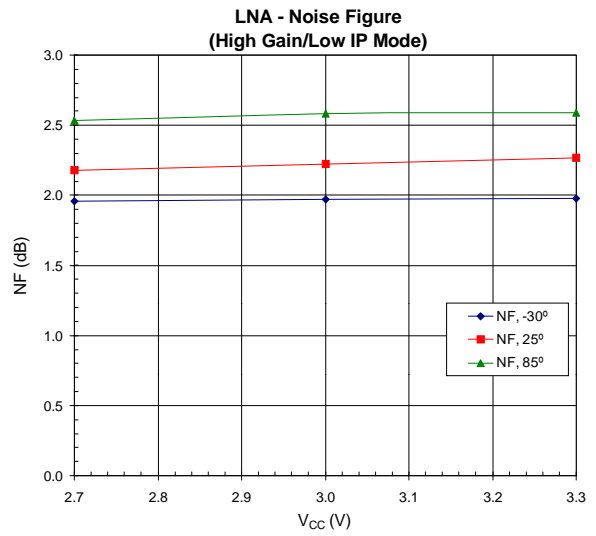
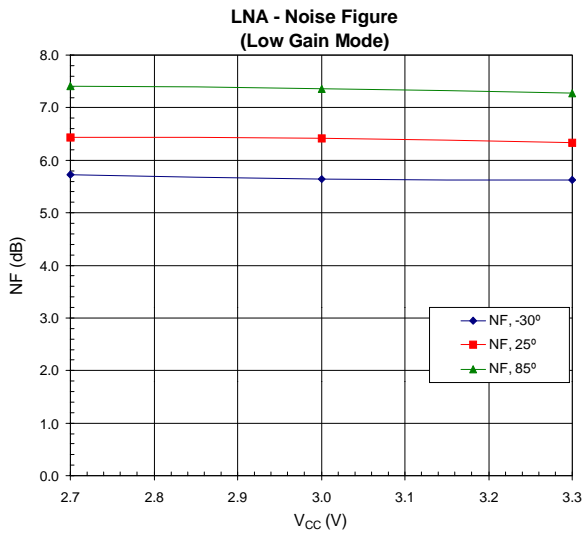
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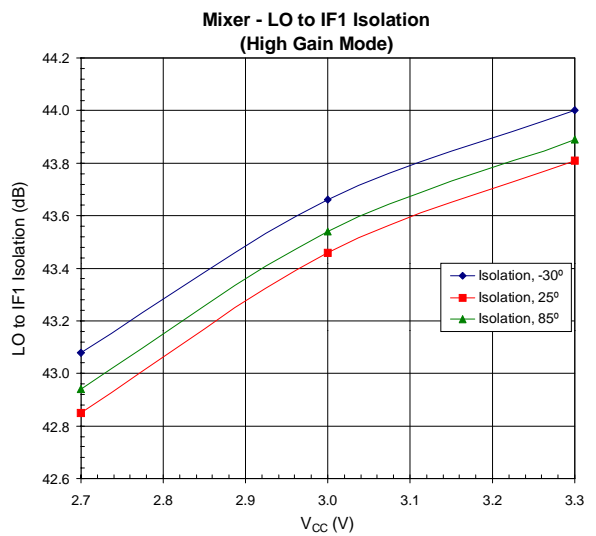
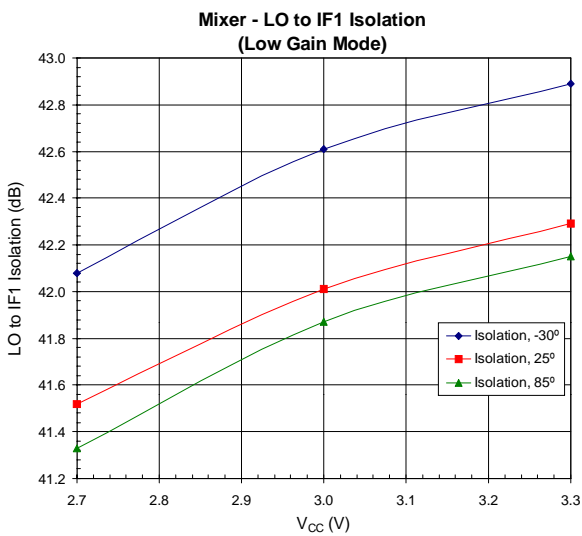
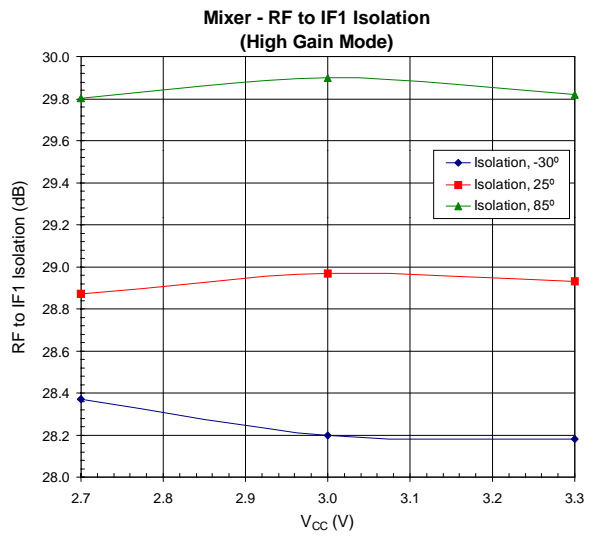
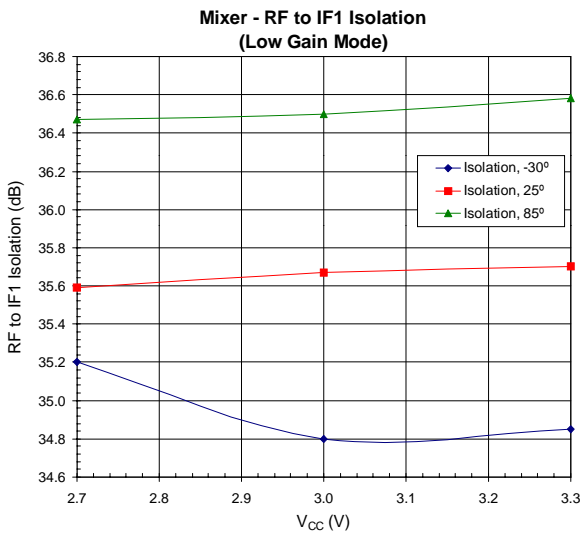
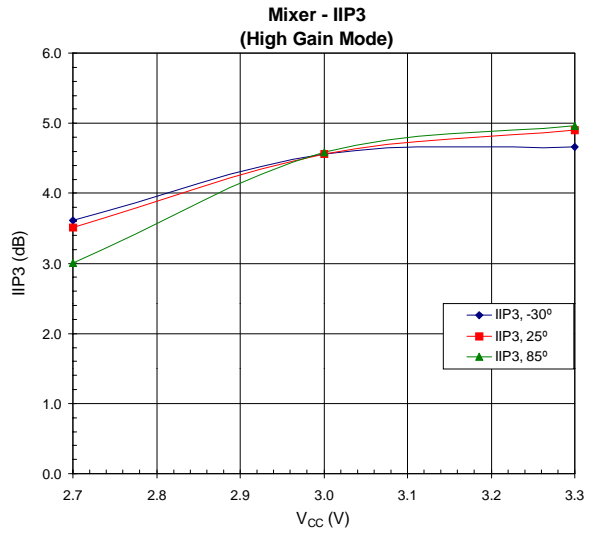
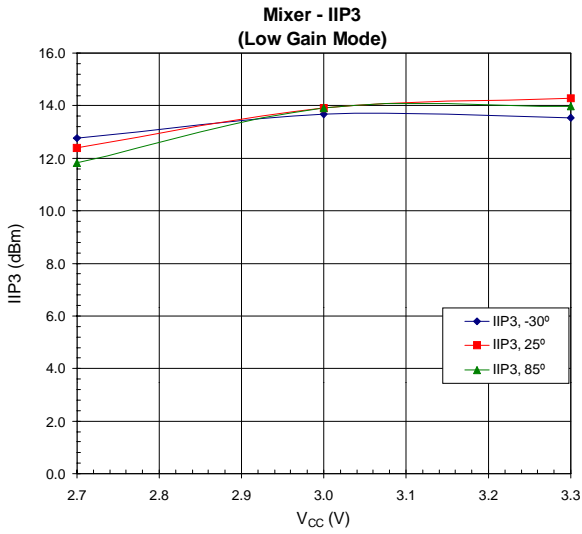


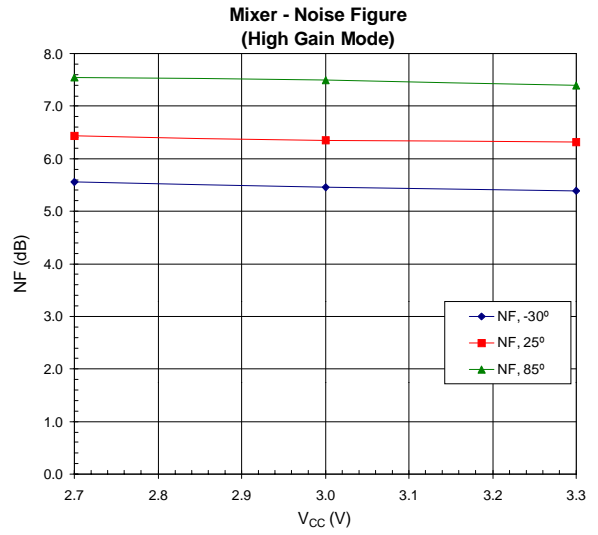
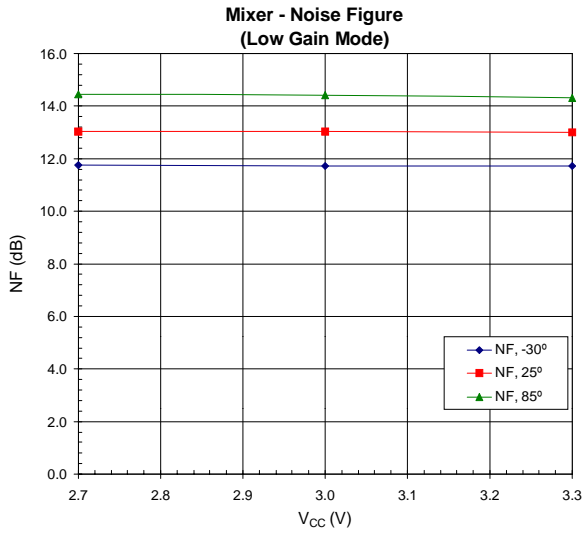
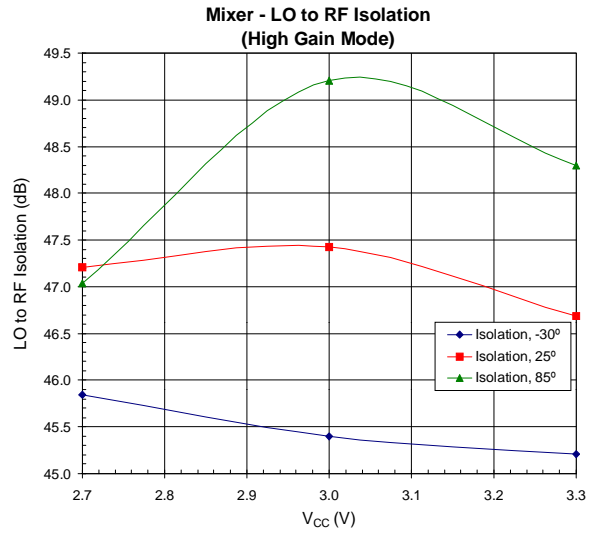
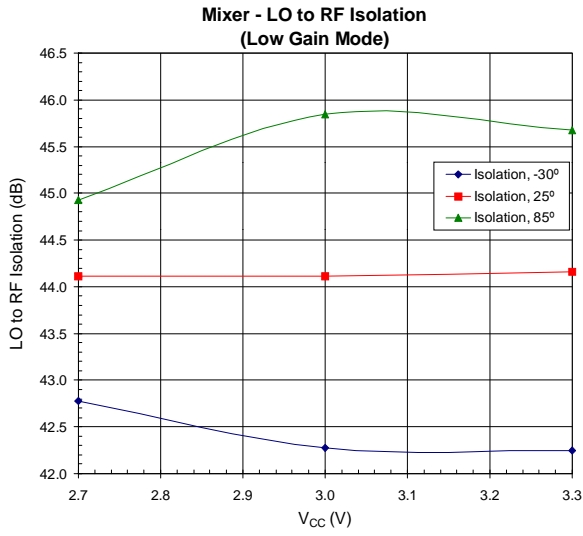
Back











RF2449

Preliminary

∞

FRONT-ENDS