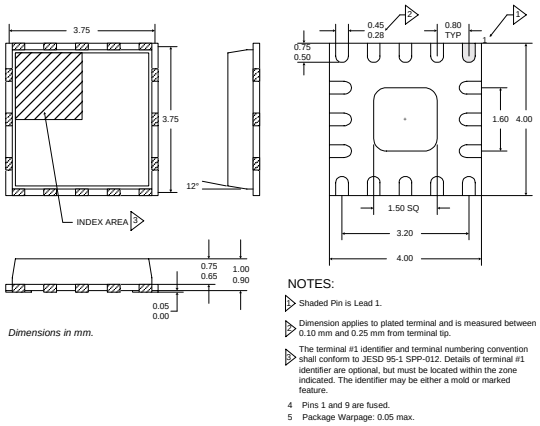
Typical Applications

- Dual-Band CDMA Base Stations
- TDMA/TDMA-EDGE Base Stations
- GSM-EDGE/EGSM Base Stations
- W-CDMA Base Stations
- WLAN and WLL Systems
- GMSK, QPSK, DQPSK, QAM Modulation

Product Description

The RF2484 is a monolithic integrated quadrature modulator IC capable of universal direct modulation for high-frequency AM, PM, or compound carriers. This low-cost IC features excellent linearity, noise floor, and over-temperature carrier suppression performance. The device implements differential amplifiers for the modulation inputs, 90° carrier phase shift network, carrier limiting amplifiers, two matched double-balanced mixers, summing amplifier, and an output RF amplifier which will drive 50Ω from 800MHz to 2500MHz. It is packaged in a small industry-standard LCC 16-pin plastic package.

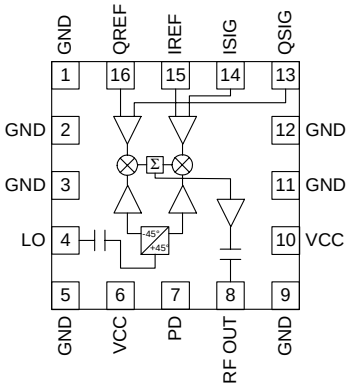


Dimensions in mm.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: LCC, 16-Pin



Functional Block Diagram

Features

- Typical Carrier Suppression >35dBc, Sideband Suppression >35dBc over temperature with highly linear operation
- Noise Floor better than -152dBm/Hz from 800MHz to 2200MHz
- Single 5V Power Supply

Ordering Information

RF2484	Direct Quadrature Modulator
RF2484 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

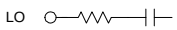
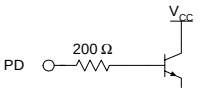
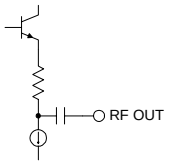
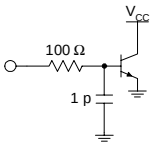
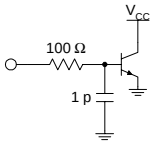
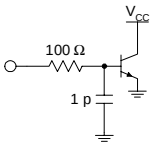
Absolute Maximum Ratings

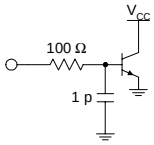
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Input LO and RF Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

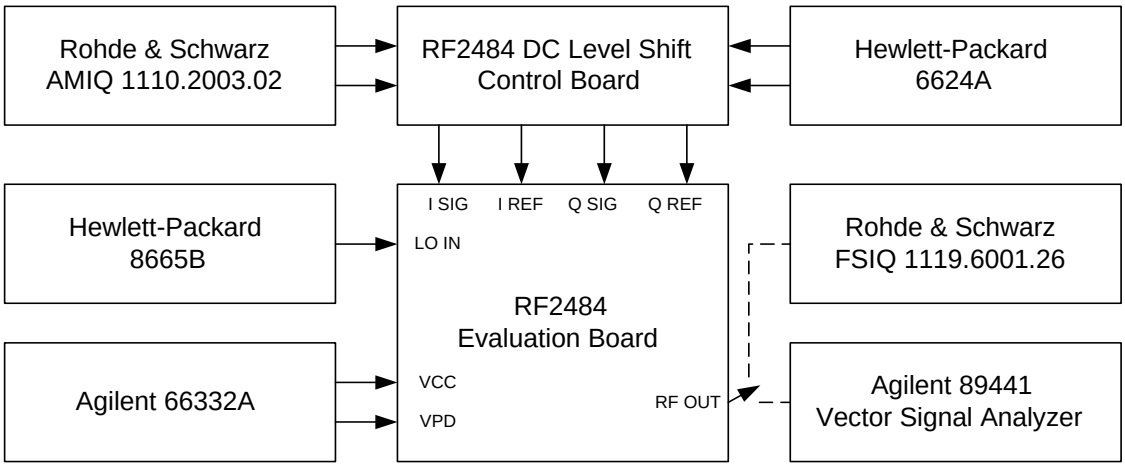
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LO Input					T=25°C, V_{CC}=5V, V_{REF}=4.1V; I and Q driven single-ended
Frequency Range	800		2500	MHz	
Power Level	-6		+6	dBm	
Input Impedance		45-j95		Ω	At 880MHz
		52-j54		Ω	At 1960MHz
		58-j50		Ω	At 2140MHz
		63-j40		Ω	At 2400MHz
Modulation Input					
Frequency Range	DC		250	MHz	
Reference Voltage (V_{REF})		4.1		V	
Input Resistance		30		kΩ	
Input Bias Current			40	µA	
RF Output (880MHz)					LO= -5dBm at 880MHz; Single sideband testing unless otherwise noted
CDMA Output Channel Power		-12		dBm	For ACPR=-72dBc; I&Q Amplitude=1.1V_{PP} (single-ended)
CDMA ACPR		-72		dBc	Channel Power=-12dBm; see Test Setup for detailed information
Carrier Suppression	50			dBc	T=25°C; P_{OUT}=-10dBm; optimized I,Q DC offsets
Carrier Suppression over Temperature	35			dBc	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-10dBm
Sideband Suppression	50			dBc	T=25°C; P_{OUT}=-10dBm; optimized I,Q amplitude and phase balance
Sideband Suppression over Temperature	35			dBc	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-10dBm
Broadband Noise Floor		-152.5		dBm/Hz	At 20MHz offset, 30kHz res BW, V_{CC}=5V; ISIG, QSIG, IREF, and QREF tied to V_{REF}
EVM		2.3		%	See Test Setup for detailed information
Phase Error		1		° RMS	See Test Setup for detailed information
Rho		.9993			See Test Setup for detailed information
Output Impedance		28-j72		Ω	
RF Output (1960MHz)					LO=-5dBm at 1960MHz; Single sideband testing unless otherwise noted
PCS CDMA Output Power		-13		dBm	For ACPR=-72dBc; I&Q Amplitude=1.2V_{PP} (single-ended)
PCS CDMA ACPR		-72		dBc	Channel Power=-13dBm; see Test Setup for detailed information
Carrier Suppression	50			dBc	T=25°C; P_{OUT}=-13dBm; optimized I,Q DC offsets
Carrier Suppression over Temperature	35			dBc	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-13dBm
Sideband Suppression	50			dBc	T=25°C; P_{OUT}=-13dBm; optimized I,Q amplitude and phase balance
Sideband Suppression over Temperature	35			dBc	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-13dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Output (1960MHz) cont'd					
Broadband Noise Floor		-154.5		dBm/Hz	At 20MHz offset, 30kHz res BW, V_{CC}=5V; ISIG, QSIG, IREF, and QREF tied to V_{REF}
EVM		2.3		%	See Test Setup for detailed information
Phase Error		1		° RMS	See Test Setup for detailed information
Rho		.9988			See Test Setup for detailed information
Output Impedance		46-j22		Ω	
RF Output (2140MHz)					LO= -5dBm at 2140MHz; Single sideband testing unless otherwise noted
W-CDMA Output Channel Power		-16		dBm	For ACPR=-60dBc; I&Q Amplitude=1.4V_{PP} (single-ended)
W-CDMA ACPR		-60		dBc	Channel Power=-16dBm; see Test Setup for detailed information
Carrier Suppression	50			dBc	T=25°C; P_{OUT}=-13dBm; optimized I,Q DC offsets
Carrier Suppression over Temperature	35			dBc	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-13dBm
Sideband Suppression	50			dBc	T=25°C; P_{OUT}=-13dBm; optimized I,Q amplitude and phase balance
Sideband Suppression over Temperature	35			dBc	Temperature cycled from -40°C to +85°C after optimization at T=25°C; P_{OUT}=-13dBm
Broadband Noise Floor		-152		dBm/Hz	At 20MHz offset, 30kHz res BW, V_{CC}=5V; ISIG, QSIG, IREF, and QREF tied to V_{REF}
EVM		5.9		%	See Test Setup for detailed information
Phase Error		2.4		° RMS	See Test Setup for detailed information
Rho		.9961			See Test Setup for detailed information
Output Impedance		58-j16		Ω	
Power Down					
Turn On/Off Time			100	ns	
PD Input Resistance	50			kΩ	
Power Control "ON"			2.8	V	Threshold voltage
Power Control "OFF"	1.0	1.2		V	Threshold voltage
Power Supply					
Voltage		5.0		V	Specifications
	4.5		6.0	V	Operating Limits
Current		66	70	mA	
			25	µA	Power Down

Pin	Function	Description	Interface Schematic
1	GND	Ground connection. This pin should be connected directly to the ground plane.	
2	GND	Same as pin 1.	
3	GND	Same as pin 1.	
4	LO	The input of the phase shifting network. This pin has an internal DC blocking capacitor. This port is voltage-driven so matching at different frequencies is generally not required.	
5	GND	Same as pin 1.	
6	VCC	Power supply. An external capacitor is needed if no other low frequency bypass capacitor is nearby.	
7	PD	Power Down control. When this pin is "low," all circuits are shut off. A "low" is typically 1.2V or less at room temperature.When this pin is "high" (V_{CC}), all circuits are operating normally. If PD is below V_{CC}, output power and performance will be degraded. Operating in this region is not recommended, although it might be useful in some applications where power control is required.	
8	RF OUT	RF Output. This pin has an internal DC blocking capacitor. At some frequencies, external matching may be needed to optimize output power. A small amount of DC current may be present at this output. As a result, if the voltage at this pin is measured using a high impedance probe, some DC voltage may be observed at this output.	
9	GND	Same as pin 1.	
10	VCC	Same as pin 6.	
11	GND	Same as pin 1.	
12	GND	Same as pin 1.	
13	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. The input drive level determines output power and linearity performance; for better carrier suppression, sideband suppression, and dynamic range, the drive level should be as high as possible to meet the required linearity performance. The recommended DC level for this pin is 4.1V. For optimum carrier suppression, the DC voltages on I REF, Q REF, I SIG and Q SIG should be adjusted slightly to compensate for inherent undesired internal DC offsets; for optimum sideband suppression, phase and signal amplitude on IREF, Q REF, I SIG and Q SIG should be adjusted slightly to compensate for inherent undesired internal offsets. See RFMD AN0001 for more detail.	
14	I SIG	Baseband input to the I mixer. This pin is DC coupled. The input drive level determines output power and linearity performance; for better carrier suppression, sideband suppression, and dynamic range, the drive level should be as high as possible to meet the required linearity performance. The recommended DC level for this pin is 4.1V; see pin 13 for more information.	
15	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. A voltage of 4.1V is recommended; see pin 13 for more information. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a differential mode. This will increase the gain.	

Pin	Function	Description	Interface Schematic
16	**Q REF**	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. A voltage of 4.1V is recommended; see pin 13 for more information.	
Pkg Base	**GND**	Ground connection. The package base should be connected to the ground plane.	

CDMA/W-CDMA Test Setup



General

The above setup was used to evaluate the RF2484 under CDMA and W-CDMA modulation conditions. Due to test equipment limitations, a DC-level shifting board was required to provide the appropriate DC reference voltage (4.1V) for the I and Q pins. I and Q were driven single-endedly; differential drive may improve performance. A PC-controlled Rohde & Schwarz AMIQ generated the CDMA I and Q signals. In order to reduce AMIQ noise contributions to adjacent channel power, W-CDMA baseband signals were filtered using a high order low pass filter before application to the RF2484.

EVM, Phase Error, and Rho

To measure EVM, phase error, and Rho, signals were generated using the AMIQ and decoded with the Agilent VSA. For CDMA Cellular and PCS, I and Q input signals were generated with the Pilot Channel active, 32x oversampling and base station equifilters. For W-CDMA, the Common Pilot Channel was active with 8x oversampling and a root cosine filter. In all cases, relative signal amplitude levels were adjusted to optimize signal quality.

CDMA Modulation Setup (Cellular and PCS)

To measure ACPR, I and Q input signals were generated using the following settings:

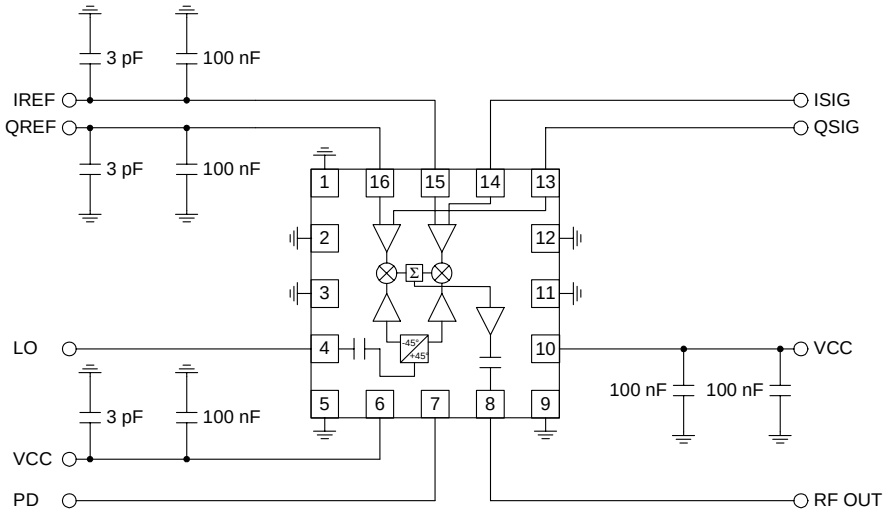
- Pilot Channel active
- Sync Channel active
- Paging Channel active
- 6 Traffic Channels active
- 32x Oversampling
- Base Station equifilter

W-CDMA Modulation Setup

To measure W-CDMA ACPR, I and Q input signals were generated using the following settings in the AMIQ:

- P-CPICH (Common Pilot Channel) active
- P-SCH (Sync Channel) active
- P-CCPCH (Primary Common Control Physical Channel) active
- P-ICH (Page Indicator Channel) Active
- DL-DPCCH (Dedicated Physical Control Channel) active
- 6 DPCH (Dedicated Physical Channels) active
- 8x Oversampling

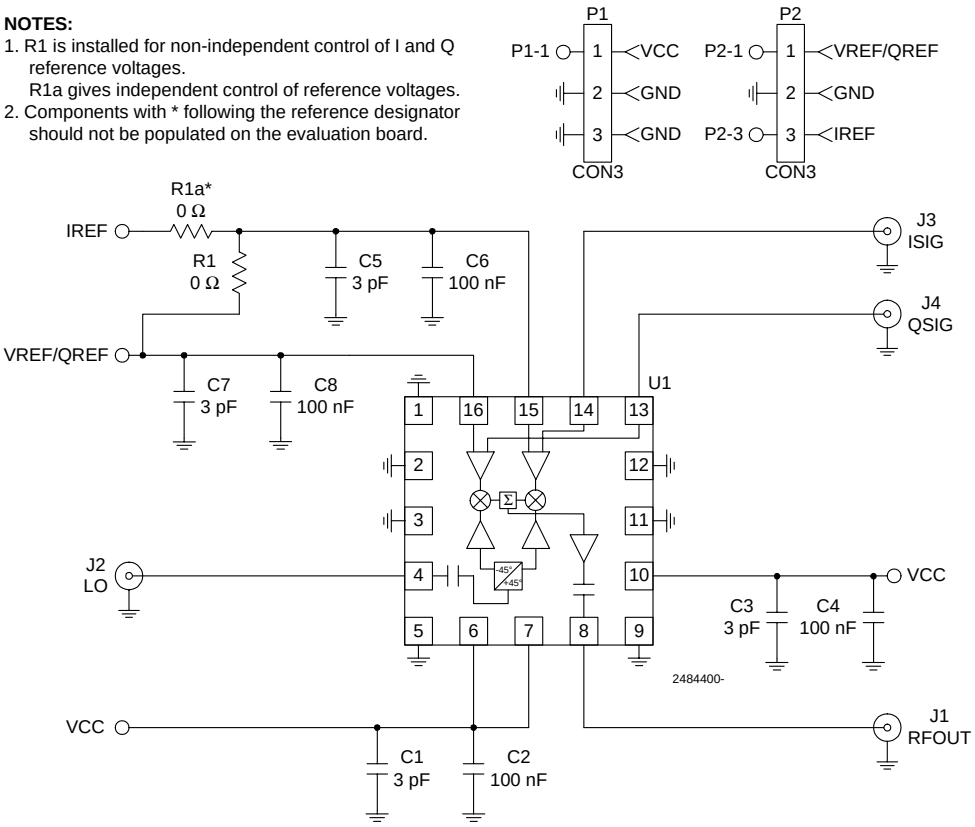
Application Schematic



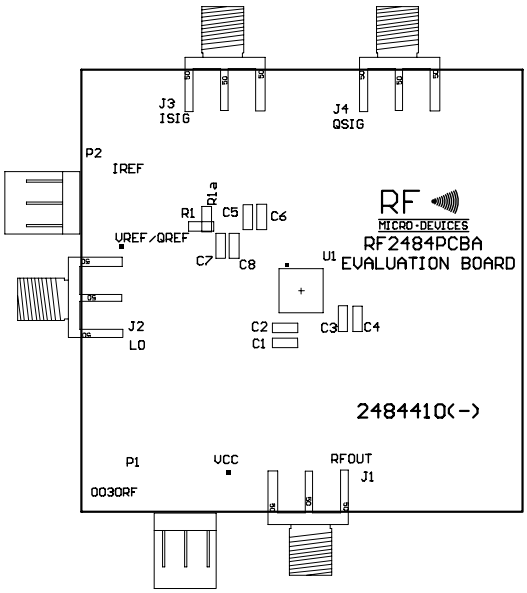
Evaluation Board Schematic

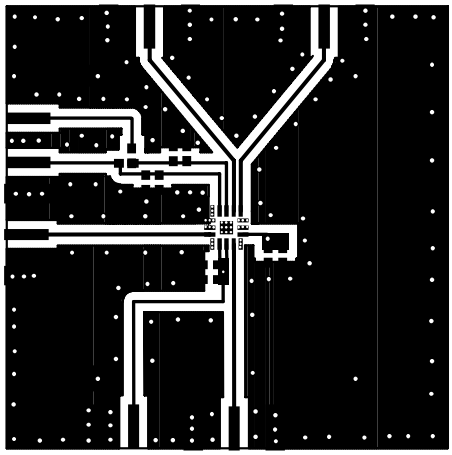
(Download Bill of Materials from www.rfmd.com.)

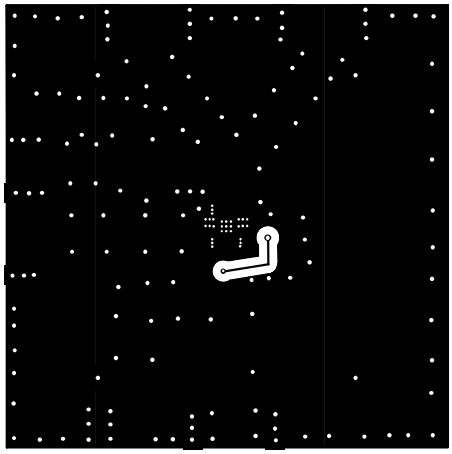
NOTES:
1. R1 is installed for non-independent control of I and Q reference voltages.
   R1a gives independent control of reference voltages.
2. Components with * following the reference designator should not be populated on the evaluation board.



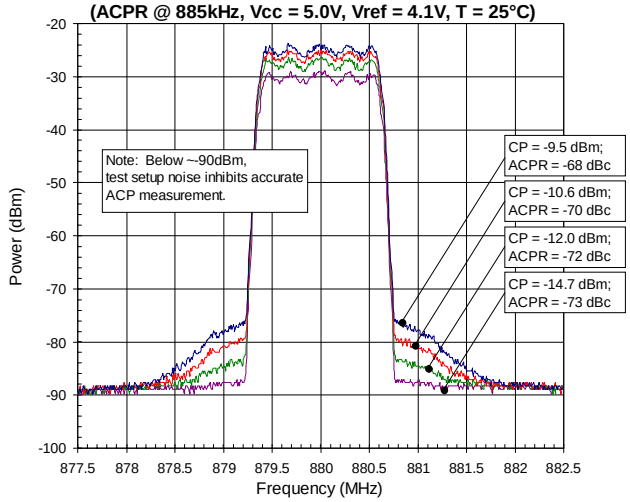
Evaluation Board Layout
Board Size 2.0" x 2.0"
Board Thickness 0.028", Board Material FR-4



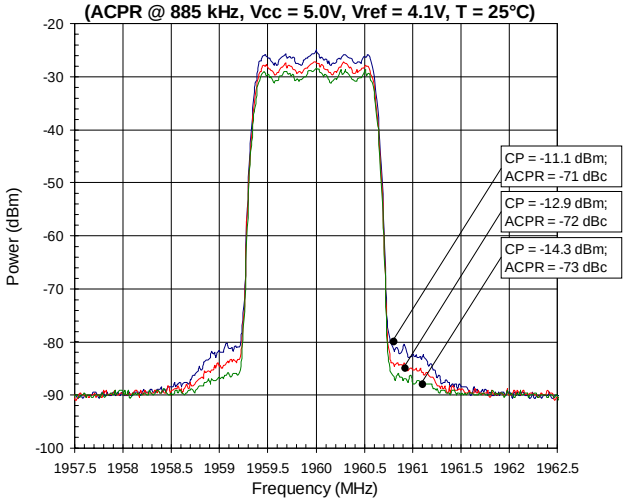




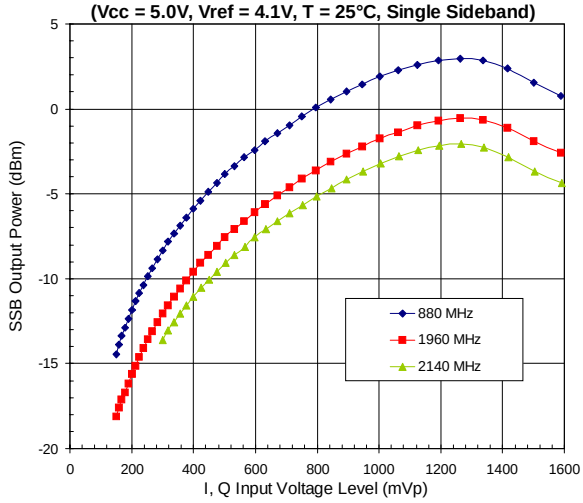
RF2484 Cellular CDMA Spectra at Various Output Levels
(ACPR @ 885kHz, Vcc = 5.0V, Vref = 4.1V, T = 25°C)



RF2484 PCS CDMA Spectra at Various Output Levels
(ACPR @ 885 kHz, Vcc = 5.0V, Vref = 4.1V, T = 25°C)



RF2484 Output Power versus I, Q Input Voltage Level
(Vcc = 5.0V, Vref = 4.1V, T = 25°C, Single Sideband)



RF2484 Output Channel Power vs I, Q Input Voltage Level
(Vcc = 5.0V, Vref = 4.1V, T = 25°C, CDMA/W-CDMA Mod.)