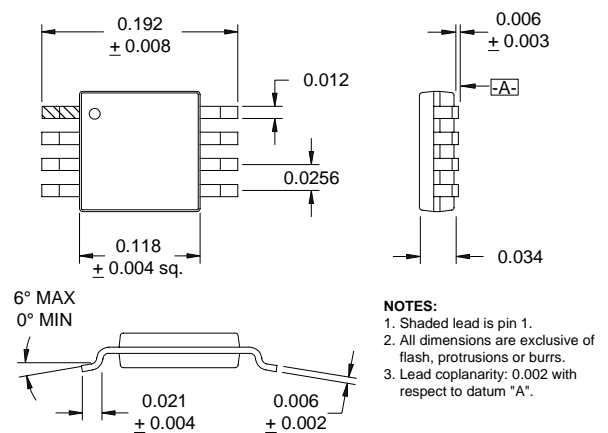


Typical Applications

- 3V CDMA Cellular Systems
- 3V CDMA PCS Systems
- 3V TDMA Cellular/PCS Systems
- General Purpose Linear IF Amplifier
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

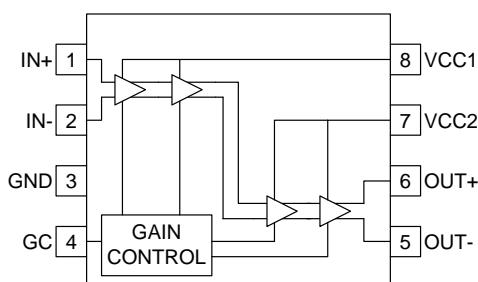
The RF2627 is a complete AGC amplifier designed for the receive section of 3V CDMA cellular and PCS applications. It is designed to amplify IF signals while providing more than 90dB of gain control range. Noise Figure, IP<sub>3</sub>, and other specifications are designed for CDMA handsets. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of a Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and this Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process, and is packaged in a standard miniature 8-lead plastic MSOP package.



Optimum Technology Matching® Applied

- Si BJT
- GaAs HBT
- GaAs MESFET
- Si Bi-CMOS
- SiGe HBT
- Si CMOS

Package Style: MSOP-8



Functional Block Diagram

Features

- Supports PCS and Cellular Applications
- -48dB to +48dB Gain Control Range
- Single 3V Power Supply
- -2dBm Input IP<sub>3</sub>
- 12MHz to 285MHz Operation
- Monolithic Construction

Ordering Information

- RF2627 3V CDMA Receive AGC Amplifier
- RF2627 PCBA Fully Assembled Evaluation Board

RF Micro Devices, Inc.  
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<http://www.rfmd.com>

# RF2627

## Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage	-0.5 to +7.0	V <sub>DC</sub>
Control Voltage	-0.5 to +5.0	V <sub>DC</sub>
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



**Caution!** ESD sensitive device.

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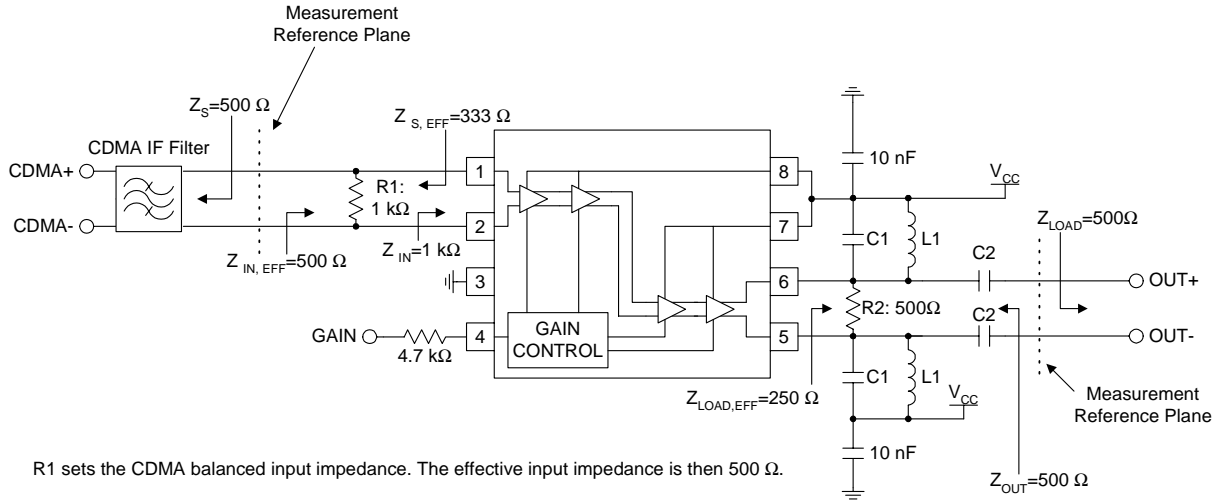
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T=25°C, 85MHz, V <sub>CC</sub> =3.0V, Z <sub>S</sub> =500Ω, Z <sub>L</sub> =500Ω, 500Ω External Input Terminating Resistor, 500Ω External Output Terminating Resistor (Effective Z <sub>S</sub> =333Ω, Effective Z <sub>L</sub> =250Ω) (See Application Example)
Frequency Range		12 to 285		MHz	
Maximum Gain	+45	+48		dB	V <sub>CC</sub> =2.4V
Minimum Gain		-48	-45	dB	V <sub>CC</sub> =0.3V
Gain Slope		57		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 3		V <sub>DC</sub>	Source impedance of 4.7kΩ
Gain Control Input Impedance		30		kΩ	
Noise Figure		5	8	dB	At maximum gain and 85MHz
Input IP <sub>3</sub>	-44	-40		dBm	At +40dB gain, referenced to 500Ω
	-4	-2		dBm	At minimum gain, referenced to 500Ω
Stability (Max VSWR)	10:1				Spurious < -70dBm
<b>IF Input</b>					
Input Impedance		1		kΩ	CDMA, differential
<b>Power Supply</b>					
Voltage		2.7 to 3.4		V	
Current Consumption		13	15	mA	Minimum gain, V <sub>CC</sub> =3.0V
Current Consumption		14	16	mA	Maximum gain, V <sub>CC</sub> =3.0V

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IF AMPLIFIERS

Pin	Function	Description	Interface Schematic
1	IN+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level other than $V_{CC}$ present. A DC to connection to $V_{CC}$ is acceptable. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is $1\text{ k}\Omega$ , while the single-ended input impedance is $500\Omega$ .	
2	IN-	Same as pin 2, except complementary input.	See pin 1.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are only valid for a $4.7\text{ k}\Omega$ DC source impedance.	
5	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a $250\Omega$ balanced load. The load sets the operating impedance, but an external choke or matching inductor to $V_{CC}$ must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to $V_{CC}$ , a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
6	OUT+	Same as pin 5, except complementary output.	See pin 5.
7	VCC1	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	VCC2	Same as pin 7.	

## Application Schematic

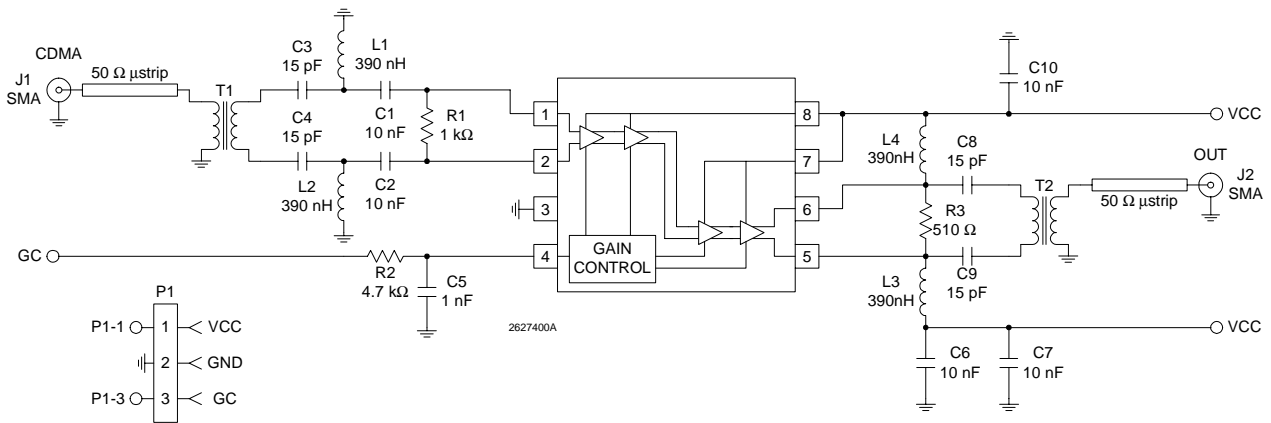


R1 sets the CDMA balanced input impedance. The effective input impedance is then 500 Ω.

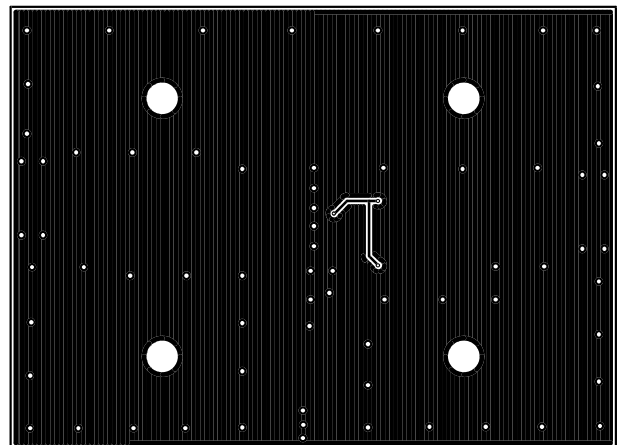
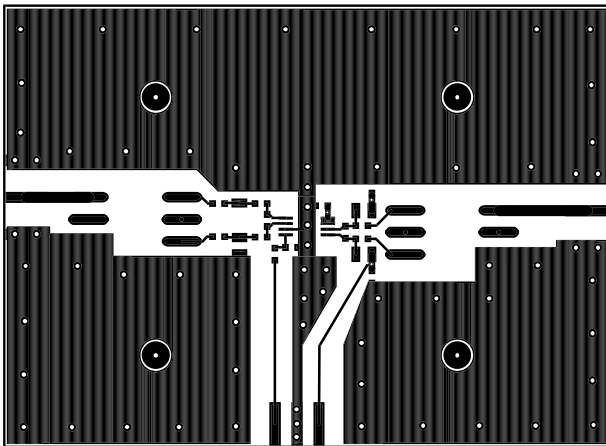
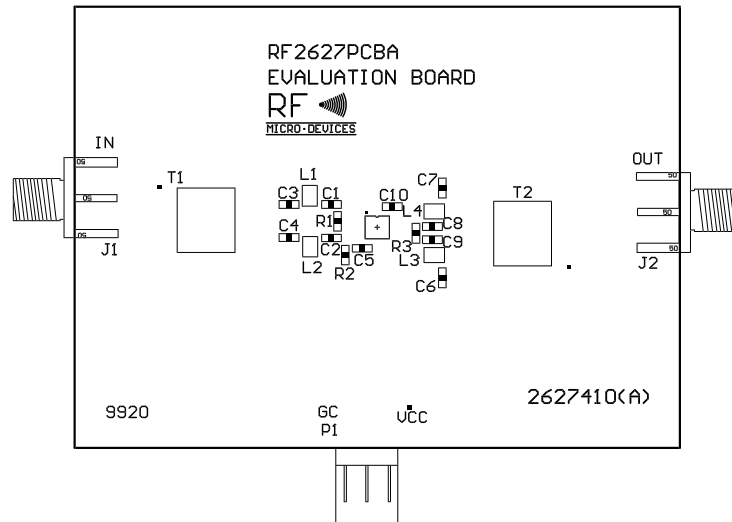
R2 sets the balanced output impedance to 500 Ω. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network of the load impedance is not 500 Ω. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the load impedance is 500 Ω.

## Evaluation Board Schematic

(Download [Bill of Materials](http://www.rfmd.com) from [www.rfmd.com](http://www.rfmd.com).)



Evaluation Board Layout  
Board Size 2.750" x 2.000"  
Board Thickness 0.031", Board Material FR-4



# RF2627

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IF AMPLIFIERS

