RF2938

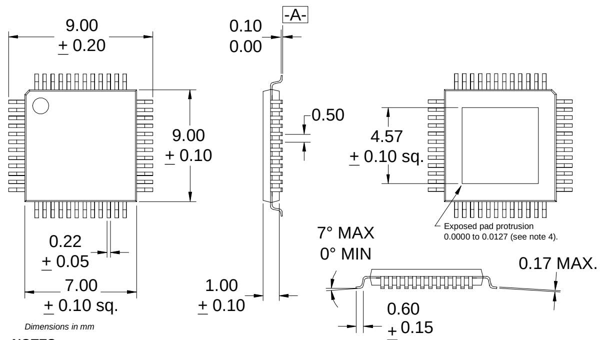
2.4GHZ SPREAD-SPECTRUM TRANSCEIVER

Typical Applications

- Wireless LANs
- Wireless Local Loop
- Secure Communication Links
- Inventory Tracking
- Wireless Security
- Digital Cordless Telephones

Product Description

The RF2938 is a monolithic integrated circuit specifically designed for direct-sequence spread-spectrum systems operating in the 2.4GHz ISM band. The part includes a direct conversion from IF receiver, quadrature demodulator, I/Q baseband amplifiers with gain control and RSSI, on-chip programmable baseband filters, dual data comparators. For the transmit side, a QPSK modulator and upconverter are provided. The design reuses the IF SAW filter for transmit and receive reducing the number of SAW filters required. Two cell or regulated three cell (3.6V maximum) battery applications are supported by the part. The part is also designed to be part of a 2.4GHz chip set consisting of the RF2444 LNA/Mixer and one of the many RFMD high efficiency GaAs HBT PA's and a dual frequency synthesizer.

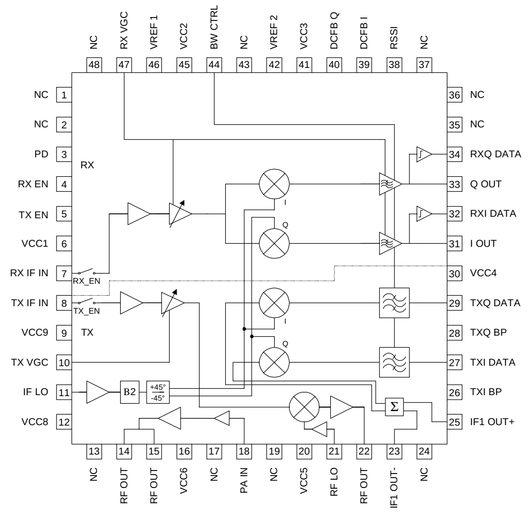


NOTES:
1. Shaded lead is Pin 1.
2. Lead coplanarity - 0.08 with respect to datum "A".
3. Leadframe material: EFTEC 64T copper or equivalent, 0.127 mm (0.005) thick.
4. Solder plating (85/15) on exposed area.

Package Style: TQFP-48 EDF, 9x9

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- 45MHz to 500MHz IF Quad Demod
- On-Chip Variable Baseband Filters
- Quadrature Modulator and Upconverter
- 2.7V to 3.6V Operation
- Part of 2.4GHz Radio Chipset
- 2.4GHz PA Driver

Ordering Information

RF2938TR13	2.4GHz Spread-Spectrum Transceiver (Tape & Reel)
RF2938 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to +3.6	V_{DC}
Input RF Level	+12	dBm
LO Input Levels	+5	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	JEDEC Level 5 @ 220°C	

Refer to “Handling of PSOP and PSSOP Products” on page 16-15 for special handling information.

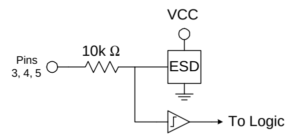
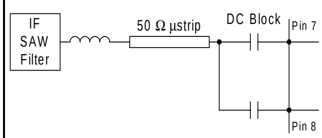
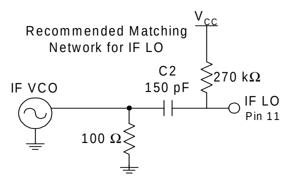
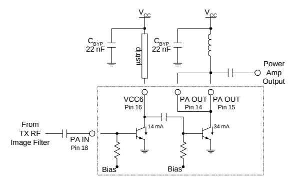
Refer to “Soldering Specifications” on page 16-13 for special soldering information.

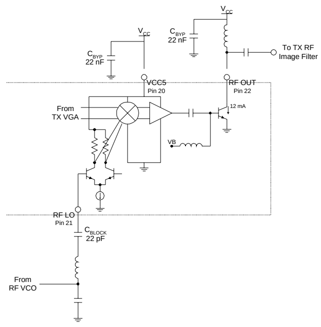
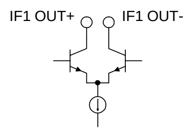
Caution! ESD sensitive device.

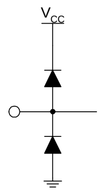
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Receiver					T=25°C, V_{CC}=3.3V, Freq=280MHz, R_{BW}=10kΩ
RX Frequency Range	45		500	MHz	
Cascaded Voltage Gain		8 to 93		dB	Dependent upon RX VGC
Cascaded Noise Figure		5		dB	At maximum gain.
Cascaded Input IP_3		30		dBμV	V_{GC} <1.2V
Cascaded Input IP_3		105		dBμV	V_{GC}>2.0V
RSSI Dynamic Range		60		dB	At V_{GC}=1.4V
RSSI Output Voltage Compliance		1.1 to 2.3		V	Maximum RSSI is 2.5V or V_{CC}-0.3, whichever is less. V_{GC}=1.4V
IF LO Leakage		-68		dBm	f=280MHz, LO Power=-10dBm
Quadrature Phase Variation		±2	±5	°	With expected LO amplitude and harmonic content. R1=270kΩ.
Quadrature Amplitude Offset		+0.25		dB	Q>I
Quadrature Amplitude Variation		±0.25	±0.5	dB	
IF AMP and Quad Demod					
Gain Control Range		43		dB	VGC <1.2V max gain, VGC>2.0V=min gain
Noise Figure		5		dB	Single Sideband
IF Input Impedance		230-j400		Ω	Single ended. 280MHz
		75-j350		Ω	Single ended. 374MHz
Input IP_3		-68		dBm	V_{GC}<1.2V
		-8		dBm	V_{GC}>2.0V
RX Baseband Amplifiers					
THD		3		%	At maximum gain setting
		3		%	At minimum gain setting
Gain Control Range		30		dB	V_{GC}<1.2V=max gain, V_{GC}>2.0V=min gain
Output Voltage		500		mV_{PP}	$R_L \geq 5k\Omega$, $C_L \leq 5pF$
DC Output Voltage		1.7		V	
RX Baseband Filters					
Baseband Filter 3dB Bandwidth	1		35	MHz	5th order Bessel LPF. Set by BW CTRL
Passband Ripple			0.1	dB	
Baseband Filter 3dB Frequency Accuracy		±10	±30	%	
Group Delay		15		ns	At 35MHz, increasing as bandwidth decreases.
Group Delay		400		ns	At 2MHz.
Baseband Filter Ultimate Rejection		>80		dB	
Output Impedance		20		Ω	Designed to drive $\geq$5kΩ, $\leq$5pF load.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Data Amplifiers					
Bandwidth	40			MHz	
Gain (Limiting mode)		60		dB	Open Loop.
Rise and Fall Time		2	5	ns	5pF load.
Logic High Output	V_{CC}-0.3V	V_{CC}		V	Source Current 1mA
Logic Low Output			0.3	V	Sink Current 1mA.
Hysteresis		30		mV	
Transmit Modulator and LPF					
Filter Gain		0		dB	Any setting
Baseband Filter 3dB Bandwidth	1		35	MHz	5th order Bessel LPF, Set by BW CTRL
Passband Ripple			0.1	dB	
Group Delay		15		ns	At 35MHz, increasing as bandwidth decreases.
Group Delay		400		ns	At 2MHz.
Ultimate Rejection		>80		dB	
Input Impedance	3			kΩ	Single ended
Input AC Voltage			200	mV_{p-p}	Linear, Single ended.
Input DC Offset Requirement	1.6	1.7	1.8	V	For correct operation.
IF Frequency Range	45		500	MHz	
Output Impedance		2		kΩ	Open Collector when TX on, hi-Z when off
I/Q Phase Balance		±2	±5		
I/Q Gain Balance		0.5±0.25	1.0	dB	
Conversion Voltage Gain		1.1		V/V	With Current Combination into 50Ω single-ended load
Output P1dB		-6		dBm	With Current Combination into 50Ω single-ended load
Carrier Output		-30		dBm	Without external offset adjustments. 280MHz
Harmonic Outputs		-30		dBc	
Transmit VGA and Upconverter					
VGA Gain Range		17		dB	
VGA Input Voltage Range		1.0 to 2.0		V	Positive Slope
VGA Gain Sensitivity		17		dB/V	
VGA Input Impedance		230-j400		Ω	280MHz
		75-j350		Ω	374MHz
RF Mixer Output Impedance		50		Ω	With matching elements.
VGA/Mixer Conversion Gain		+10 to +27		dB	With 50Ω match on the output.
VGA/Mixer Output Power		-9		dBm	1dB compression - Single Side Band, TX GC=1.0V
VGA/Mixer Output Power		-4		dBm	1dB compression - Single Side Band, TX GC=2.0V

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmit Power Amp					
Linear Output Power		6		dBm	
Gain		23		dB	
Output P1dB		12		dBm	
Output Impedance		50		Ω	
Input IP3		0		dBm	
Input Impedance		50		Ω	
Power Down Control					
Logical Controls "ON"	V_{CC}-0.3V		V_{CC}+0.3V	V	Voltage supplied to the input, not to exceed 3.6V
Logical Controls "OFF"	-0.3	0	0.3	V	Voltage supplied to the input.
Control Input Impedance		>1		MΩ	
RSSI Response Time		1.8		μs	≤8pF on RSSI output.
RX V_{GC} Response TIme		200		ns	Full step in gain, to 90% of final output level.
RX EN Response TIme		2		μs	I/Q output VALID
TX EN Response TIme		330		ns	To IF output VALID
V_{PD} to RX Response TIme		1.33		ms	To I/Q output VALID
V_{PD} to TX Response TIme		50		μs	To IF output VALID
IF LO Input					The IF LO is divided by 2 and split into quadrature signals to drive the frequency mixers.
Input Impedance		1050-j1200		Ω	f=560MHz
Input Power Range	-15	-10	0	dBm	peak
Input Frequency	90		1000	MHz	(2x IF Frequency)
RF LO Input					
Input Impedance		33-j110		Ω	f=2.16GHz untuned.
Input Power Range	-15		0	dBm	
Input Frequency	2000		2400	MHz	
Power Supply					
Voltage	2.7	3.3	3.6	V	
Total Current Consumption					V_{CC}=3.3V, Baseband BW 1MHz to 40MHz
Sleep Mode Current		1		μA	PD=0, RX EN=1, TX EN=1
PA Driver Current		48		mA	
RX Current BW (MHz)					
0-11		65		mA	
12-20		70		mA	
20-30		110		mA	
TX Current BW (MHz)					Excluding PA Driver
0-11		95		mA	
12-20		105		mA	
20-30		115		mA	

Pin	Function	Description	Interface Schematic
1	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
2	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
3	PD	This pin is used to power up or down the transmit and receive base-band sections. A logic high powers up the quad demod mixers, TX and RX GmC LPF's, baseband VGA amps, data amps, and IF LO buffer amp/ phase splitter. A logic low powers down the entire IC for sleep mode. Also, see State Decode Table.	
4	RX EN	Enable pin for the receiver 15dB gain IF amp and the RX VGA amp. Powers up all receiver functions when PD is high, turns off the receiver IF circuits when low. Also, see State Decode Table.	See pin 3.
5	TX EN	This pin is used to enable the transmit upconverter, buffer amps, 15db IF amp, quad mod mixers, TX LO buffer, TX VGA, and PA driver. TX EN is active low, when TX EN <1V, the transmit circuit is active if PD is high. A logic high (TX EN >2V) disables the transmit IF/RF circuitry and quad mod. Also, see State Decode Table.	See pin 3.
6	VCC1	Power supply for RX VGA amplifier, IC logic and RX references.	
7	RX IF IN	IF input for receiver section. Must have DC blocking cap. The capacitor value should be appropriate for the IF frequency. External matching to 50Ω recommended. For half duplex operation, connect RX IF IN and TX IF IN signals together after the DC blocking caps, then run a trans-mission line from the output of the IF SAW. AC coupling capacitor must be less than 150pF to prevent delay in switching RX to TX/TX to RX.	See pin 8.
8	TX IF IN	Input for the TX IF signal after SAW filter. External DC blocking cap required. External matching to 50Ω recommended. For half duplex operation, connect RX IF IN and TX IF IN signals together after the DC blocking caps, then run a transmission line from the output of the IF SAW. AC coupling capacitor must be less than 150pF to prevent delay in switching RX to TX/TX to RX.	
9	VCC9	Power supply for the TX 15dB gain amp and TX VGA.	
10	TX VGC	Gain control setting for the transmit VGA. Positive slope.	
11	IF LO	IF LO input. Must have DC blocking cap. The capacitor value should be appropriate for the IF frequency. LO frequency=2xIF. Quad mod/ demod phase accuracy requires low harmonic content from IF LO, so it is recommended to use an n=3 LPF between the IF VCO and IF LO. This is a high impedance input and the recommended matching approach is to simply add a 100Ω shunt resistor at this input to con-strain the mismatch. This pin requires a 6.5µA DC bias current. This can be accomplished with a 270kΩ resistor to V_{CC} for 3.3V operation.	
12	VCC8	Power supply for IF LO buffer and quadrature phase network.	
13	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
14	RF OUT	This is the output transistor of the power amp stage. It is an open col-lector output. The output match is formed by an inductor to V_{CC}, which supplies DC and a series cap.	
15	RF OUT	This is the output transistor of the power amp stage. It is an open col-lector output. The output match is formed by an inductor to V_{CC}, which supplies DC and a series cap.	See pin 14.
16	VCC6	Power supply for the PA driver amp. This inductance to ground via decoupling, along with an internal series capacitor, forms the interstage match.	See pin 14.

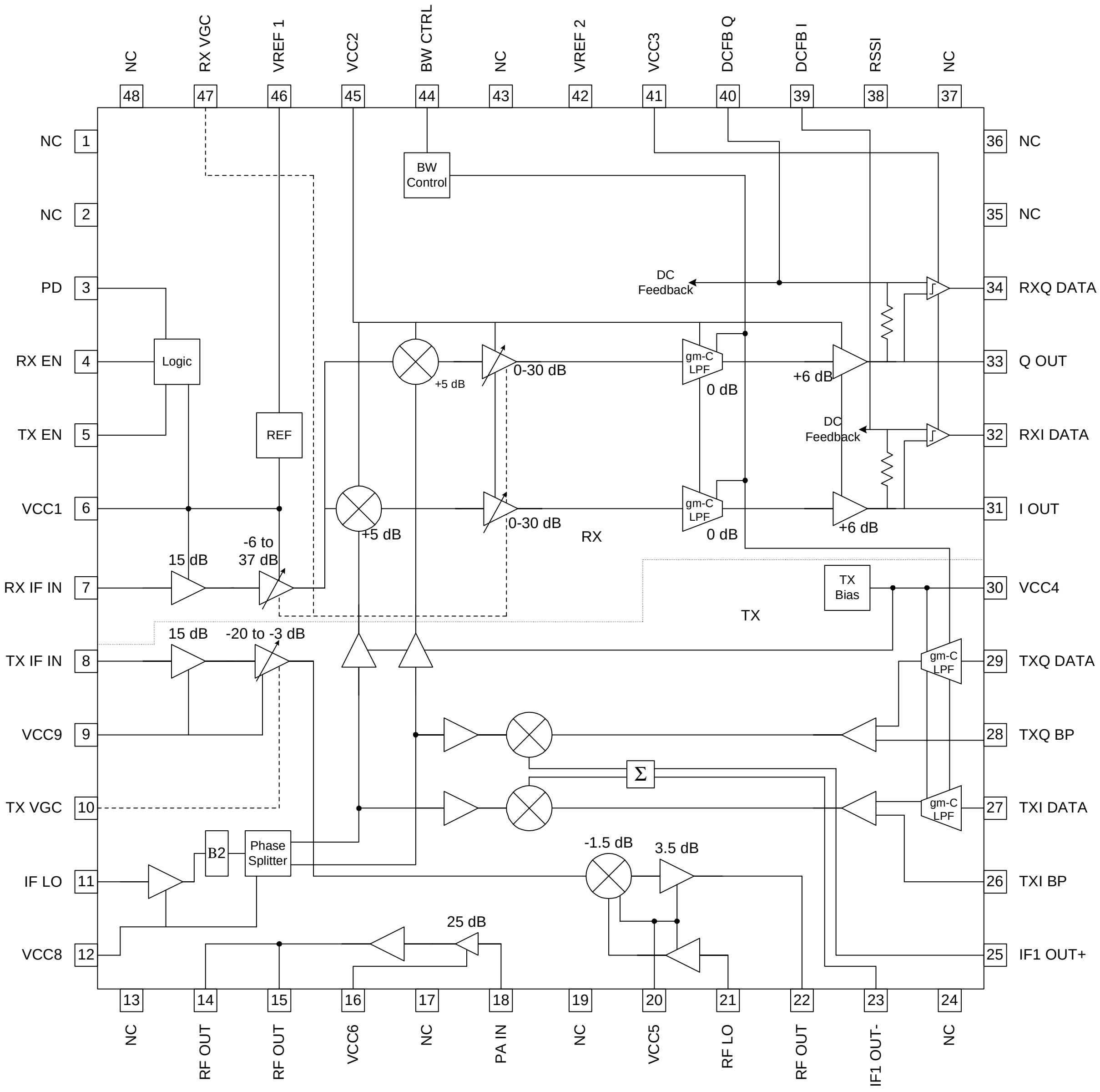
Pin	Function	Description	Interface Schematic
17	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
18	PA IN	Input to the power amplifier stage. This is a 50Ω input. Requires DC blocking/tuning cap.	See pin 14.
19	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
20	VCC5	Supply for the RF LO buffer, RF upconverter and amplifier.	
21	RF LO	Single ended LO input for the transmit upconverter. External matching to 50Ω and a DC block are required.	See pin 20.
22	RF OUT	Upconverted Transmit signal. This 50Ω output is intended to drive an RF filter to suppress the undesired sideband, harmonics, and other out-of-band mixer products.	See pin 20.
23	IF1 OUT-	The inverting open collector output of the quadrature modulator. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun with IF1 OUT+, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, just IF1 OUT+ can be used to drive a SAW single-ended with an RF choke (high Z at IF) from V_{CC} to IF1 OUT-.	
24	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
25	IF1 OUT+	The non-inverting open collector output of the quadrature modulator. This pin needs to be externally biased and DC isolated from other parts of the circuit. This output can drive a Balun with IF1 OUT-, to convert to unbalanced to drive a SAW filter. The Balun can be either broadband (transformer) or narrowband (discrete LC matching). Alternatively, just IF1 OUT+ can be used to drive a SAW single-ended with an RF choke (high Z at IF) from V_{CC} to IF1 OUT+.	See pin 23.
26	TXI BP	This is the in-phase modulator bypass pin. A 10nF capacitor to ground is recommended.	
27	TXI DATA	I input to the baseband 5 pole Bessel LPF for the transmit modulator.	
28	TXQ BP	This is the quadrature modulator bypass pin. A 10nF capacitor to ground is recommended.	
29	TXQ DATA	Q input to the baseband 5 pole Bessel LPF for the transmit modulator.	
30	VCC4	Power supply for quadrature modulator.	
31	I OUT	Baseband analog signal output for in-phase channel. 500mV$_{P-P}$ linear output.	
32	RXI DATA	Logic-level data output for the in-phase channel. This is a digital output signal obtained from the output of a Schmitt trigger. 0.3V to VCC3 - 0.3V swing minimum.	
33	Q OUT	Baseband analog signal output for quadrature channel. 500mV$_{P-P}$ linear output.	
34	RXQ DATA	Logic-level data output for the quadrature channel. This is a digital output signal obtained from the output of a Schmitt trigger. 0.3V to VCC3 - 0.3V swing minimum.	
35	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	

Pin	Function	Description	Interface Schematic
36	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
37	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
38	RSSI	Received signal strength indicator. Connect 8.2pF to ground. Output impedance is 40kΩ in parallel with 2pF.	
39	DCFB I	DC feedback capacitor for in-phase channel. Requires decoupling capacitor to ground. (22nF recommended)	
40	DCFB Q	DC feedback capacitor for quadrature channel. Requires capacitor to ground. (22nF recommended)	
41	VCC3	Supply for the I and Q data amps.This pin should be bypassed with a 10nF capacitor connected as direct as possible to GND3. Ground this pin if data amps are not used.	
42	VREF 2	Gain control reference voltage. No current should be drawn from this pin (<50μA). 2.0V nominal.	
43	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
44	BW CTRL	This pin requires a resistor to ground to set the baseband LPF bandwidth of the receiver and transmit GmC filter amps.	
45	VCC2	Supply for the I and Q baseband and GmC filters. This pin should be bypassed with a 10nF capacitor.	
46	VREF 1	This is a bypass pin for the bias circuits of the GmC filter amps and for I/Q inputs. No current should be drawn from this pin (<10μA). 1.7V nominal.	
47	RX VGC	Receiver IF and baseband amp gain control voltage. Negative slope.	
48	NC	No internal connection. May be grounded or connected on adjacent signal or left floating. Connect to ground for best results.	
Pkg Base		Ground for all circuitry in the device. A very low inductance from the base to the PCB groundplane is essential for good performance. Use an array of vias immediately underneath the device.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 3-6, 9, 10, 12, 26-34, 38-42, 44-47.	

State Decode Table	Input Pins			Internally Decoded Signals		
	PD	RX EN	TX EN	BB EN	RXIF EN	TXRF EN
Sleep Mode	0	x	x	0	0	0
Baseband Only	1	0	1	1	0	0
Receive Mode	1	1	1	1	1	0
Transmit Mode	1	0	0	1	0	1
Full Duplex	1	1	0	1	1	1

NOTES	
BB_EN Enables:	
	TX_LPF's and buffers
	Quad Demodulator mixers
	Baseband VGA and gm-C LPF's
	Data Amplifiers
	IF LO buffer/phase splitters
RXIF_EN Enables:	
	Front-end IF amplifier (RX)
	RX IF VGA amplifiers
TXRF_EN Enables:	
	Front-end IF amplifier (TX)
	TX VGA
	RF upconverter and buffer
	PA driver
	RF LO buffer
	Quad Modulator mixers

Detailed Functional Block Diagram



Theory of Operation

RECEIVER

RX IF AGC/Mixer

The front end of the IF AGC starts with a single-ended input and a constant gain amp of 15dB. This first amp stage sets the noise figure and input impedance of the IF section, and its output is taken differentially. The rest of the signal path is differential until the final baseband output, which is converted back to single-ended. Following the front end amp are multiple stages of variable gain differential amplifiers, giving the IF signal path a gain range of 9dB to 52dB. The noise figure (in max gain mode) of the IF amplifiers is 5dB, which should not degrade the system noise figure.

The IF to BB mixers are double-balanced, differential in, differential out, mixers with 5dB conversion gain. The LO for each of these mixers is shifted 90° so that the I and Q signals are separated in the mixers.

RX Baseband Amps, Filters, Data Slicers, and DC Feedback

At baseband frequency, there are multiple AGC amplifiers offering a gain range of 0dB to 30dB. Following these amplifiers are fully integrated gm-C low pass filters to further filter out-of-band signals and spurs that get through the SAW filter, anti-alias the signal prior to the A/D converter, and to band-limit the signal and noise to achieve optimal signal-to-noise ratio. The 3dB cut-off frequency of these low pass filters is programmable with a single external resistor, and continuously variable from 1MHz to 35MHz. A five-pole Bessel type filter response was chosen because it is optimal for data systems due to its flat delay response and clean step response. Butterworth and Chebychev type filters ring when given a step input making them less ideal for data systems.

The filter outputs, with +6dBm gain, drive the linear 500mV$_{PP}$ signal off-chip, but also connect internally to a data slicer which squares up the signal to CMOS levels, and drives this “data” signal off-chip. This data slicer is a high speed CMOS comparator with 30mV of hysteresis and self-aligned input DC offset. This data slicer can be independently disabled if only the linear outputs are desired.

DC feedback is built into the baseband amplifier section to correct for input offsets. Large DC offsets can arise when a mixer LO leaks to the mixer input and then mixes with itself. DC offsets can also result from random transistor mismatches. A large external capacitor is needed for the DC feedback to set the high pass cutoff, and this capacitor is reused to set the DC input level for the self-aligned data slicer.

RSSI and V_{GC} Operation

The receive signal path also has an RSSI output which is the sum of both the I and Q channels. The RSSI has about 60dBm of dynamic range and the RSSI characteristic is optimized to give best linearity and dynamic range at a VGC setting of 1.4V. It is recommended that the system sets VGC to 1.4V to take an RSSI reading to make channel activity and signal level decisions, then adjusts VGC to obtain optimum dynamic range from the I_{OUT} and Q_{OUT} outputs.

LO Input Buffers

RF LO Buffer

The RF LO input has a limiting amplifier before the mixer on both the RF2444 (RX) and RF2938 (TX). This limiting amplifier design and layout is identical on both ICs, which will make the input impedance the same as well. Having this amplifier between the VCO and mixer minimizes any reverse effect the mixer has on the VCO, expands the range of acceptable LO input levels, and holds the LO input impedance constant when switching between RX and TX. The LO input power range is -18dBm to +5dBm, which should make it easy to interface to any VCO and frequency synthesizer.

IF LO Buffer

The IF LO input has a limiting amplifier before the phase splitting network to amplify the signal and help isolate the VCO from the IC. Also, the LO input signal must be twice the desired intermediate frequency. This simplifies the quadrature network and helps reduce the LO leakage onto the RX_IF input pin (since the LO input is now at a different frequency than the IF). The amplitude of this input needs to be between -15dBm and 0dBm. Excessive IF LO harmonic content affects phase balance of the modulator and demodulator so it is recommended that a simple n=3 low pass filter is included between VCO and IF LO input. The IF LO input requires a DC bias current of +6.5μA. This can be accomplished with a 270kΩ resistor to V_{CC} for 3.3V operation. Failing to provide this will cause a phase imbalance in the IF LO quadrature divider of up to 8°, which in turn causes a similar imbalance in the I/Q outputs and the T_X modulator.

TRANSMITTER

TX LPF and Mixers

The transmit section starts with a pair of 5-pole Bessel filters identical to the filters in the receive section and with the same 3dB frequency. These filters pre-shape and band-limit the digital or analog input signals prior to the first upconversion to IF. These filters have a high input impedance and expect an input signal of 200mV$_{PP}$ typical. Following these low pass filters are the I/Q quadrature upconverter mixers. Each of these mixers is half the size and half the current of the RF to IF downconverter on the RF2444. Recall that this upconverted signal may drive the same SAW filter (in half duplex mode) as the RF2444 and therefore share the same load. Having the sum of the two BB to IF mixers equal in size and DC current to the RF to IF mixer, will minimize the time required to switch between RX and TX, and will facilitate the best impedance match to the filter.

TX VGA

The AGC after the SAW filter starts with a switch and a constant gain amplifier of 15dB, which is identical to the circuitry on the receive IF AGC. This was, done, as on the RX signal path, so that the input impedance will remain constant for different TX gain control voltages. Following this 15dB gain amplifier is a single stage of gain control offering 15dB gain range. The main purpose of adding this variable gain is to give the system the flexibility to use different SAW filters and image filters with different insertion loss values. This gain could also be adjusted real time, if desired.

TX Upconverter

The IF to RF upconverter is a double-balanced differential mixer with a differential to single-ended converter on the output to supply 0dBm peak linear power to the image filter. The upconverted SSB signal should have -6dBm power at this point, and the image will have the same power, but due to the correlated nature of the signal and image, the output must support 0dBm of linear power to maintain linearly.

+6dBm PA Driver

The SSB output of the upconverter is -6dBm of linear power. The image filter should have at most 4dB of insertion loss while removing the image, LO, 2LO and any other spurs. The filter output should supply the PA driver input -10dBm of power.

The PA driver is a two-stage class A amplifier with 10dB gain per stage and capable of delivering 6dBm of linear power to a 50Ω load, and has a 1dB compression point of 12dBm. For lower power applications, this PA driver can be used to drive a 50Ω antenna directly.

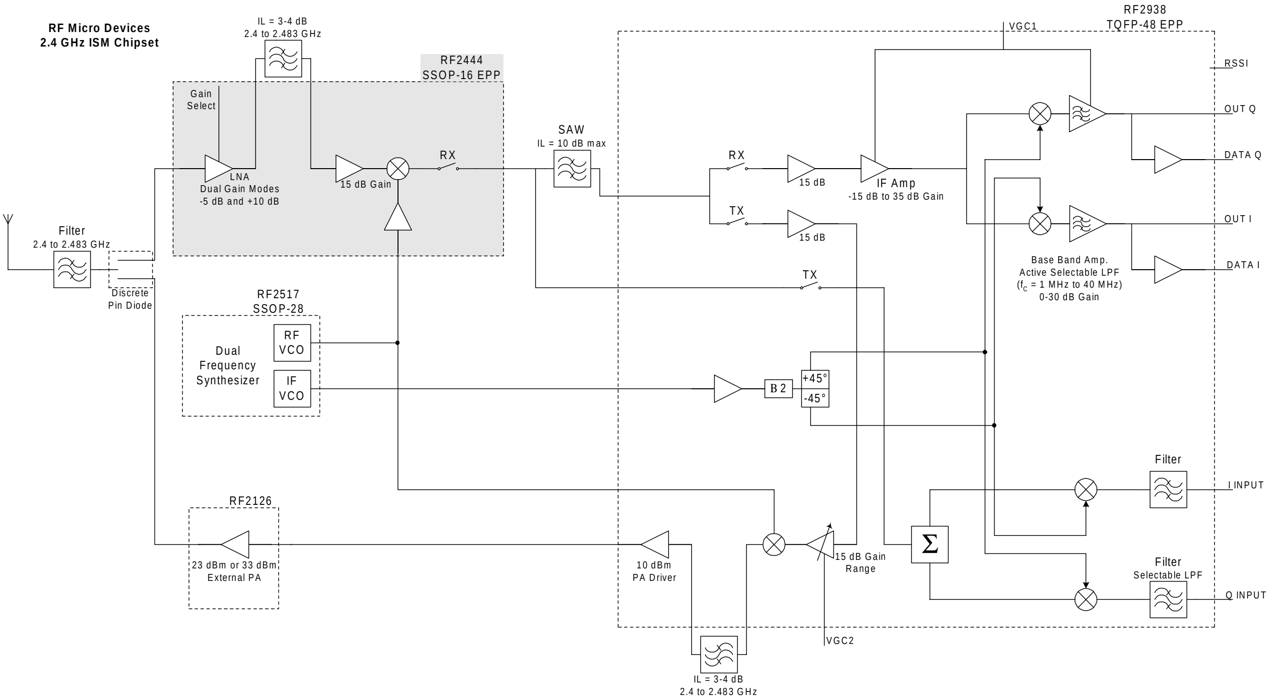
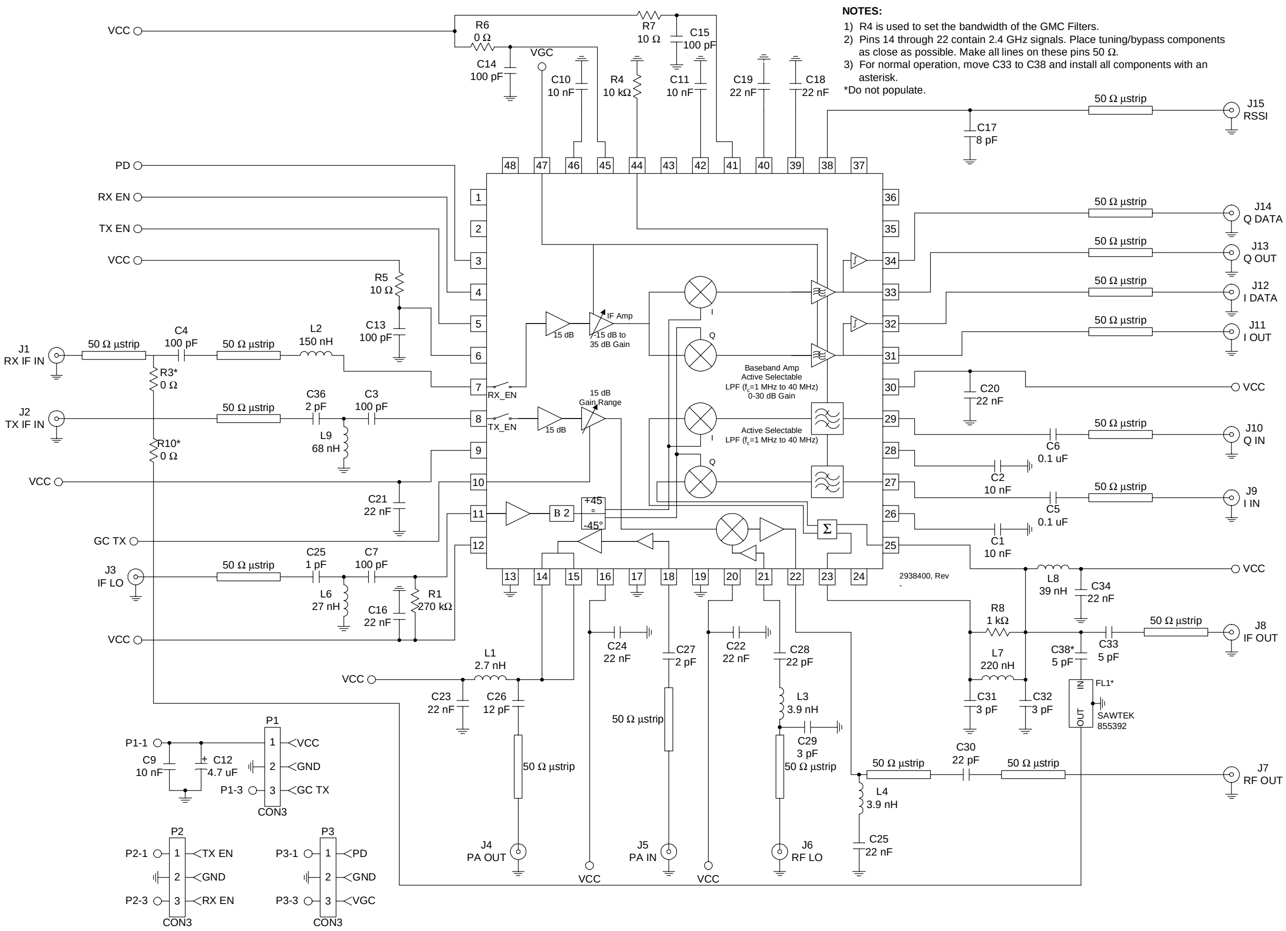


Figure 1. Entire Chipset Functional Block Diagram

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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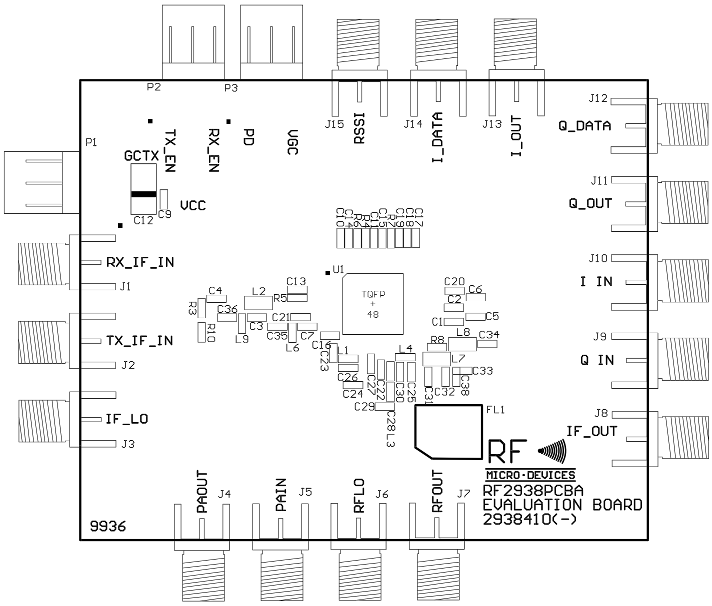
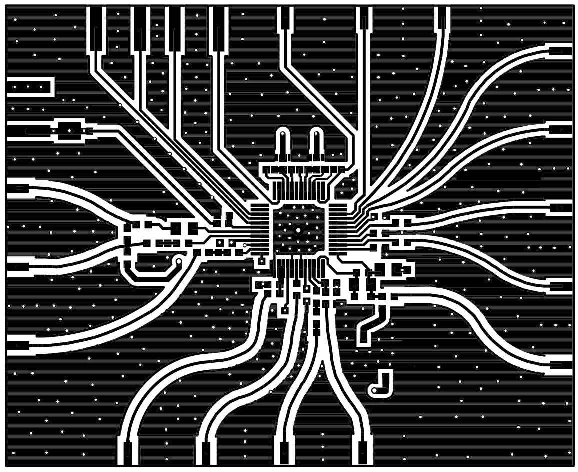
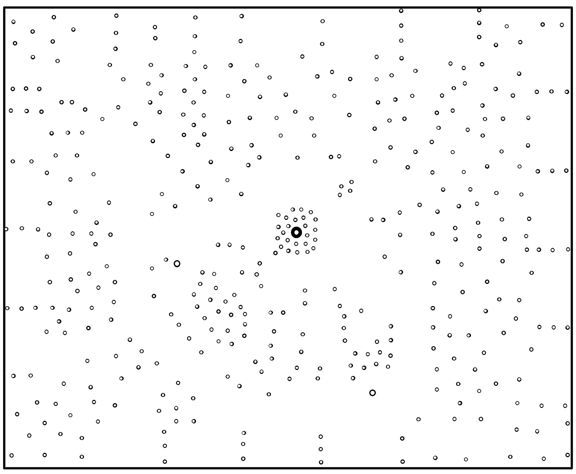
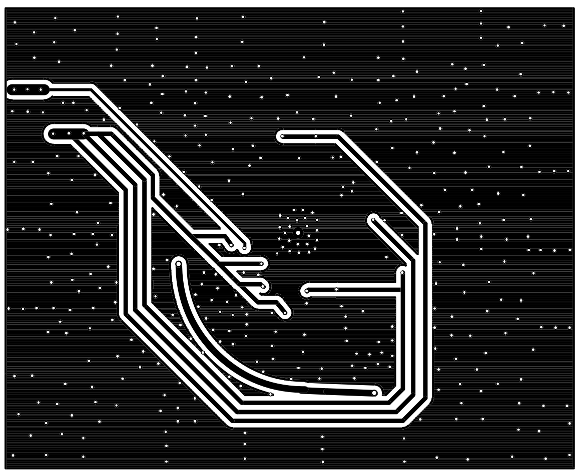
Evaluation Board Layout
Board Size 2.580” x 2.086”

Thickness: Top to Ground Laminate, 0.008”; Ground to Bottom Laminate, 0.023”;
Board Material FR-4; Multi-Layer



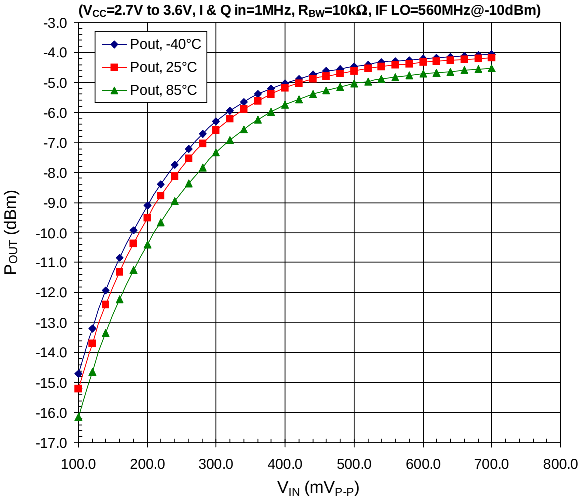






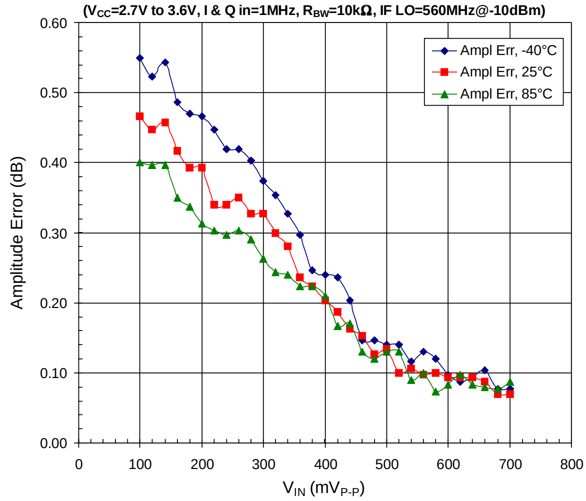
V_{IN} versus P_{OUT}

(V_{CC}=2.7V to 3.6V, I & Q in=1MHz, R_{BW}=10kΩ, IF LO=560MHz@-10dBm)



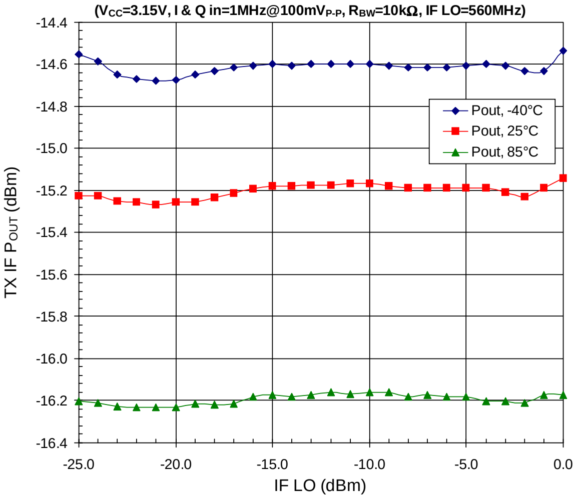
V_{IN} versus Amplitude Error

(V_{CC}=2.7V to 3.6V, I & Q in=1MHz, R_{BW}=10kΩ, IF LO=560MHz@-10dBm)



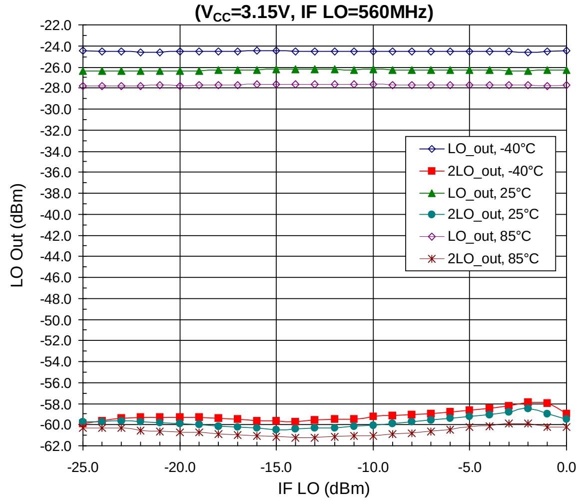
TX IF P_{OUT} versus IF LO

(V_{CC}=3.15V, I & Q in=1MHz@100mVP-P, R_{BW}=10kΩ, IF LO=560MHz)



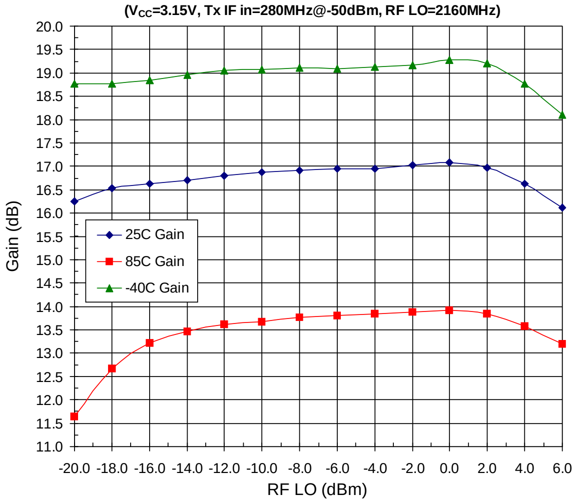
LO & 2LO Out versus IF LO

(V_{CC}=3.15V, IF LO=560MHz)

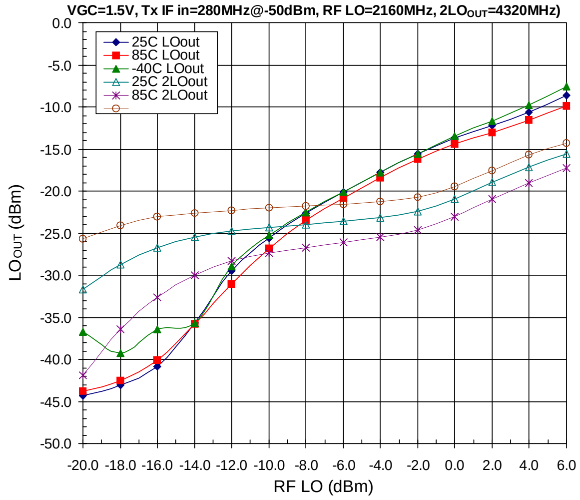


RF Conversion Gain versus RF LO Level

(V_{CC}=3.15V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz)



RF LO_{OUT} & RF $2LO_{OUT}$ versus RF LO Level (V_{CC}=3.15V, VGC=1.5V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz, $2LO_{OUT}$=4320MHz)



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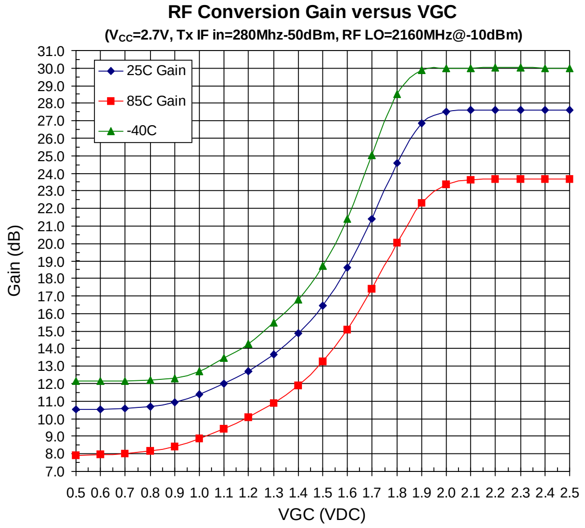
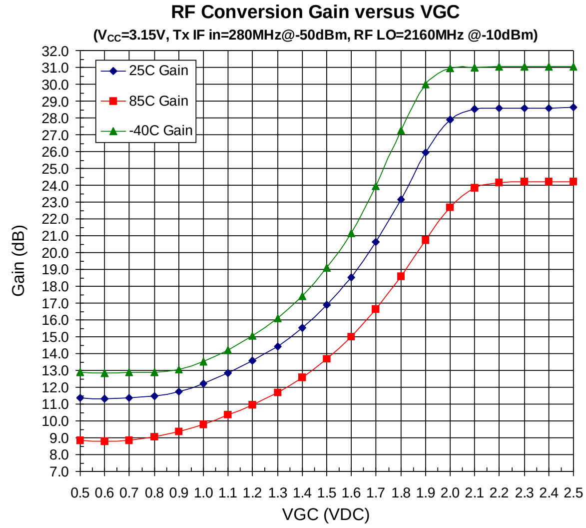
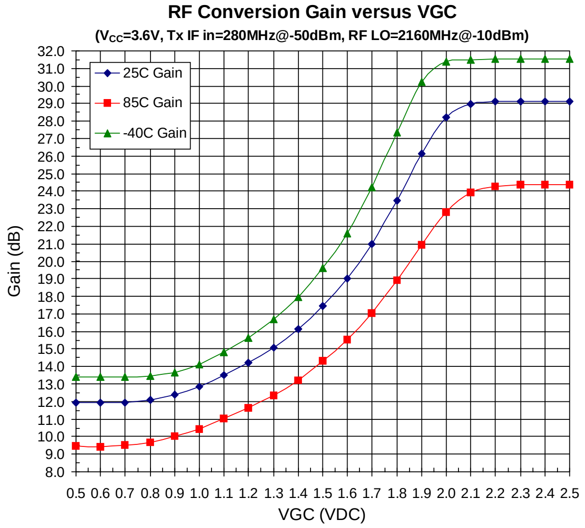
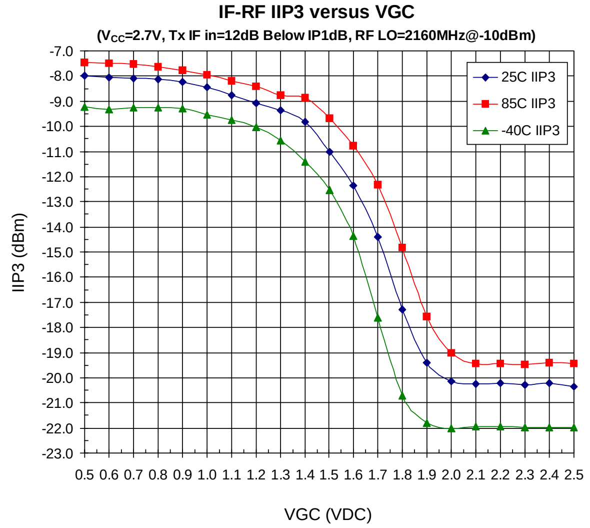
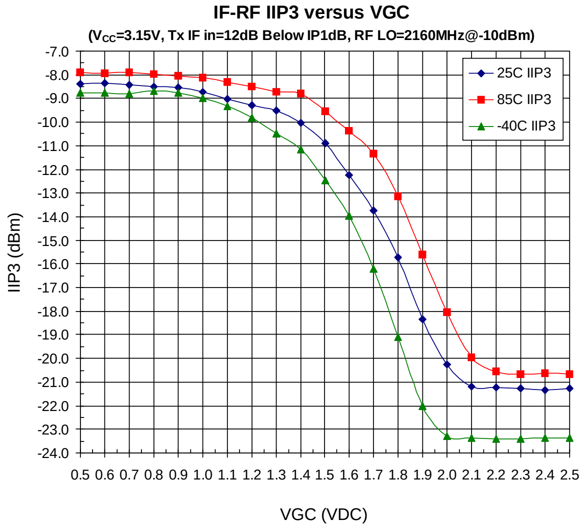
TRANSCEIVERS

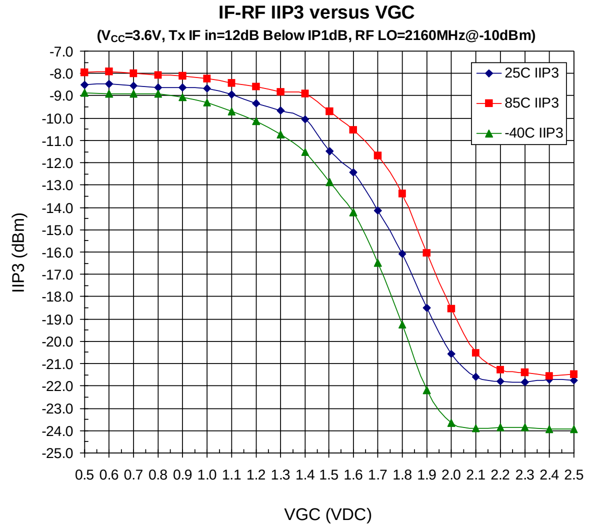

RF Conversion Gain versus VGC
(VCC=2.7V, Tx IF in=280Mhz-50dBm, RF LO=2160MHz@-10dBm)
25C Gain
85C Gain
-40C
Gain (dB)
VGC (VDC)


RF Conversion Gain versus VGC
(VCC=3.15V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz @-10dBm)
25C Gain
85C Gain
-40C Gain
Gain (dB)
VGC (VDC)

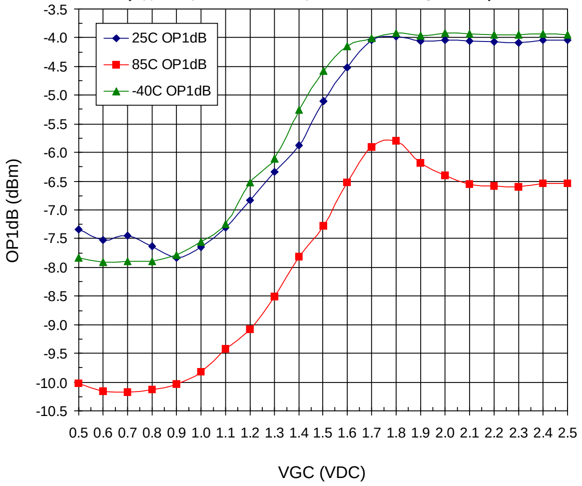

RF Conversion Gain versus VGC
(VCC=3.6V, Tx IF in=280MHz@-50dBm, RF LO=2160MHz@-10dBm)
25C Gain
85C Gain
-40C Gain
Gain (dB)
VGC (VDC)


IF-RF IIP3 versus VGC
(VCC=2.7V, Tx IF in=12dB Below IP1dB, RF LO=2160MHz@-10dBm)
25C IIP3
85C IIP3
-40C IIP3
IIP3 (dBm)
VGC (VDC)

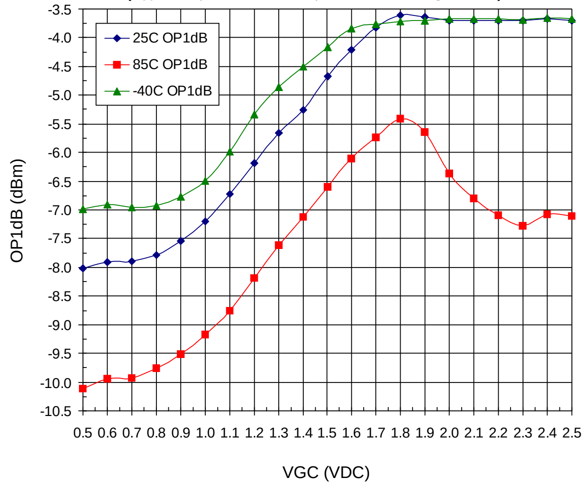

IF-RF IIP3 versus VGC
(VCC=3.15V, Tx IF in=12dB Below IP1dB, RF LO=2160MHz@-10dBm)
25C IIP3
85C IIP3
-40C IIP3
IIP3 (dBm)
VGC (VDC)


IF-RF IIP3 versus VGC
(VCC=3.6V, Tx IF in=12dB Below IP1dB, RF LO=2160MHz@-10dBm)
25C IIP3
85C IIP3
-40C IIP3
IIP3 (dBm)
VGC (VDC)

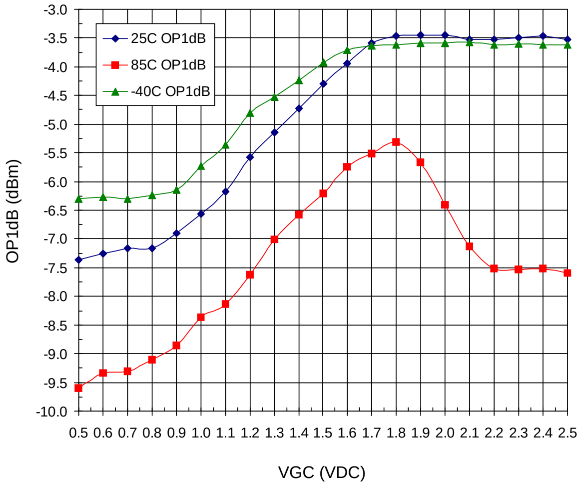
IF-RF OP1dB versus VGC
(V_{CC}=2.7V, Tx IF in=280Mhz, RF LO=2160MHz@-10dBm)



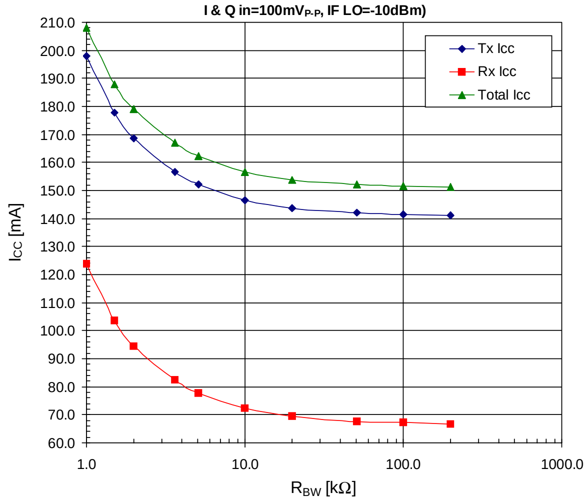
IF-RF OP1dB versus VGC
(V_{CC}=3.15V, Tx IF in=280MHz, RF LO=2160MHz@-10dBm)



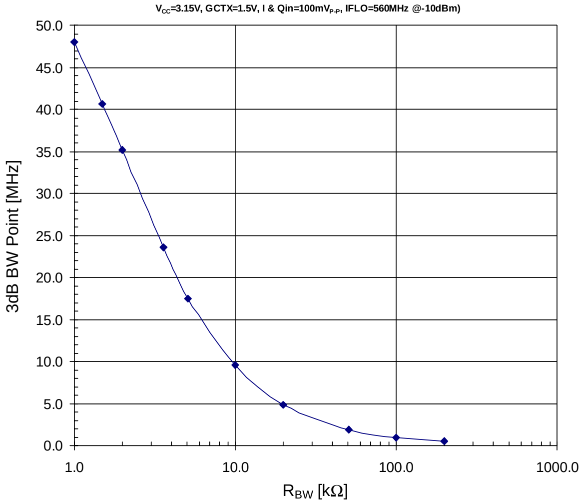
IF-RF OP1dB versus VGC
(VCC=3.6V, Tx IF in=280MHz, RF LO=2160MHz@-10dBm)



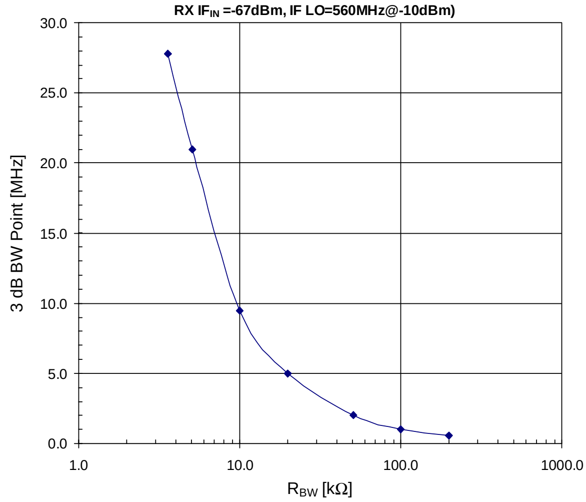
I_{CC} versus R_{BW} (Temp=Ambient, V_{CC}=3.15V, GC TX=1.5V, I & Q in=100mV_{P-P}, IF LO=-10dBm)



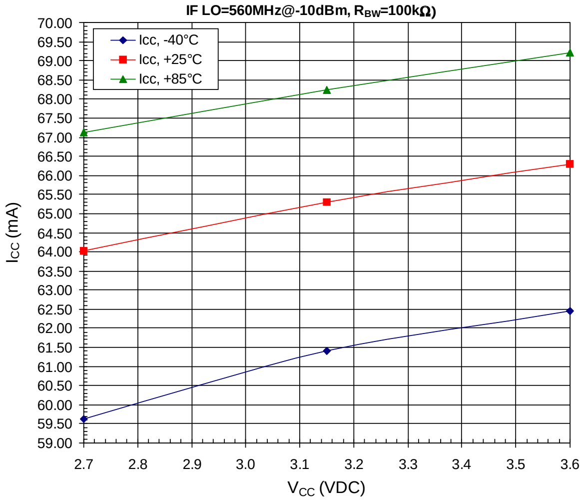
TX 3dB BW point versus R_{BW} (Broadband 50Ω match on IF out, Temp=Ambient, V_{CC}=3.15V, GCTX=1.5V, I & Qin=100mV_{P-P}, IFLO=560MHz @-10dBm)



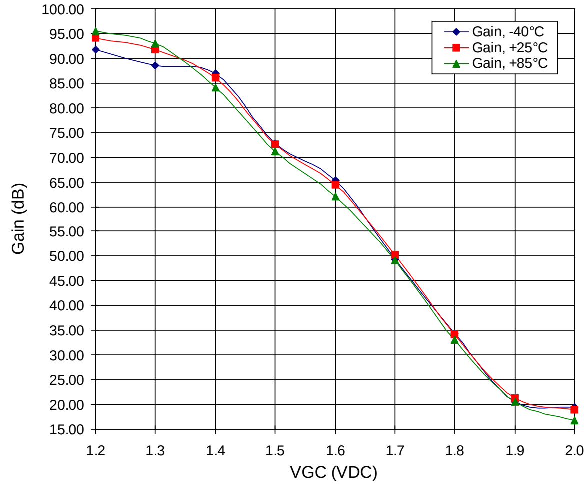
RX 3dB BW versus R_{BW} (Temp=Ambient, V_{CC}=3.15V, V_{GC}=1.6V, RX IF_{IN} =-67dBm, IF LO=560MHz@-10dBm)



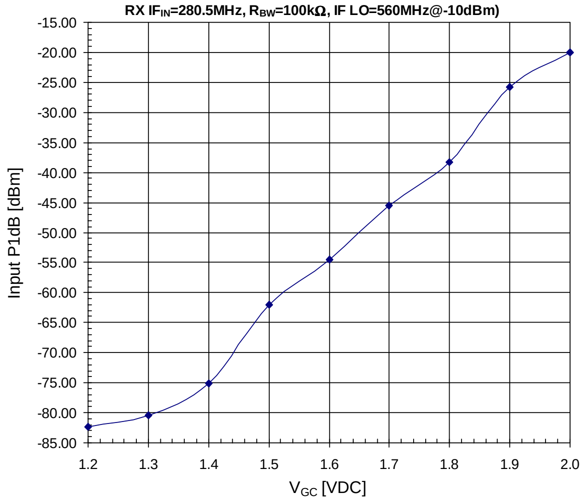
RX I_{CC} versus V_{CC} (V_{GC}=1.2V to 2.0V, I & Q_out=500mV_{P-P}, IF LO=560MHz@-10dBm, R_{BW}=100kΩ)



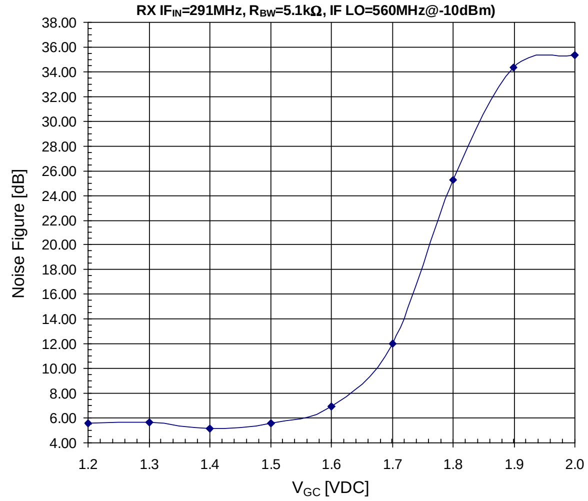
RX Gain versus V_{GC} (V_{CC}=2.7-3.6V, RX IF_{IN}=280.5MHz, R_{BW}=100kΩ, I & Q out=500mV_{P-P}, IF LO=560MHz@-10dBm)



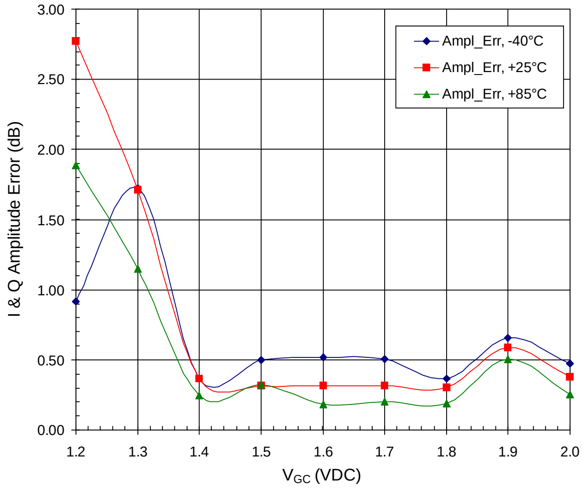
Input P1dB versus V_{GC} (Temp=Ambient, V_{CC}=3.15V, RX IF_{IN}=280.5MHz, R_{BW}=100kΩ, IF LO=560MHz@-10dBm)



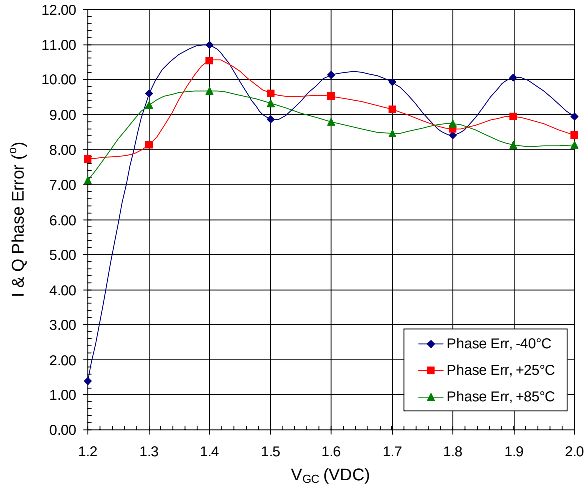
Noise Figure versus V_{GC} (Temp=Ambient, V_{CC}=3.15V, RX IF_{IN}=291MHz, R_{BW}=5.1kΩ, IF LO=560MHz@-10dBm)

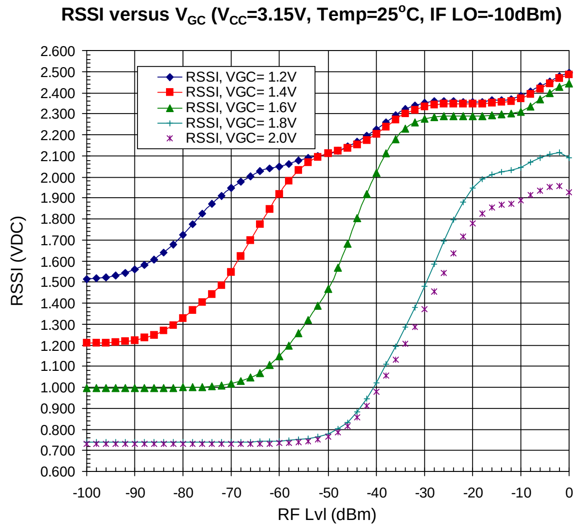


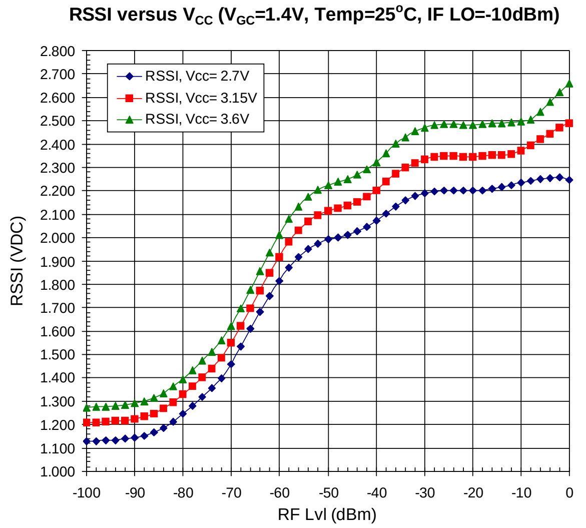
I & Q Amplitude Balance versus V_{GC} (V_{CC}=3.15V, RX IF_{IN}=280.5MHz, R_{BW}=100kΩ, I & Q out=500mV_{P-P}, IF LO=560MHz@-10dBm)

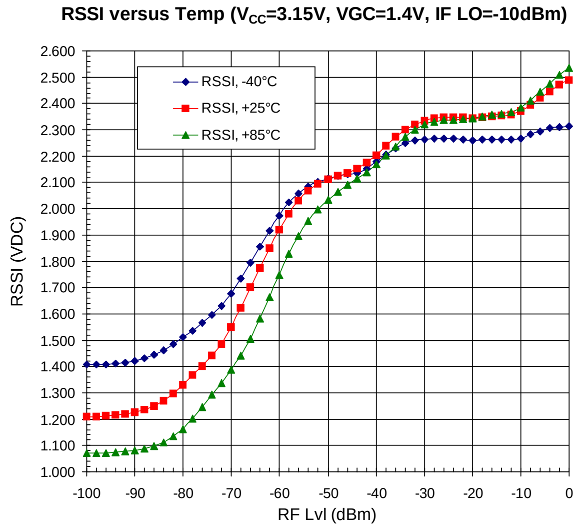


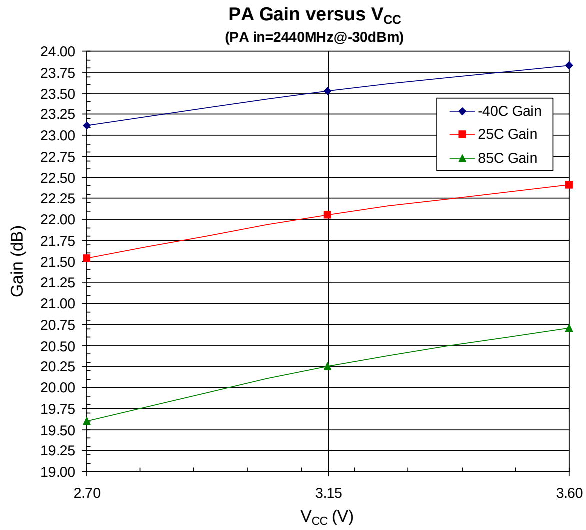
I & Q Phase Balance versus V_{GC} (V_{CC}=2.7-3.6V, RX IF_{IN}=280.5MHz, R_{BW}=100kΩ, I & Q out=500mV_{P-P}, IF LO=560MHz@-10dBm)

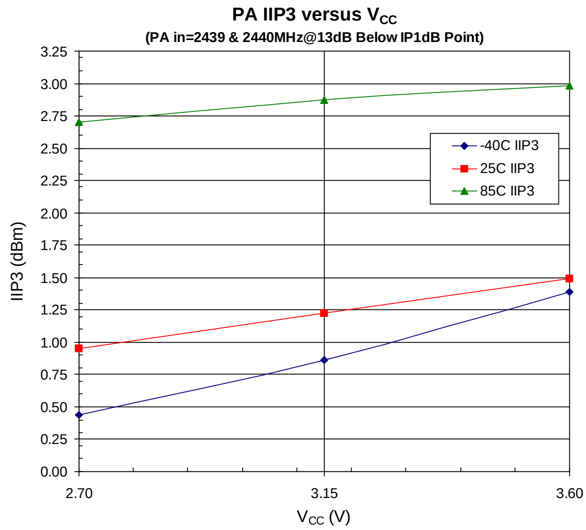


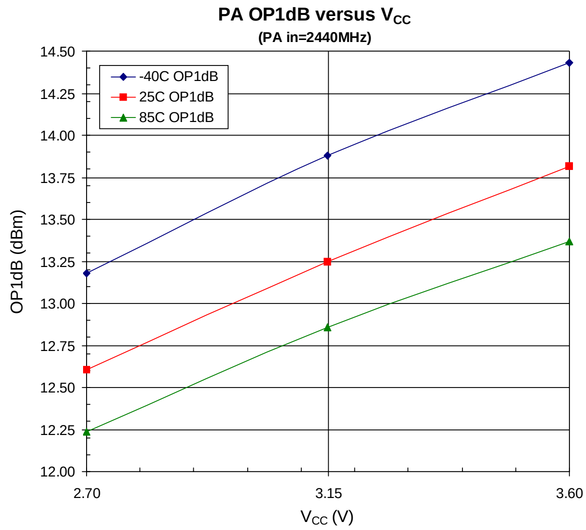

RSSI versus V_{GC} (V_{CC}=3.15V, Temp=25°C, IF LO=-10dBm)
RSSI, VGC= 1.2V
RSSI, VGC= 1.4V
RSSI, VGC= 1.6V
RSSI, VGC= 1.8V
RSSI, VGC= 2.0V
RSSI (VDC)
RF Lvl (dBm)

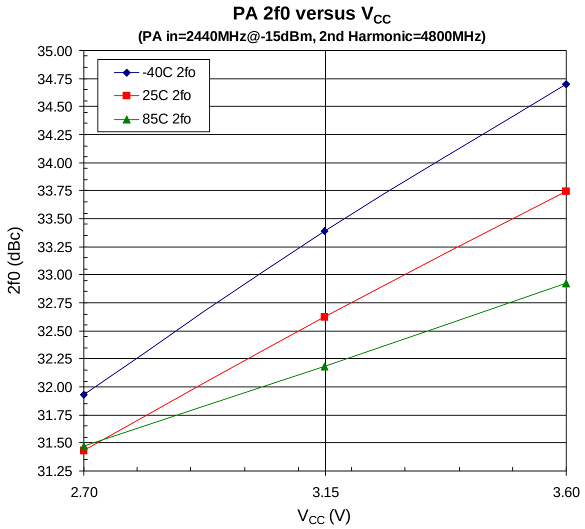

RSSI versus V_{CC} (V_{GC}=1.4V, Temp=25°C, IF LO=-10dBm)
RSSI, Vcc= 2.7V
RSSI, Vcc= 3.15V
RSSI, Vcc= 3.6V
RSSI (VDC)
RF Lvl (dBm)


RSSI versus Temp (V_{CC}=3.15V, VGC=1.4V, IF LO=-10dBm)
RSSI, -40°C
RSSI, +25°C
RSSI, +85°C
RSSI (VDC)
RF Lvl (dBm)


PA Gain versus V_{CC}
(PA in=2440MHz@-30dBm)
-40C Gain
25C Gain
85C Gain
Gain (dB)
V_{CC} (V)


PA IIP3 versus V_{CC}
(PA in=2439 & 2440MHz@13dB Below IP1dB Point)
-40C IIP3
25C IIP3
85C IIP3
IIP3 (dBm)
V_{CC} (V)


PA OP1dB versus V_{CC}
(PA in=2440MHz)
-40C OP1dB
25C OP1dB
85C OP1dB
OP1dB (dBm)
V_{CC} (V)


PA 2f0 versus V_{CC}
(PA in=2440MHz@-15dBm, 2nd Harmonic=4800MHz)
-40C 2fo
25C 2fo
85C 2fo
2f0 (dBc)
35.00
34.75
34.50
34.25
34.00
33.75
33.50
33.25
33.00
32.75
32.50
32.25
32.00
31.75
31.50
31.25
2.70
3.15
3.60
V_{CC} (V)