RF5176

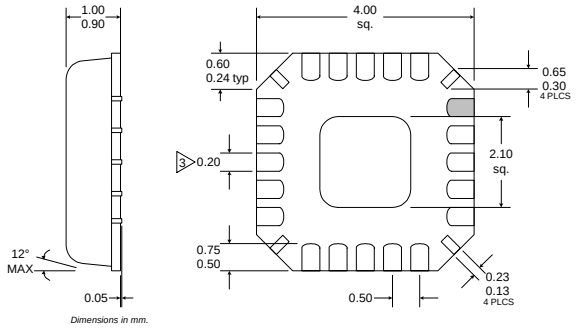
3V W-CDMA POWER 1900MHZ/
3V LINEAR POWER AMPLIFIER

Typical Applications

- 3V 1850-1910MHz CDMA-2000 Handsets
- 3V 1920-1980MHz W-CDMA Handsets
- Spread-Spectrum Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

The RF5176 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 3V CDMA-2000 and W-CDMA handsets as well as other applications in the 1850MHz to 2000MHz band. The device is self-contained, and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics over all recommended supply voltages. The device has a continuously variable bias circuit to allow idle current to be optimized for a given output power.

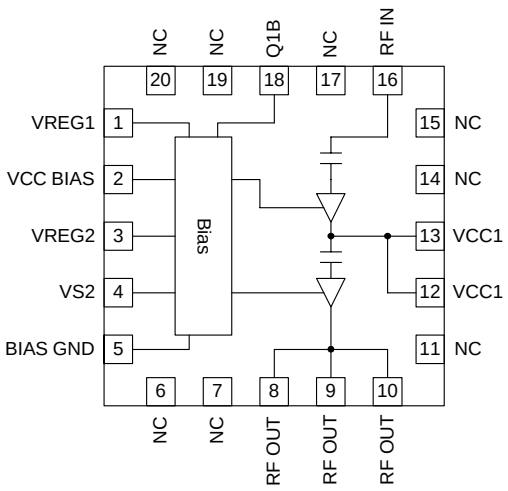


NOTES:
1. Shaded lead is Pin 1.
2. Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
3. Dimension applies to plated terminal: to be measured between 0.02 mm and 0.25 mm from terminal end.
4. Package Warpage: 0.05 mm max.
5. Die Thickness Allowable: 0.305 mm max.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: LCC, 20-Pin, 4x4



Functional Block Diagram

Features

- Single 3V Supply
- 27dBm Linear Output Power
- 26dB Linear Gain
- 40% Linear Efficiency
- On-board Power Down Mode

Ordering Information

RF5176	3V W-CDMA Power 1900MHZ/ 3V Linear Power Amplifier
RF5176 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

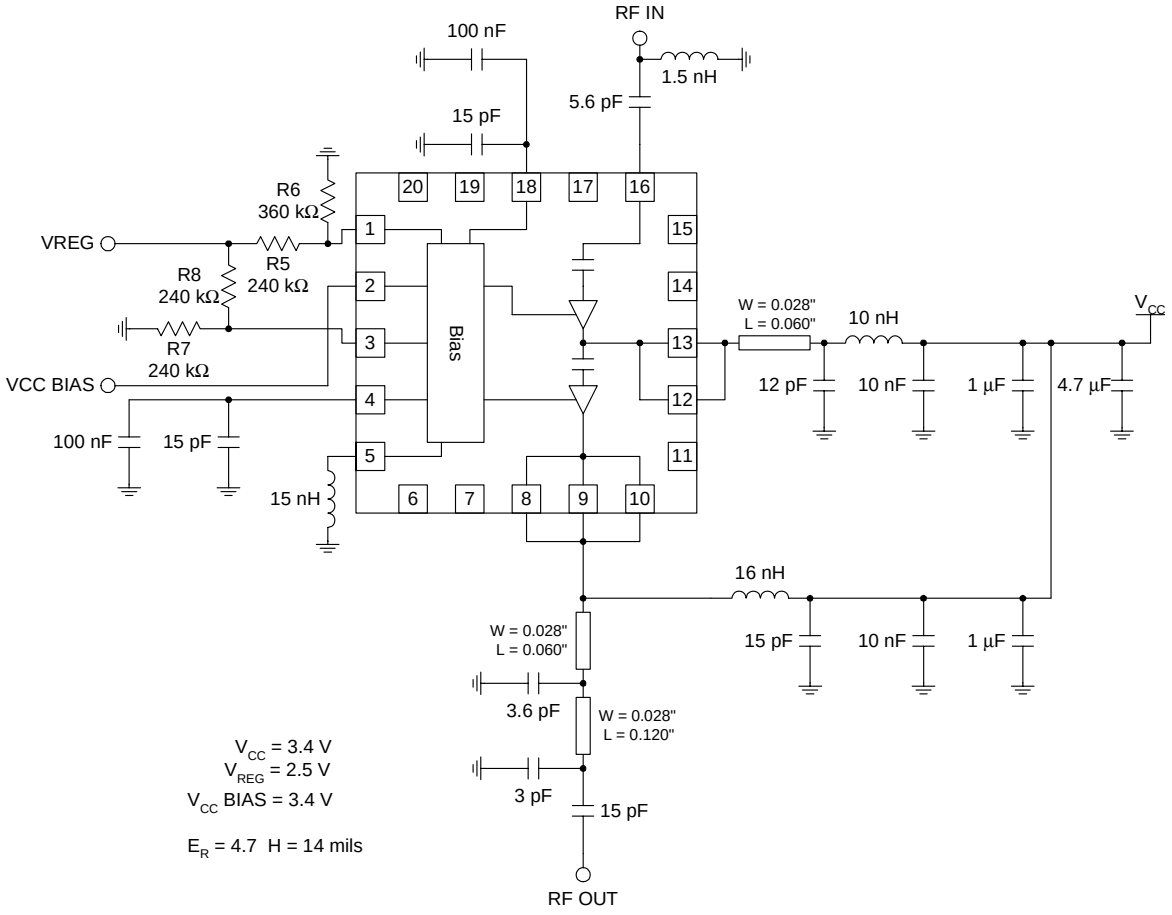
Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.0	V_{DC}
Bias Voltage (V_{BIAS})	+3.0	V_{DC}
Control Voltage (V_{REG})	+3.0	V_{DC}
Input RF Power	+6	dBm
Operating Case Temperature	-30 to +100	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, Freq=1920MHz to 1980MHz, V_{REG}=2.5V, unless otherwise specified
Usable Frequency Range	1850		2000	MHz	
Typical Frequency Range		1850 to 1910		MHz	
		1920 to 1980		MHz	
Linear Gain		26		dB	
Second Harmonic (including second harmonic trap)		-55		dBc	
Third Harmonic		-50		dBc	
Maximum Linear Output Power (W-CDMA Modulation)		27		dBm	
Total Linear Efficiency		40		%	P_{OUT}=27dBm
Adjacent Channel Power Rejection@5MHz		-40	-38	dBc	P_{OUT}=27dBm, W-CDMA Modulation, 3GPP 3.2 03-00 DPCCH + 1 DPDCH
Adjacent Channel Power Rejection@10MHz		-50	-48	dBc	P_{OUT}=27dBm, W-CDMA Modulation, 3GPP 3.2 03-00 DPCCH + 1 DPDCH
Noise Power		-144		dBm/Hz	P_{OUT}=+27dBm, Rx Band 2110MHz to 2170MHz
Input VSWR		< 2:1			
Output Load VSWR			5:1		No oscillations
Power Supply					
Power Supply Voltage	3.0	3.4	5.0	V	
Idle Current		80		mA	V_{REG}=2.5V
VREG Current		10		µA	Total pins 1 and 3, V_{REG}=2.5V
Turn On/Off time				ns	
Total Current (Power down)			10	µA	V_{REG}=Low
V_{REG} "Low" Voltage		0	0.2	V	
V_{REG} "High" Voltage		2.5		V	See Alternative Biasing Network table following the application schematic.

Pin	Function	Description	Interface Schematic
1	VREG1	Bias control for the first stage. Needs to be divided down from its nominal value of 2.5V using a resistive divider network of 240kΩ and 360kΩ. V_{REG1} and V_{REG2} may be adjusted to minimize idle current for a given output power. Alternative V_{REG} voltages can be used as defined on the application schematic.	
2	VCC BIAS	Supply for bias circuits.	
3	VREG2	Bias control for the second stage. Needs to be divided down from its nominal value of 2.5V using a resistive divider network of 240kΩ and 240kΩ. Alternative V_{REG} voltages can be used as defined on the application schematic.	
4	VS2	Second stage bias circuit source. For best linearity, decouple with bypassing capacitors of 15pF and 100nF.	
5	BIAS GND	Connect to ground plane via a 15nH inductor. DC return for the second stage bias circuit.	
6	NC	Not currently used.	
7	NC	Not currently used.	
8	RF OUT	RF output and power supply for the final stage. This is the unmatched collector of the final stage. It requires an output matching network, including a DC blocking capacitor.	
9	RF OUT	Same as pin 8.	
10	RF OUT	Same as pin 8.	
11	NC	Not currently used.	
12	VCC1	Power supply for the first stage and interstage match. Requires a shunt capacitor of 12pF close to the pin for optimum match.	
13	VCC1	Same as pin 12.	
14	NC	Not currently used.	
15	NC	Not currently used.	
16	RF IN	RF input. Requires a blocking capacitor and shunt inductor to provide 2:1 VSWR.	
17	NC	Not currently used.	
18	Q1B	Base bias for first stage. For best linearity, decouple with 15pF and 100nF capacitors.	
19	NC	Not currently used.	
20	NC	Not currently used.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic

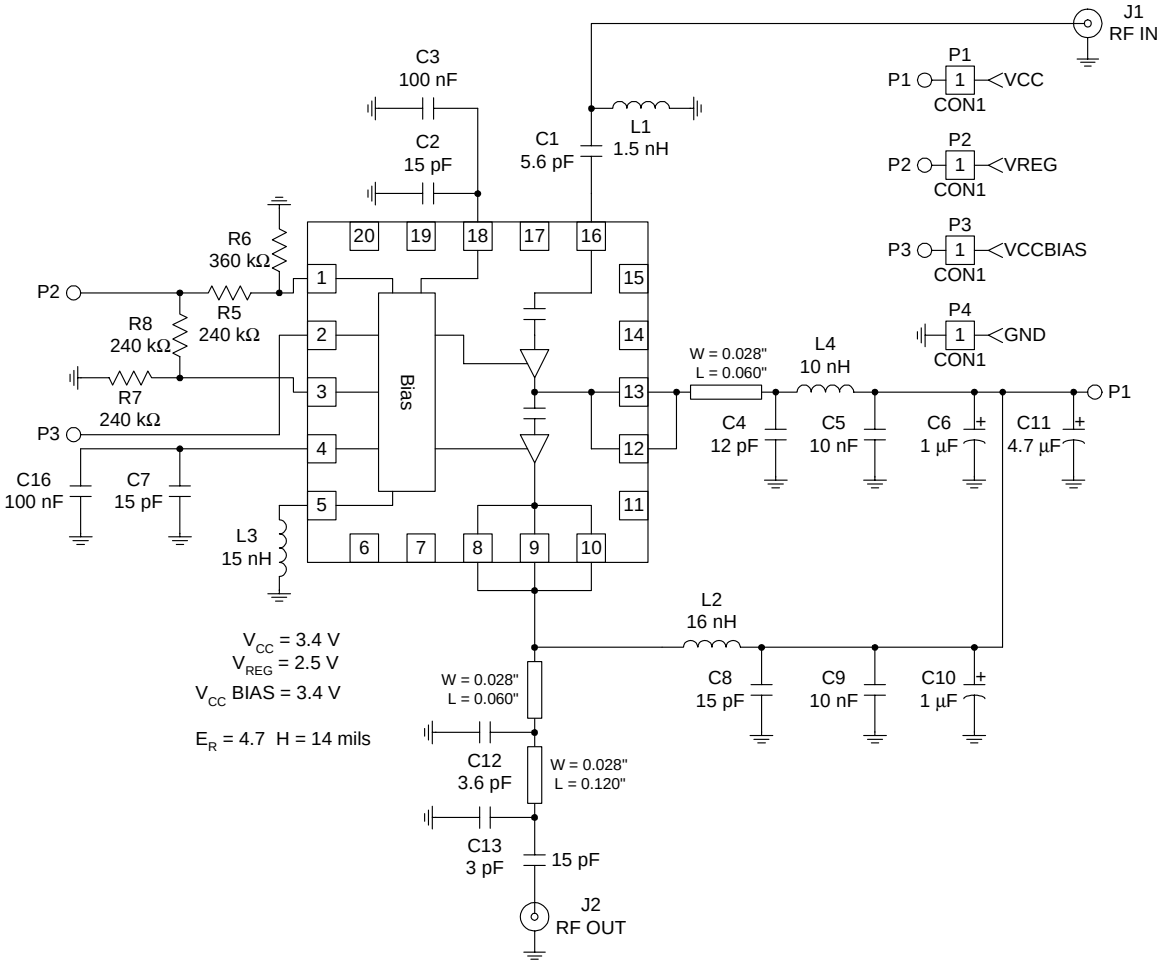


Alternative Biasing Networks for Various V_{REG} Voltages

V_{REG} (V)	R5 (1ST) kΩ	R6 (1ST-GND) kΩ	R7 (2ND-GND) kΩ	R8 (2ND) kΩ
2.50	240	360	240	240
2.60	240	330	360	380
2.70	240	300	200	230
2.80	240	270	220	270
2.90	220	240	180	240

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.028", Board Material FR-4, Multi-Layer
Ground Plane at 0.014"