RF9957

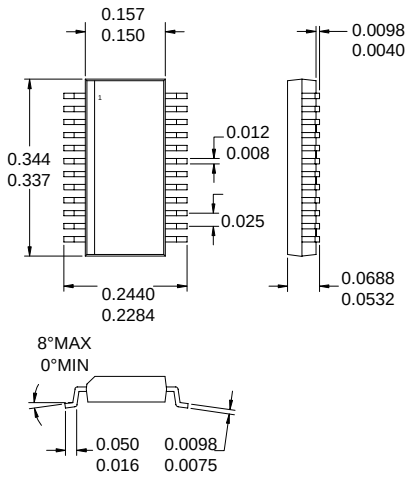
CDMA/FM RECEIVE AGC AND DEMODULATOR

Typical Applications

- CDMA/FM Cellular Systems
- CDMA PCS Systems
- Wireless Local Loop Systems
- Spread-Spectrum Cordless Phones
- High Speed Data Modems
- General Purpose Digital Receivers

Product Description

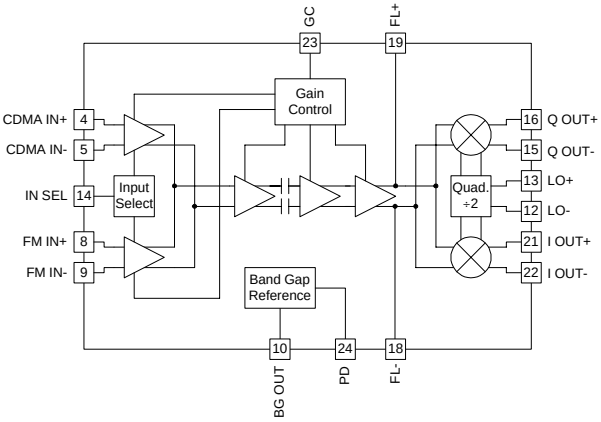
The RF9957 is an integrated complete IF AGC amplifier and Quadrature Demodulator designed for the receive section of dual-mode CDMA/FM cellular and PCS applications. It is designed to amplify received IF signals, while providing 100dB of gain control range, and demodulate to baseband I and Q signals. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98 and J-STD-018 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced 15GHz F_T Silicon Bipolar process, and is packaged in a standard miniature 24-lead plastic SSOP package.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation (CDMA and FM)
- Digitally Controlled Power Down Mode
- 2.7V to 3.3V Operation
- Quadrature LO Divider
- IF AGC Amp with 100dB Gain Control

Ordering Information

RF9957	CDMA/FM Receive AGC and Demodulator
RF9957 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
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http://www.rfmd.com

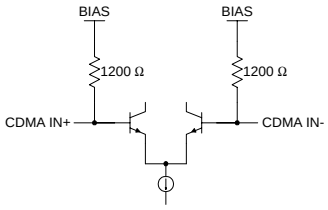
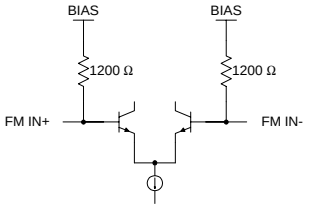
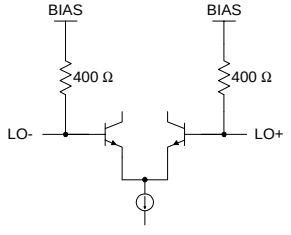
7 QUADRATURE DEMODULATORS

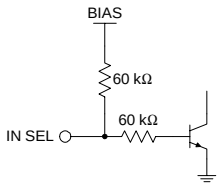
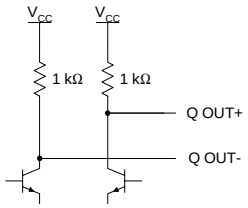
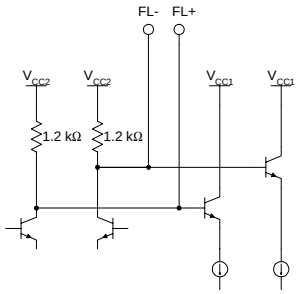
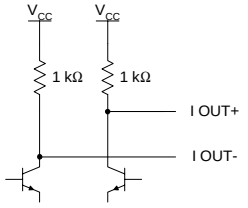
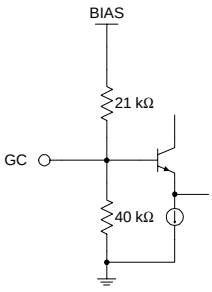
Absolute Maximum Ratings

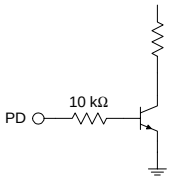
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}+0.7	V_{DC}
Input RF Power	+3	dBm
Ambient Operating Temperature	-40 to +85	℃
Storage Temperature	-40 to +150	℃

Caution! ESD sensitive device.

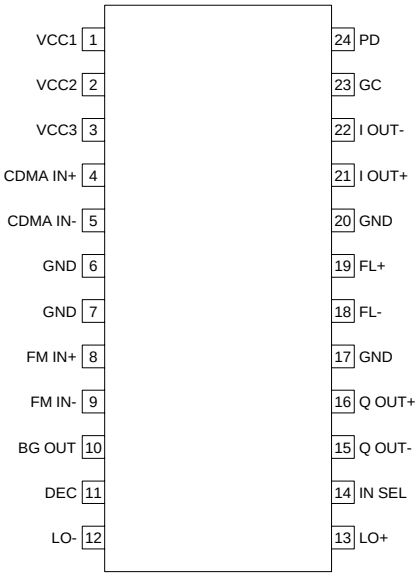
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (Cascaded)					T=25℃, V_{CC}=3.0V, Z_{LOAD}=5kΩ, LO=170MHz @400mV_{PP}, IF Freq=85MHz, Z_S=500Ω (CDMA), Z_S=850Ω (FM)
Maximum Gain	+45	+50		dB	V_{GC}=2.5V, FM or CDMA Input, Balanced
Minimum Gain		-55	-50	dB	V_{GC}=0.5V, FM or CDMA Input, Balanced
Gain Variation vs. V_{CC} and T	-3		+3	dB	V_{CC}=2.7V to 3.3V and T=-30℃ to +85℃
Input IP3		-50		dBm	V_{GC}=2.5V, Maximum Gain
	-39	-36		dBm	Gain = 35 dB, P_{IN}=-61dBm
		-4		dBm	V_{GC}=0.5V, Minimum Gain
Noise Figure		5		dB	V_{GC}=2.5V, Maximum Gain
		70		dB	V_{GC}=0.5V, Minimum Gain
IF Input Frequency Range		50 to 250		MHz	
IF Input Impedance	2040	2400	2760	Ω	FM or CDMA, Balanced
	1020	1200	1380	Ω	FM or CDMA, Single Ended
I/Q Frequency Range		0 to 50		MHz	
I/Q Amplitude Balance		0.1	0.5	dB	
I/Q Phase Balance		1	5	deg	
Max I/Q Output Voltage	500			mV_{PP}	Balanced, maximum output level
I/Q DC Output		2.0		V_{DC}	Common Mode
I/Q DC Offset		5	20	mV_{DC}	I OUT+ to I OUT-; Q OUT+ to Q OUT-
LO Input Frequency Range		100 to 500		MHz	
LO Input Level		60 to 600		mV_{PP}	Balanced
LO Input Impedance	680	800	920	Ω	Balanced
	340	400	460	Ω	Single Ended
Power Supply					
Supply Voltage	2.7	3.0	3.3	V_{DC}	
Current Consumption		14.5	18	mA	CDMA Mode
		12.5	16	mA	FM Mode
			10	μA	Sleep Mode (PD≤0.5V)

Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LO flip-flop divider and limiting amp. This pin may be connected in parallel with pins 2 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
2	VCC2	Supply voltage for the bandgap, gain control bias circuitry, and AGC stages 2, 3, and 4. This pin may be connected in parallel with pins 1 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
3	VCC3	Supply voltage for the FM and CDMA AGC input stages. This pin may be connected in parallel with pins 1 and 2. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
4	CDMA IN+	CDMA Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
5	CDMA IN-	Same as pin 4, except complementary input.	See pin 4.
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	GND	Same as pin 6.	
8	FM IN+	FM Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other FM input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
9	FM IN-	Same as pin 8, except complementary input.	See pin 8.
10	BG OUT	Bandgap Voltage Reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 10nF external bypass capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
12	LO-	LO Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The frequency of the signal applied to these pins is internally divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 400Ω (balanced is 800Ω). The LO input may be driven single-ended but balanced provides optimum gain and phase balance.	
13	LO+	Same as pin 12, except complementary input.	See pin 12.

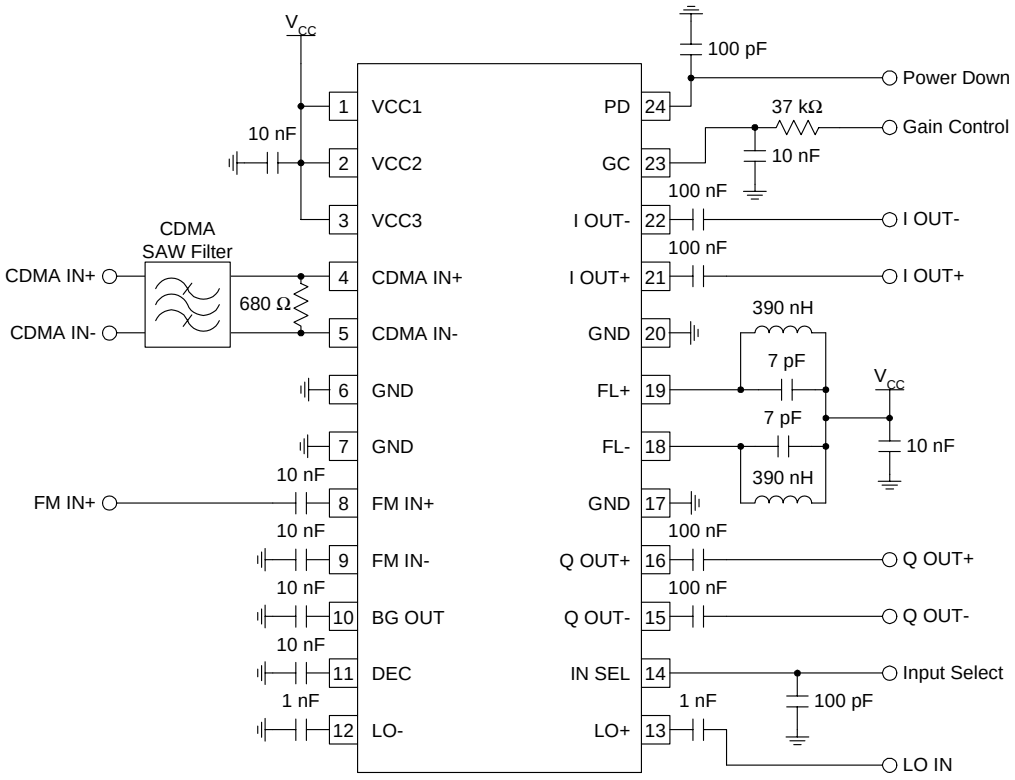
Pin	Function	Description	Interface Schematic
14	IN SEL	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" (≥VCC-0.7V_{DC}) selects CDMA mode. A logic "low" (<0.5V_{DC}) selects FM mode. In FM mode, ONLY the I mixer is active. There is no Q output in FM mode. The impedance on this pin is 30kΩ.	
15	Q OUT-	Balanced Baseband Output of Q Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in CDMA mode, but is NOT active in FM mode. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5kΩ. The balanced load should be 5kΩ. The single-ended output impedance is 1kΩ, while the balanced output impedance is 2kΩ.	
16	Q OUT+	Same as pin 15, except complementary output.	See pin 15.
17	GND	Same as pin 6.	
18	FL-	Balanced AGC Output/Demod Input. This balanced node is pinned out to allow shunt filtering of the AGC output signal as it enters the demodulator. The basic configuration of the filter should consist of a shunt inductor and shunt capacitor, both connected to the power supply, as the internal circuitry requires this power supply connection through the inductor to operate.	
19	FL+	Same as pin 18, except complementary.	See pin 18.
20	GND	Same as pin 6.	
21	I OUT+	Balanced Baseband Output of I Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in both CDMA and FM modes. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5kΩ. The balanced load should be 5kΩ. The single-ended output impedance is 1kΩ, while the balanced output impedance is 2kΩ.	
22	I OUT-	Same as pin 21, except complementary output.	See pin 22.
23	GC	Analog Gain Control for AGC Amplifiers. The valid control range is from 0.5 to 2.5V_{DC}. These voltages are valid for ONLY a 37kΩ source impedance. The gain range for the AGC is 95dB.	

Pin	Function	Description	Interface Schematic
24	**PD**	Power Down Control. When logic "high" ($\geq V_{CC}$-0.3V), all circuits are operating; when logic "low" ($\leq$0.5V), all circuits are turned off. The input impedance of this pin is 10kΩ.	

Pin Out

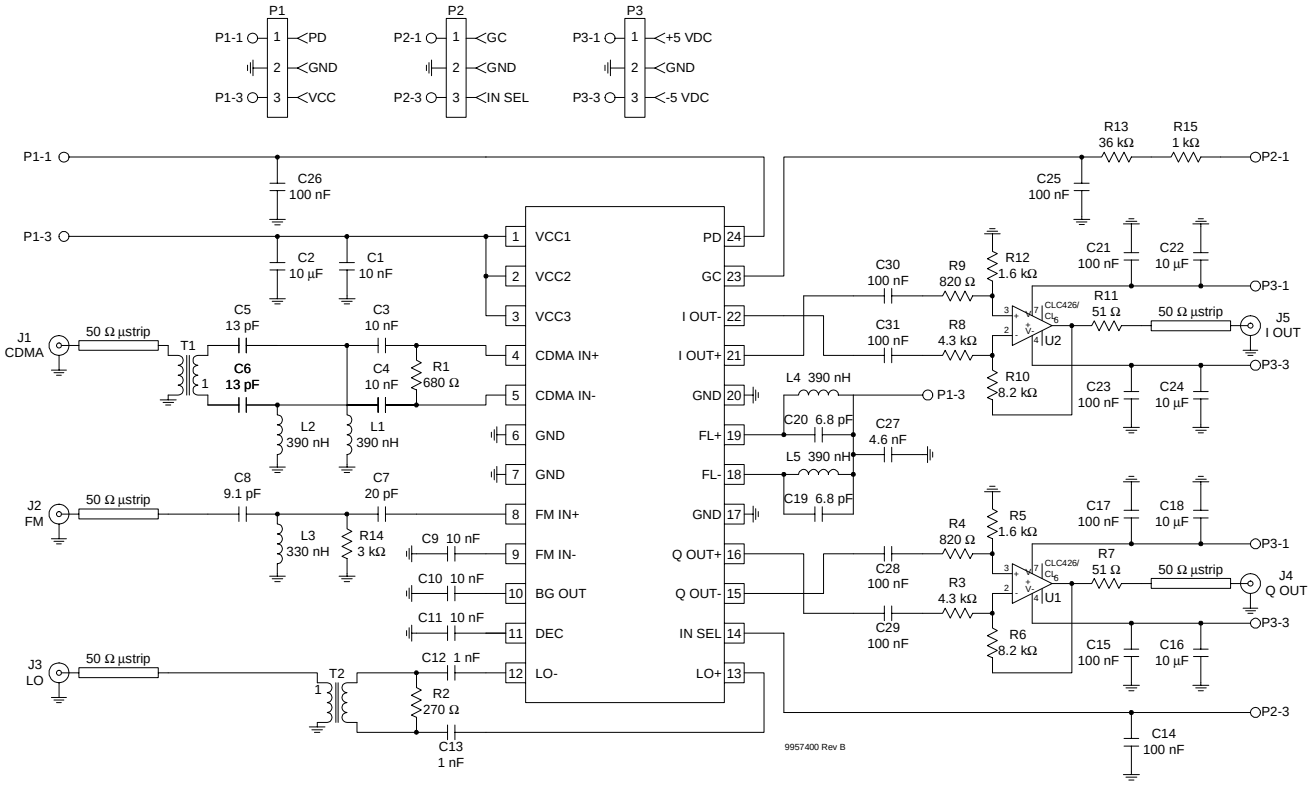


Application Schematic

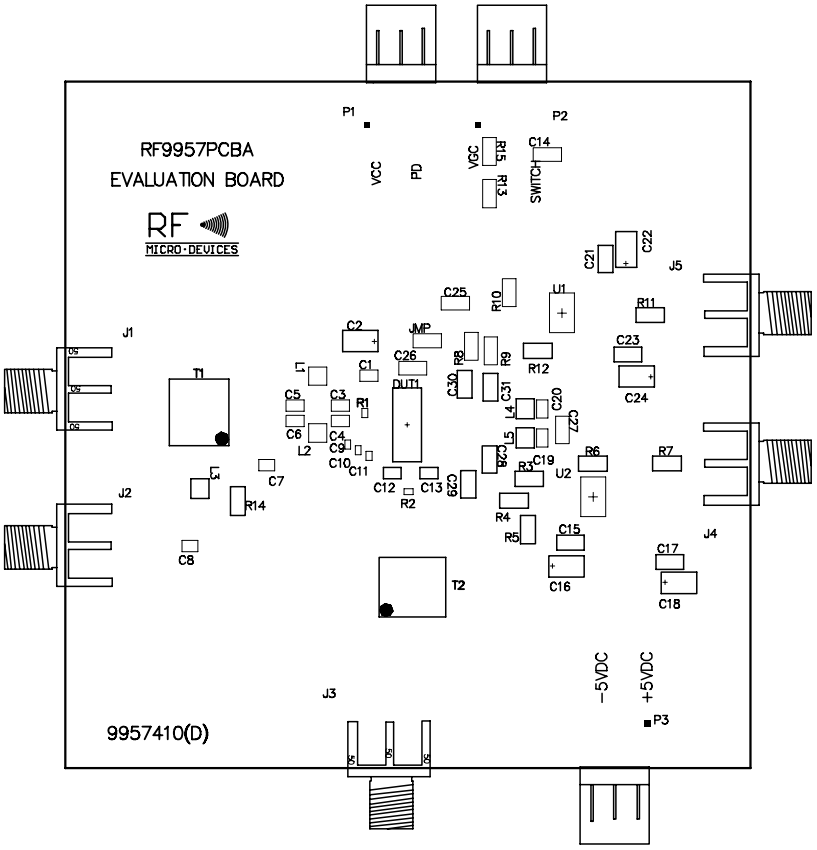


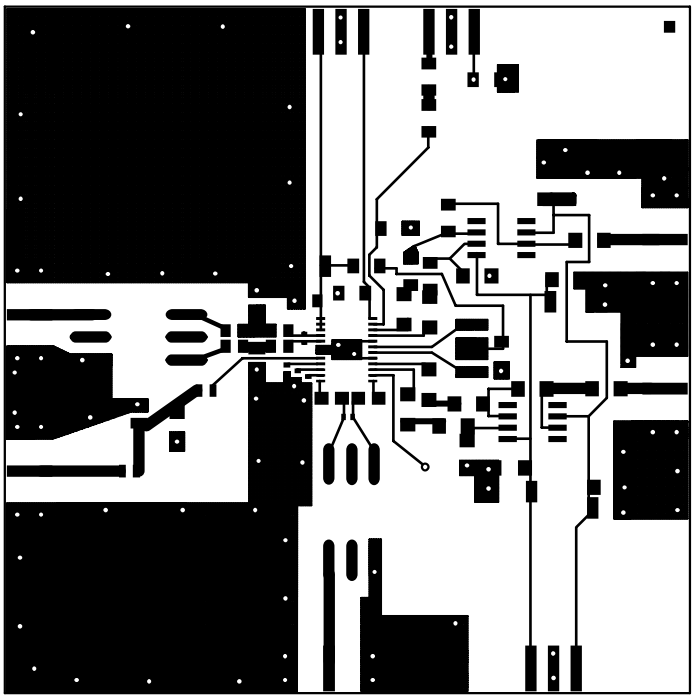
Evaluation Board Schematic

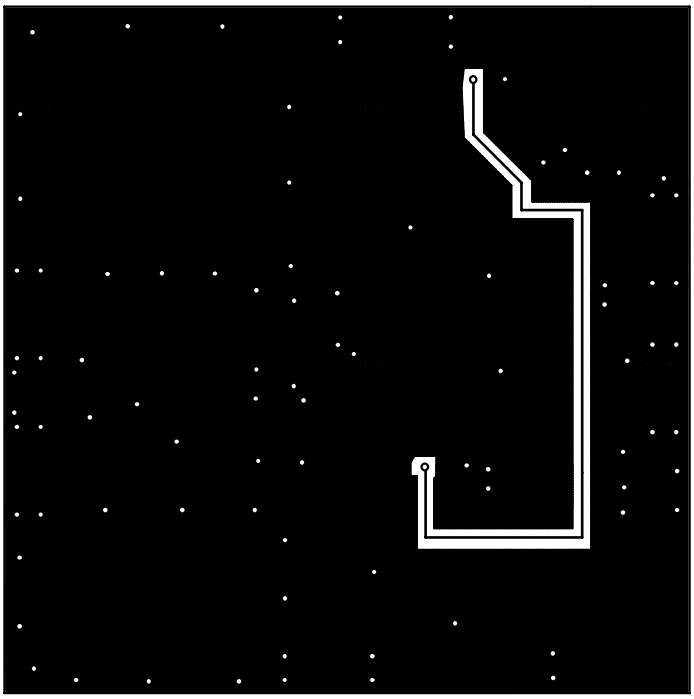
(Download Bill of Materials from www.rfmd.com.)



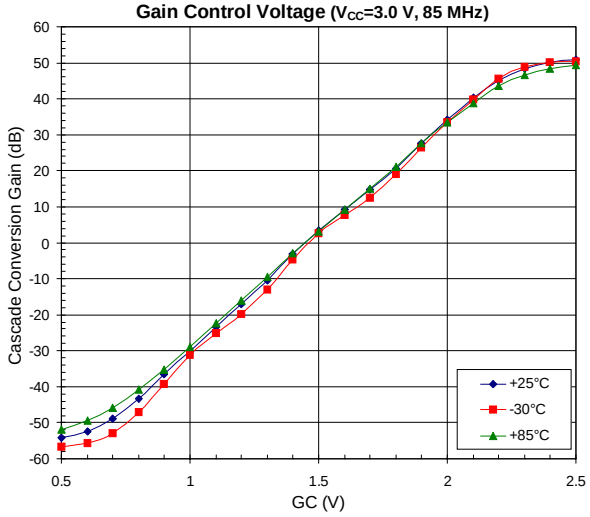
Evaluation Board Layout
Board Size 3.025” x 3.025”
Board Size 0.031”, Board Material FR-4



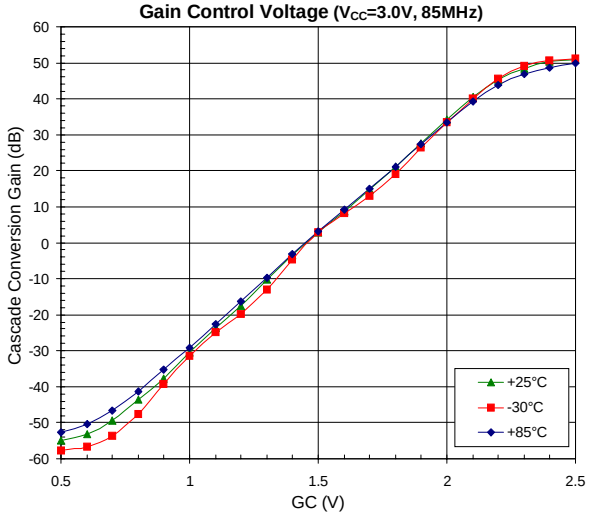




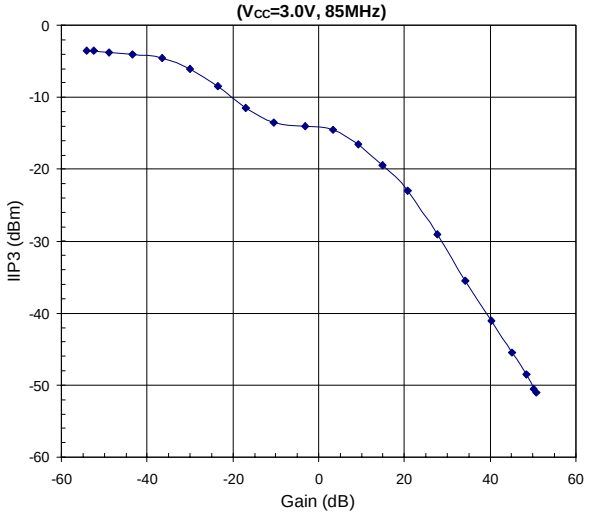
CDMA Cascade Conversion Gain versus Gain Control Voltage (V_{CC}=3.0 V, 85 MHz)



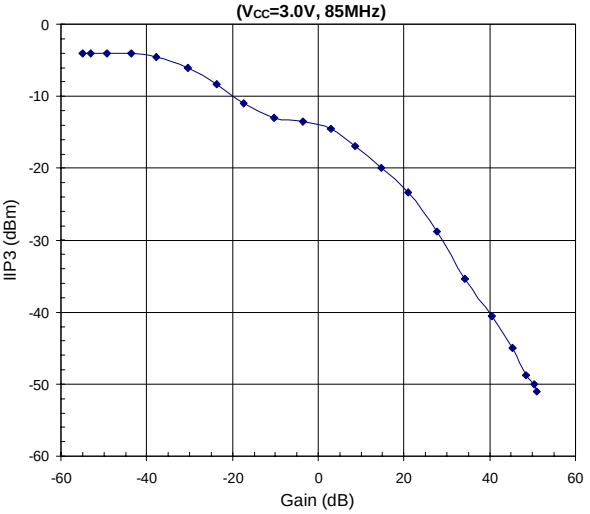
FM Cascade Conversion Gain versus Gain Control Voltage (V_{CC}=3.0V, 85MHz)



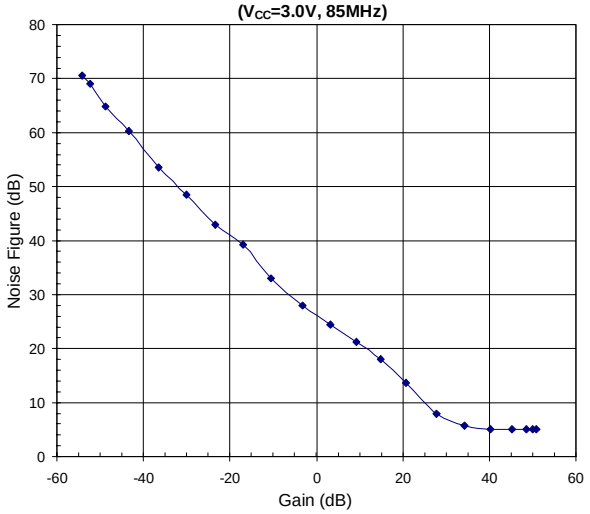
CDMA IIP3 versus Gain (V_{CC}=3.0V, 85MHz)



FM IIP3 versus Gain (V_{CC}=3.0V, 85MHz)



CDMA Noise Figure versus Gain (V_{CC}=3.0V, 85MHz)



FM Noise Figure versus Gain (V_{CC}=3.0V, 85MHz)