RF9958

CDMA/FM TRANSMIT MODULATOR, IF AGC, AND UPCONVERTER

Typical Applications

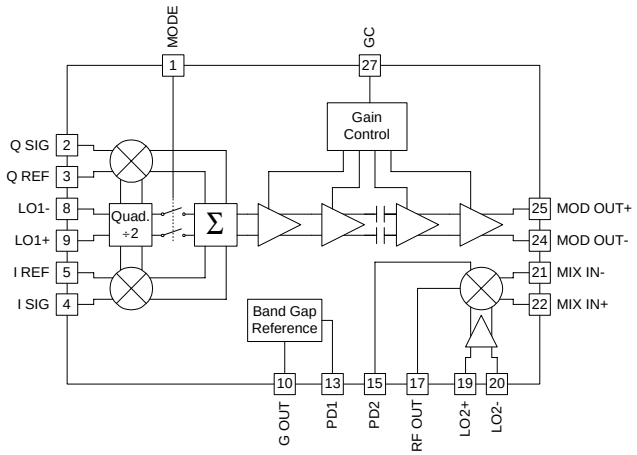
- CDMA/FM Cellular Systems
- CDMA PCS Systems
- Wireless Local Loop Systems
- Spread Spectrum Cordless Phones
- High Speed Data Modems
- General Purpose Digital Transmitters

Product Description

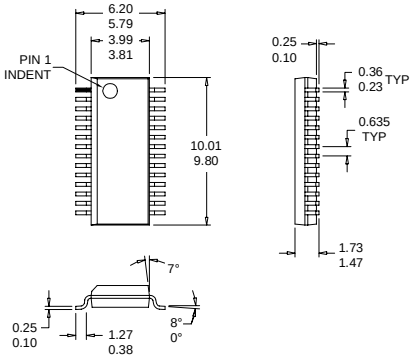
The RF9958 is an integrated complete Quadrature Modulator, IF AGC amplifier, and Upconverter designed for the transmit section of dual-mode CDMA/FM cellular and PCS applications. It is designed to modulate baseband I and Q signals, amplify the resulting IF signals while providing 95dB of gain control range, and perform the final upconversion to UHF. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-98 Interim Standard for CDMA cellular communications. This circuit is designed as part of RFMD's newest CDMA Chip Set, which also includes the RF9957 CDMA/FM Receive IF AGC and Demodulator. The IC is manufactured on an advanced 15GHz F_T Silicon Bipolar process, and is supplied in a 28-lead plastic SSOP package.

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] GaAs HBT
- [ ] GaAs MESFET
- [ ] Si Bi-CMOS
- [ ] SiGe HBT
- [ ] Si CMOS



Functional Block Diagram



NOTES:
1. Shaded lead is Pin1.
2. Lead frame material: Copper 194
3. Mold flash shall not exceed 0.006 (0.15 mm) per end.
4. Interlead flash shall not exceed 0.010 (0.25 mm) per side.
5. All dimensions are excluding mold flash and protrusions.

Package Style: QSOP-28

Features

- Supports Dual Mode Operation
- Digitally Controlled Power Down Modes
- 2.7V to 3.3V Operation
- Digital First LO Quadrature Divider
- Double-Balanced UHF Upconvert Mixer
- IF AGC Amp with 95 dB Gain Control

Ordering Information

RF9958	CDMA/FM Transmit Modulator, IF AGC, and Upconverter
RF9958 PCBA	Fully Assembled Evaluation Board

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5 MODULATORS AND UPCONVERTERS

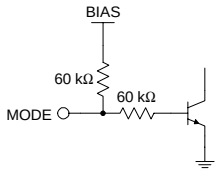
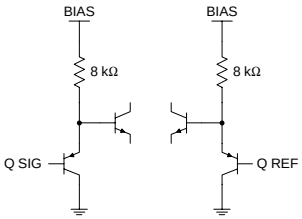
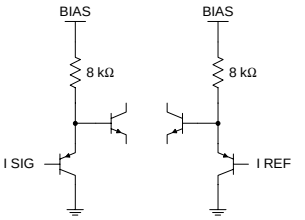
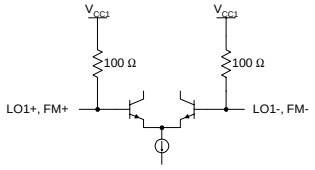
Absolute Maximum Ratings

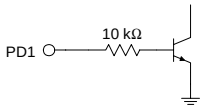
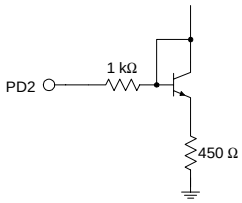
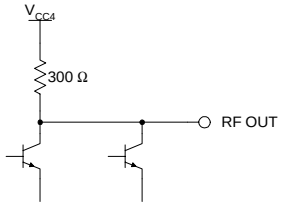
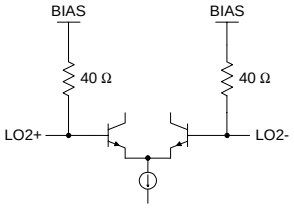
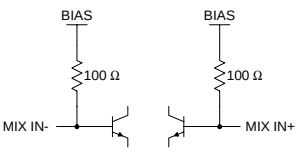
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC} + 0.7	V
I and Q Levels, per pin	1	V_{PP}
LO1 Level, balanced	+3	dBm
LO2 Level, balanced	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

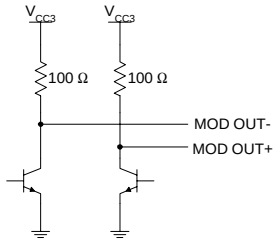
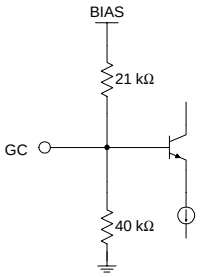
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
I/Q Modulator & AGC					T=25 °C, V_{CC}=3.0V, Z_{LOAD}=50Ω, LO1=-8dBm@260 MHz, LO2=-3dBm@960MHz, I SIG=Q SIG=300mV$_{PP}$, RF Output externally matched
I/Q Input Frequency Range		0 to 20		MHz	Balanced
I/Q Input Impedance	50	80	110	kΩ	Balanced
I/Q Input Reference Level		0.6		V_{DC}	Per Pin
LO1/FM Frequency Range		100 to 360		MHz	
LO1/FM Input Level	-15	-8	-5	dBm	
LO1/FM Input Impedance	170	200	230	Ω	Balanced
Sideband Suppression	35	40		dBc	I/Q Amplitude adjusted to within ±20mV
		30		dBc	Unadjusted
Carrier Suppression	40	50		dBc	I/Q DC Offset adjusted to within ±20mV
		30		dBc	Unadjusted
Max Output, FM Mode	+2.5	+4		dBm	V_{GC}=2.5 V_{DC}, T=-20°C to +85°C
Max Output, CDMA Mode	-3	0		dBm	V_{GC}=2.5 V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
	-2	0		dBm	ISIG=QSIQ=300mVpp@100kHz
Min Output, CDMA Mode		-95	-89	dBm	V_{GC}=0.5 V_{DC}, T=-20°C to +85°C, IS-95A CDMA Modulation
Output Power Accuracy	-3		+3	dB	T=-20 to +85 °C, Ref=25 °C
	-2		+2	dB	1.4V≤GC≤2.5
Adjacent Channel Power Rejection @ 885kHz		-55		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Adjacent Channel Power Rejection @ 1.98MHz		-67		dBc	IS-95A CDMA Modulation P_{OUT} = -5dBm
Output Noise Power		-116	-111	dBm/Hz	P_{OUT} = -3 dBm, T=-20°C to +85°C
		-137	-132	dBm/Hz	P_{OUT} = -23 dBm, T=-20°C to +85°C
		-164	-159	dBm/Hz	P_{OUT} < -70 dBm, T=-20°C to +85°C
Output Impedance	170	200	230	Ω	Balanced
Power Dissipation			150	mW	T=-20°C to +85°C
UHF Upconverter					Output externally matched
Conversion Gain	-1	0.5		dB	
Noise Figure (SSB)		15		dB	
Output IP3		+14		dBm	
IF Input Impedance	170	200	230	Ω	Balanced
IF Input Frequency Range		50 to 180		MHz	
LO2 Input Impedance		50		Ω	Single Ended
LO2 Input Level	-6	-3	0	dBm	
LO2 Input Frequency Range		700 to 1100		MHz	
RF to LO2 Isolation		20		dB	

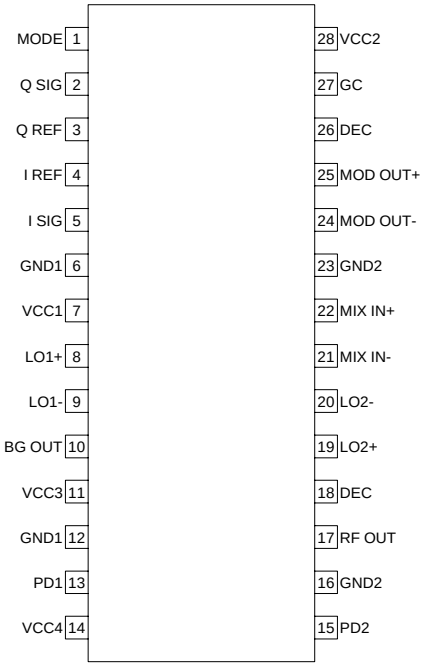
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		43		mA	Modulator and AGC only, CDMA Mode
Current Consumption		20		mA	Mixer Only
Power Down Current			20	µA	
VPD HIGH Voltage	V_{CC}-0.7			V	
VPD LOW Voltage			0.5	V	

Pin	Function	Description	Interface Schematic
1	MODE	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" ($\geq V_{CC}$-0.7V_{DC}) selects CDMA mode. A logic "low" (<0.5V_{DC}) selects FM mode. In FM mode, this switch enables the FM amplifier and turns off the I&Q modulator. The impedance on this pin is 30kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
2	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
3	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the Q SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 2.
4	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the I SIG DC voltage may be adjusted. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 5.
5	I SIG	Baseband input to the I mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50kΩ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
6	GND1	Ground connection for all baseband circuits including bandgap, AGC, flip-flop, modulator and FM amp. Keep traces physically short and connect immediately to ground plane for best performance.	
7	VCC1	Supply Voltage for the LO1 flip-flop and limiting amp only. This supply is isolated to minimize the carrier leakage. A 1nF external bypass capacitor is required, and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	LO1+, FM+	One half of the balanced modulator LO1 input. The other half of the input, LO1-, is AC grounded for single-ended input applications. The frequency on these pins is divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 100Ω (balanced is 200Ω). This pin is NOT internally DC blocked. An external blocking capacitor (1nF recommended) must be provided if the pin is connected to a device with DC present. When FM mode is selected, the output of the flip-flop divider circuit is switched to the AGC amplifier inputs and the modulator mixers are not used. Note that the frequency deviation input here will be reduced by a factor of two, due to the frequency divider operation.	
9	LO1-, FM-	One half of the balanced modulator LO1 input. In single-ended applications (100Ω input impedance), this pin is AC grounded with a 1nF capacitor.	See pin 8.

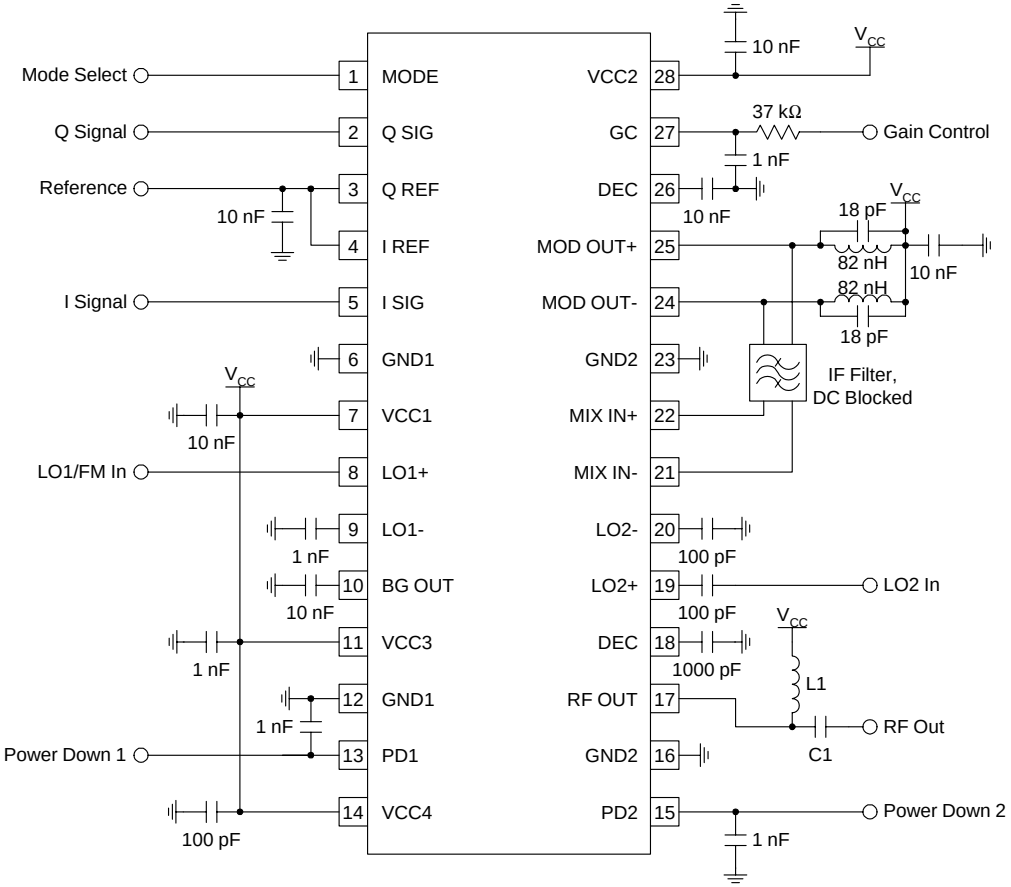
Pin	Function	Description	Interface Schematic
10	BG OUT	Bandgap voltage reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 1nF external bypass capacitor is required.	
11	VCC3	Supply voltage for the AGC and the Bandgap circuitry. A 1nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
12	GND1	Same as pin 6.	
13	PD1	Power down control for overall circuit. When logic "high" ($\geq V_{CC}$-0.7V), all circuits are operating; when logic "low" (≤0.5V), all circuits are turned off. The input impedance of this pin is >10kΩ. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
14	VCC4	Supply for the mixer stage only. The supply for the mixer is separated to maximize IF to RF isolations and reduce the carrier leakage. A 100pF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
15	PD2	Power down control for mixer only. When connected to pin 10 (BG OUT) the mixer circuits are operating; when connected to ground (≤0.5V), the mixer is turned off but all other circuits are operating. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
16	GND2	Ground connection for the mixer stage. Keep traces physically short and connect immediately to ground plane for best performance.	
17	RF OUT	RF output pin. An external shunt inductor to V_{CC} plus a series blocking/ matching capacitor are required for 50Ω output.	
18	DEC	Current Mirror decoupling pin. A 1000pF external capacitor is required to bypass this pin. The ground side of the bypass capacitors should connect immediately to ground plane.	
19	LO2+	One half of the balanced mixer LO2 input. In single-ended applications, the other half of the input, LO2- is AC grounded. This is a 50Ω impedance port. This pin is NOT internally DC blocked. An external blocking capacitor (100pF recommended) must be provided if the pin is connected to a device with DC present.	
20	LO2-	One half of the balance mixer LO2 input. In single ended applications, this pin is AC grounded with a 100pF capacitor.	See pin 19.
21	MIX IN-	One half of the 200Ω balanced impedance input to the mixer stage. This pin is NOT internally DC blocked. An external blocking capacitor (2200pF recommended) must be provided if the pin is connected to a device with DC present. If no IF filter is needed this pin may be connected to MOD OUT+ through a DC blocking capacitor. An appropriate matching network may be needed if an IF filter is used.	

Pin	Function	Description	Interface Schematic
22	MIX IN+	Same as pin 21, except complementary input.	See pin 21.
23	GND2	Same as pin 16.	
24	MOD OUT-	One half of the balanced AGC output port. The impedance of this port is 200Ω balanced. If no filtering is required, this pin can be connected to the MIX IN- pin through a DC blocking capacitor. This pin requires an inductor to V_{CC} to achieve full dynamic range. In order to maximize gain, this inductor should be a high-Q type and should be parallel resonated out with a capacitor (see application schematic). This pin is NOT DC blocked. A blocking capacitor of 2200pF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
25	MOD OUT+	Same as pin 24, except complementary output.	See pin 24.
26	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
27	GC	Analog gain control for AGC amplifiers. Valid control voltage ranges are from $0.5V_{DC}$ to $2.5V_{DC}$. The gain range for the AGC is 88dB. These voltages are valid ONLY for a 37kΩ source impedance. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
28	VCC2	Supply for the modulator stage only. A 10nF external bypass capacitor is required and an additional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	

RF9958 Pin-Out

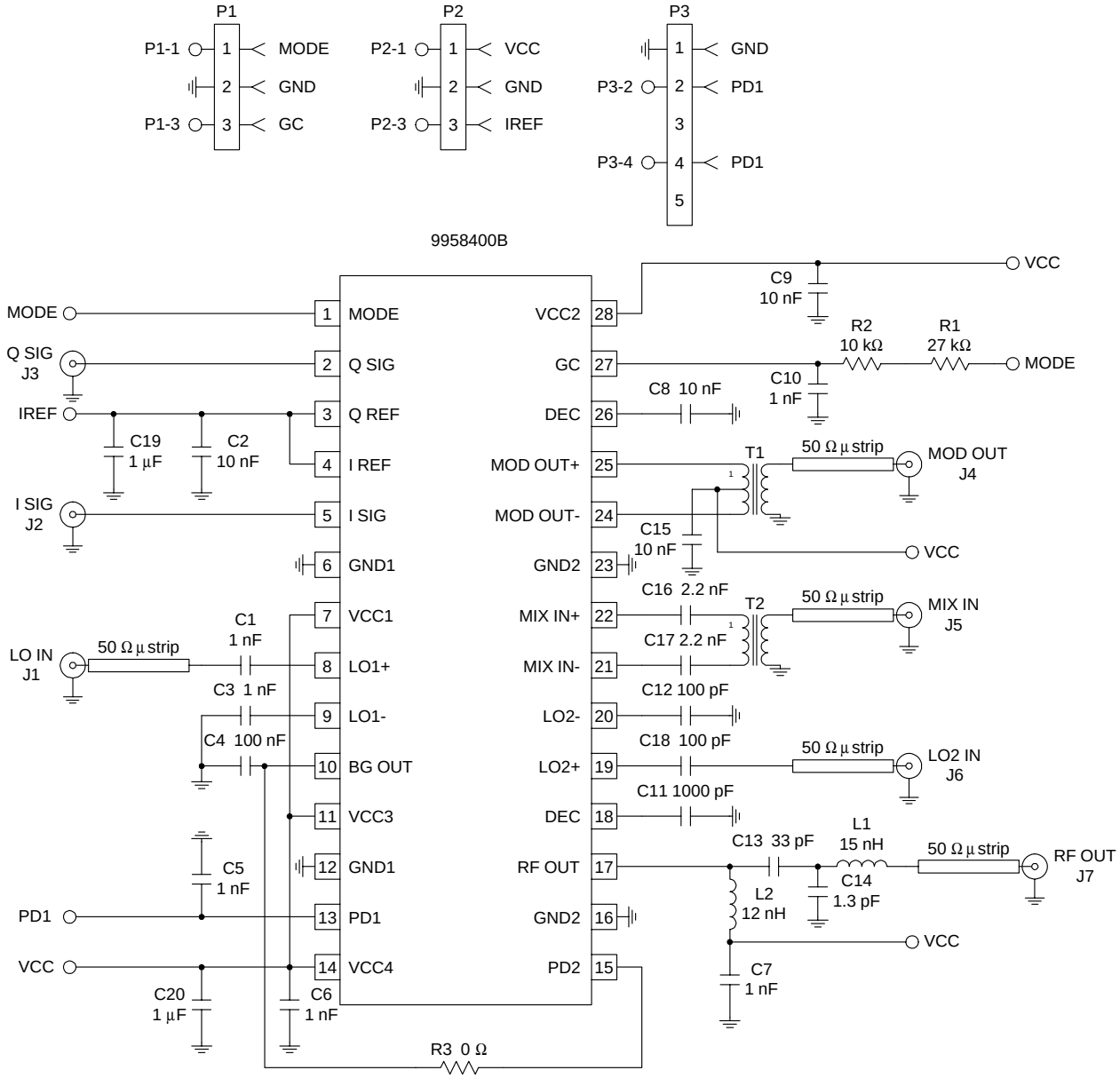


Application Schematic

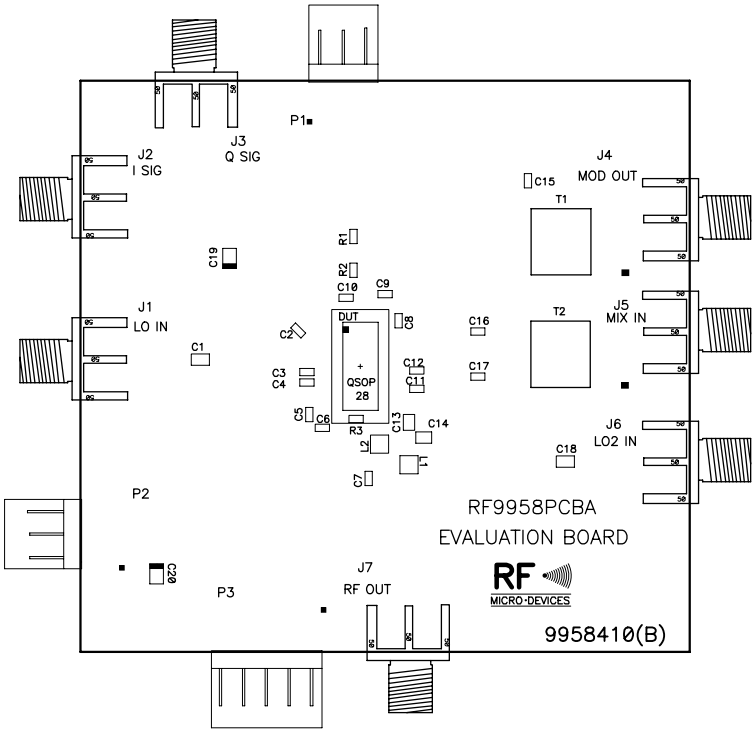


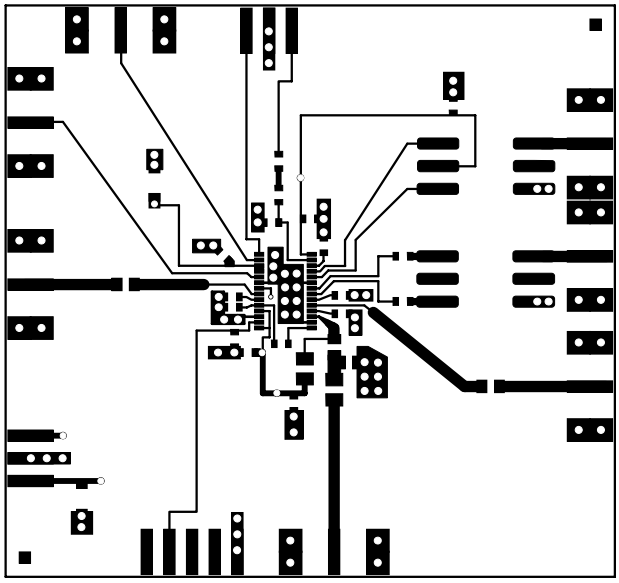
Evaluation Board Schematic

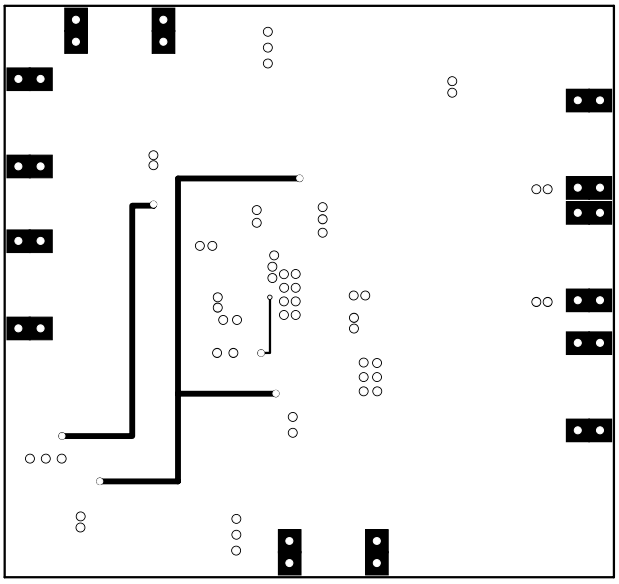
(Download Bill of Materials from www.rfmd.com.)



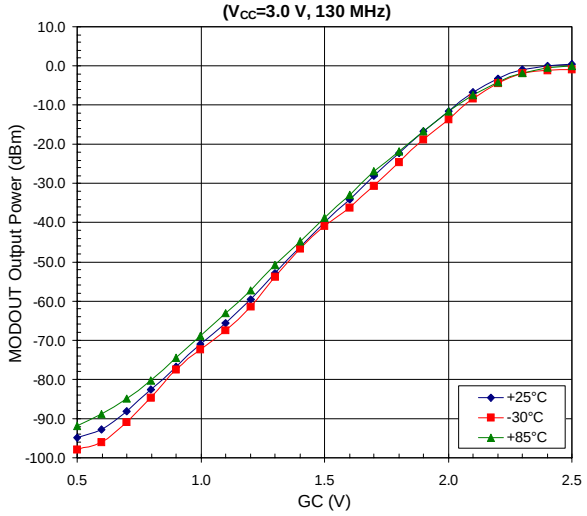
Evaluation Board Layout
2.689" X 2.521"



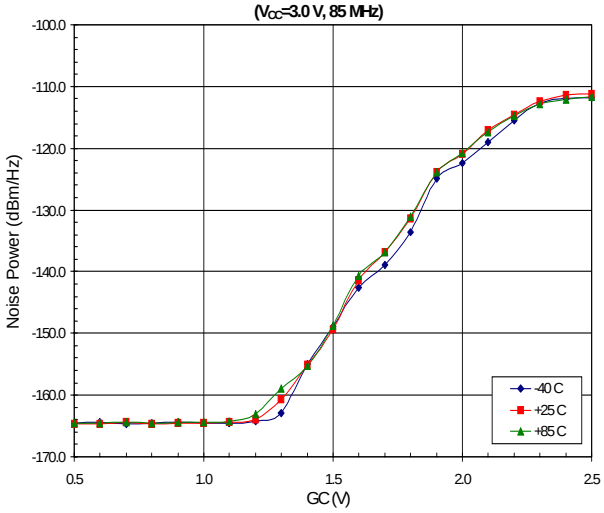




MODOUT Output Power versus Gain Control Voltage
(V_{CC}=3.0 V, 130 MHz)



MODOUT Noise Power versus Gain Control
(V_{CC}=3.0 V, 85 MHz)



MODOUT IM3 Suppression versus Output Level
(V_{CC}=3.0 V, 130 MHz)