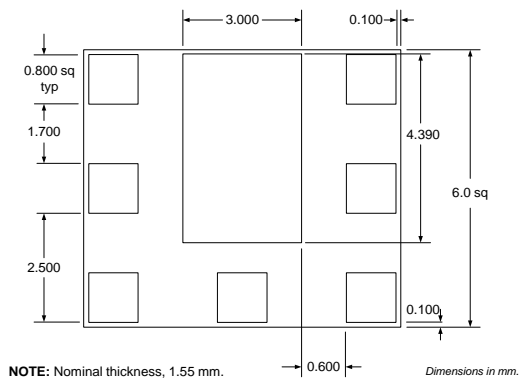


Typical Applications

- 3V CDMA Korean-PCS Handsets
- Spread-Spectrum Systems

Product Description

The RF3120 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Hetero-junction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA hand-held digital cellular equipment, spread-spectrum systems, and other applications in the 1750MHz to 1780MHz band. The RF3120 has a digital bias control voltage for low current in standby mode. The device is self-contained with 50Ω input and output that is matched to obtain optimum power, efficiency, and linearity characteristics. The module is an ultra-small 6mmx6mm land grid array with backside ground.



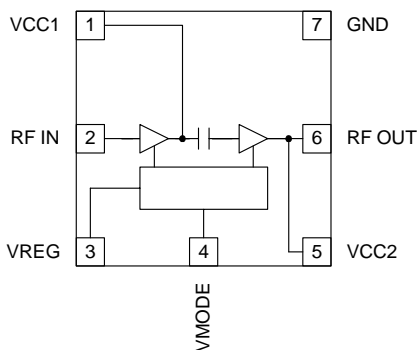
Optimum Technology Matching® Applied

- |                                     |  |                                      |
|-------------------------------------|--|--------------------------------------|
| <input type="checkbox"/> Si BJT     | <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET |
| <input type="checkbox"/> Si Bi-CMOS | <input type="checkbox"/> SiGe HBT            | <input type="checkbox"/> Si CMOS     |

Package Style: LGM (6mmx6mm)

**Features**

- Input/Output Internally Matched @ 50Ω
- Single 3V Supply
- 29dBm Linear Output Power
- 26dB Linear Gain
- 32% Linear Efficiency



Functional Block Diagram

**Ordering Information**

RF3120	3V 1800MHz Linear Amplifier Module
RF3120 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.  
7628 Thorndike Road  
Greensboro, NC 27409, USA

Tel (336) 664 1233  
Fax (336) 664 0454  
<http://www.rfmd.com>

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V <sub>DC</sub>
Supply Voltage (P <sub>OUT</sub> ≤29dBm)	+4.5	V <sub>DC</sub>
Control Voltage (V <sub>REG</sub> )	+4.2	V <sub>DC</sub>
Mode Voltage (V <sub>MODE</sub> )	+3.5	V <sub>DC</sub>
Input RF Power	+10	dBm
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-30 to +150	°C



**Caution!** ESD sensitive device.

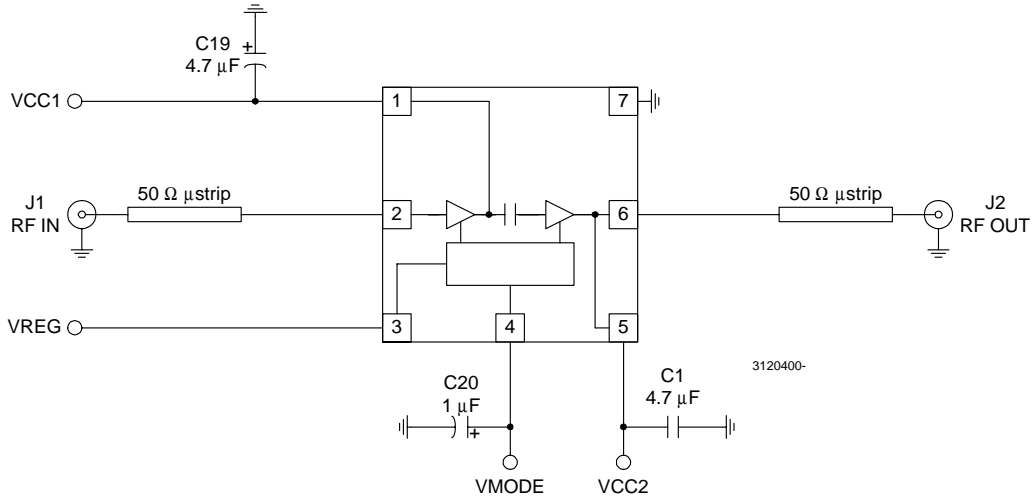
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.8V, V <sub>MODE</sub> =2.8V, Freq=1750MHz to 1780MHz unless otherwise specified
Frequency Range	1750		1780	MHz	
Linear Gain	22	26		dB	
Second Harmonic			-35	dBc	
Third Harmonic			-40	dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency	30	32		%	
Adjacent Channel Power Rejection			-44	dBc	ACPR @ 1250kHz
Input VSWR		<2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations.
Noise Figure			8	dB	
Noise Power			-95	dBm/30kHz	At 90MHz offset.
<b>Power Supply</b>					
Power Supply Voltage	3.2	3.4	4.5	V	
Quiescent Current		100		mA	
V <sub>REG</sub> Current			6	mA	Pin 3, V <sub>REG</sub> =2.8V
Turn On/Off Time			40	μs	
Total Current (Power down)			10	μA	V <sub>REG</sub> =low
V <sub>REG</sub> "Low" Voltage		0	0.2	V	
V <sub>REG</sub> "High" Voltage	2.7	2.8	2.9	V	

Pin	Function	Description	Interface Schematic
1	VCC1	First stage collector supply. A low frequency decoupling capacitor (e.g., 4.7 $\mu$ F) is required.	
2	RF IN	RF input internally matched to 50 $\Omega$ . This input is internally AC-coupled.	
3	VREG	Regulated voltage supply for amplifier bias.	
4	VMODE	For nominal operation, V <sub>MODE</sub> is set to HIGH. When set LOW: V <sub>MODE</sub> will increase the bias current by approximately 50%; and, large signal gain is increased by approximately 1.5dB.	
5	VCC2	Output stage collector supply. A low frequency decoupling capacitor (e.g., 4.7 $\mu$ F) is required.	
6	RF OUT	RF output internally matched to 50 $\Omega$ . This output is internally AC-coupled.	
7	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

## Evaluation Board Schematic

(Download [Bill of Materials](http://www.rfmd.com) from [www.rfmd.com](http://www.rfmd.com).)



Evaluation Board Layout  
Board Size 2.0" x 2.0"  
Board Thickness 0.028", Board Material FR-4

