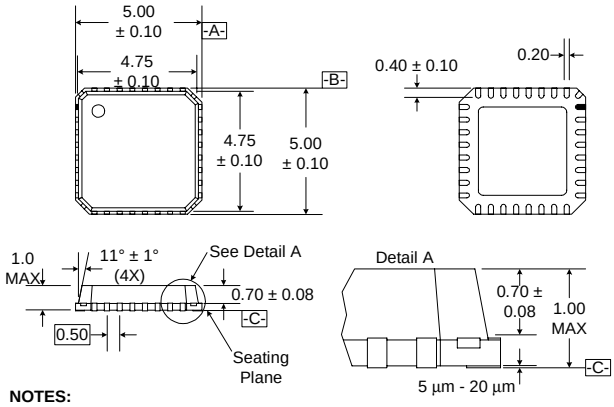
Typical Applications

- *Bluetooth* GSM/GPRS/EDGE Cellular Phones
- *Bluetooth* Wireless LAN
- Cordless Phones
- Battery-Powered Portable Devices

Product Description

The RF2968 is a monolithic integrated circuit intended for use as a low-cost FSK transceiver in *Bluetooth* applications. The device is provided in 32-lead plastic LPCC packaging and is designed to provide a fully-functional FSK transceiver. The chip is intended for *Bluetooth* applications in the 2.4GHz to 2.5GHz ISM band. The IF and demodulation sections of the chip require no external filters or discriminators. The chip also features an image reject front end and a fully programmable synthesizer with integrated oscillator circuitry. Self-calibrating RX and TX IF circuitry optimizes link performance and eliminates manufacturing variations.

BLUETOOTH is a trademark owned by the Bluetooth SIG, Inc., and licensed to RF Micro Devices, Inc.

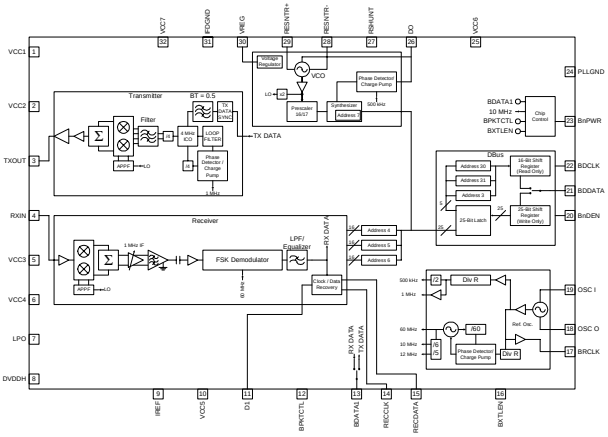


NOTES:
1. Shaded lead indicates Pin 1.
2. Package surface roughness at 1.5 µm ± 0.30.

Package Style: LCC, 32-Pin, 5x5

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Transceiver
- Self-Calibrating Transceiver
- Image Reject Receiver
- *Bluetooth* and BlueRF compatible
- Supports Reference Clocks to 40MHz
- Smallest Footprint *Bluetooth* Transceiver

Ordering Information

TBD

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

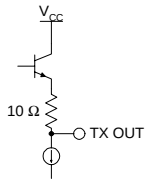
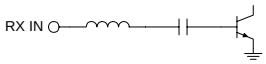
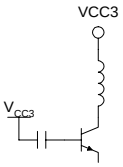
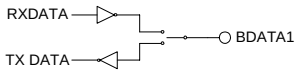
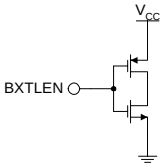
Parameter	Ratings	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to V_{CC}	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-55 to +125	°C

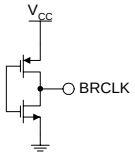
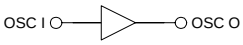
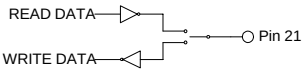
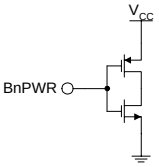
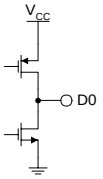
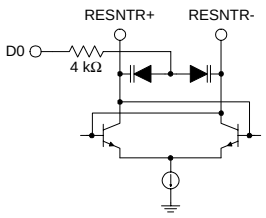
Caution! ESD sensitive device.

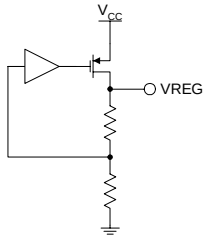
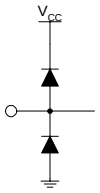
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V
RF Frequency Range		2400 to 2500		MHz	
VCO and PLL Section					
VCO Frequency Range		1100 to 1350		MHz	
Frequency Tolerance	-50		50	kHz	20ppm crystal; -40°C to +85°C
RF Channels		79			
Step Size		1		MHz	Freq=2.4GHz
SSB Phase Noise		-90		dBc/Hz	Freq=2.4GHz, 500kHz Offset
		-110		dBc/Hz	Freq=2.4GHz, 2MHz Offset
		-124		dBc/Hz	Freq=2.4GHz, 3MHz Offset
Reference Frequency	10	13	20	MHz	10, 11, 12, 13, 20MHz
	20	26	40	MHz	Div2ENB=0; 20, 22, 24, 26, 40MHz.
Hop Time		130	175	µs	Dual BW=75kHz and 25kHz; BW switch delay=100µs
K_{VCO}		85		MHz/V	VCO Freq=1.2GHz
Transmit Section					
Data Rate		1		Mbps	
Output Power		0	4	dBm	
Power Control Range		28		dB	
Power Control Step Size		4		dB	
Gain Step Switching Time		4		µs	From -28dB to 0dB
Output Impedance	25	50	100	Ω	VSWR<2:1
Deviation	140	160	175	kHz	Peak, Data Sequence 00001111
	115			kHz	Peak, Data Sequence 01010101
Transmit ISI					Data Sequence 1010
Min Freq Dev, % EYE Open	80		100	%	Reference Data Sequence 00001111
Zero Crossing Error	-125		125	ns	±1/8 Symbol
In-Band Spurious					Measurement BW=100kHz
Adjacent Channel Power			-20	dBc	
Second Channel Power			-20	dBm	
≥Third Channel Power			-40	dBm	
Out-of-Band Spurious					Measurement BW=100kHz
Operation			-36	dBm	30MHz to 1GHz
			-30	dBm	1GHz to 12.75GHz
			-47	dBm	1.8GHz to 1.9GHz
			-47	dBm	5.15GHz to 5.3GHz
Idle			-57	dBm	30MHz to 1 GHz
			-47	dBm	1GHz to 12.75 GHz
			-47	dBm	1.8GHz to 1.9GHz
			-47	dBm	5.15GHz to 5.3GHz

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Receive Section					
Cascaded Voltage Gain	18		64	dB	
Cascaded Noise Figure		8		dB	
Cascaded Input IP_3		-14		dBm	
RX Sensitivity		-85		dBm	IF BW=1MHz, BER=10^{-3}
Image Rejection		30		dB	
RX Input Impedance	25	50	100	Ω	2:1 VSWR max.
Interference Performance					BER<10^{-3} (C=Desired Signal/I=Interferer)
Co-Channel Interference, $C/I_{CO\text{-}Channel}$			14	dB	C=-60dBm
Adjacent (1MHz) Interference, C/I_{1MHz}			+4	dB	C=-60dBm
Adjacent (2MHz) Interference, C/I_{2MHz}			-30	dB	C=-60dBm
Adjacent (≥3MHz) Interference, $C/I_{\geq 3MHz}$			-40	dB	C=-67dBm
Image Frequency Interference, C/I_{image}			-9	dB	C=-67dBm
Adjacent (1MHz) Interference to In-Band Image, $C/I_{image\pm 1MHz}$			-20	dB	C=-67dBm
Out-of-Band Blocking					BER<10^{-3}, C=-67dBm, tested per evaluation board schematic
Interfering Signal Frequency					
30MHz to 2000MHz	-10			dBm	
2000MHz to 2400MHz	-27			dBm	
2500MHz to 3000MHz	-27			dBm	
3000MHz to 12.75GHz	-10			dBm	
Intermodulation Characteristic					BER<10^{-3} (BT=*Bluetooth* Modulated Signal)
f1, f2	-39			dBm	f0=-64dBm BT signal f1=sine f2=BT signal |f2-f1|=3MHz, 4MHz or 5MHz f0=2f1-f2
Maximum Usable Level	-20			dBm	BER<10^{-3}
Spurious Emissions					Measurement BW=100kHz
30MHz to 1GHz			-57	dBm	
1GHz to 12.75GHz			-47	dBm	
RSSI Operating Range	-80		-20	dBm	Power level at RX IN pin
RSSI Resolution		1		dB	
RSSI Absolute Accuracy	-4		4	dB	-60dBm input power
Front End					
Voltage Gain	25.5	27.5	29.5	dB	
Power Gain		20		dB	
Noise Figure		6	8.5	dB	
IIP3		-14		dBm	
IF Section					
IF Frequency		1		MHz	
Voltage Gain	-9.5		37	dB	Followed by 1 bit A/D
Noise Figure		25		dB	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Data Voltages					Z_{LOAD}>10kΩ
Logic Low			0.3	V	
Logic High	V_{CC}-0.3			V	
Power Supply					
Voltage	2.5	3.3	3.6	V	
TX Current Consumption		49		mA	Transmit mode, +4dBm output power
RX Current Consumption		49		mA	Receive mode
Sleep Modes		1		µA	Sleep mode, no low power clock
		250		µA	Sleep mode, low power clock, 12MHz reference
		750		µA	Sleep mode, low power clock, other reference

Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the VCO doubler and LO amplifier circuits.	
2	VCC2	Supply voltage for the RX mixers, TX PA, and LNA bias circuits.	
3	TX OUT	Transmitter output. TX OUT output impedance is 50Ω (nominal) when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled. Because this pin is DC-biased, an external coupling capacitor is required.	
4	RX IN	Receiver input. RX IN input impedance is a low impedance when the receiver is enabled. RX IN is a high impedance when the receiver is disabled. An internal series inductor is used to tune the input impedance.	
5	VCC3	Supply voltage for the RX input stage (LNA).	
6	VCC4	Supply voltage for the TX mixers and bias circuits of the LO amplifier, LNA, and RX mixers.	
7	LPO	Low frequency clock output for low power mode. In sleep mode, this pin may provide either a 3.2kHz or 32kHz clock having a 50% duty cycle to the baseband. In other modes, the output is disabled.	
8	DVDDH	Supply voltage for the RX IF VGA circuit.	
9	IREF	Connects an external precision resistor (1% tolerance) for generation of a constant current reference.	
10	VCC5	Supply voltage for the analog IF circuits.	
11	D1	This is the output of the charge pump for clock recovery circuit. A RC network from this pin to ground is used to establish the PLL bandwidth.	See pin 26.
12	BPKTCTL	In transmit mode, this pin is used as a strobe to enable the PA stage. In receive mode, the baseband has the option to use this pin to signal the detection of the sync word. The baseband drives this pin high at the end of the sync word, at which time a second DC estimation is performed by sampling the trailer bits. If baseband control is not desired to signal the second DC estimation, then an internal timer is used to mark the end of the sync word. The BBC bit is used to select the baseband control option; the default setting uses the internal timer.	See pin 23.
13	BDATA1	Input data to transmitter/output data from receiver. The input data is unfiltered data at 1MHz data rate. The pin is bidirectional, switching between data in and data out modes during Transmit and Receive modes respectively.	
14	RECCLK	Recovered clock output.	See pin 17.
15	RECDATA	Recovered data output.	See pin 17.
16	BXTLEN	This pin is part of the chip power control circuit. It is used to enable/disable “sleep” mode of chip.	

Pin	Function	Description	Interface Schematic
17	BRCLK	Reference clock output. This is a crystal controlled reference clock in the 10-40MHz range, typically 13MHz.	
18	OSC O	Same as pin 19.	See pin 19.
19	OSC I	The OSC pins are used to produce the reference frequency by means of negative feedback. A crystal and resistor are placed in parallel from OSC I to OSC O to provide the feedback path and establish the resonant frequency. A shunt capacitor is placed on each OSC pin to provide the proper loading of the crystal. If an external reference is used, it is connected to OSC I through a DC-blocking capacitor, and OSC O is connected to OSC I through a 470kΩ resistor.	
20	BnDEN	Latches data entered into the serial port. Data is clocked into the latch on the rising edge of BnDEN.	See pin 23.
21	BDDATA	Serial data port. Read/write data is sent through this pin into / out of the on chip shift register. Read data is transferred on the rising edge of BDCLK. Write data is transferred on the falling edge of BDCLK.	
22	BDCLK	Serial port input clock.This pin is used to clock data into the serial port. To minimize the hop frequency programming time, a BDCLK frequency of 10-20MHz is recommended.	See pin 23.
23	BnPWR	This pin is part of the chip power control circuit. It is used to power up the chip from the “off” state.	
24	PLL GND	Ground connection for the RF synthesizer, crystal oscillator, and serial port.	
25	VCC6	Supply voltage for the RF synthesizer, crystal oscillator, and serial port.	
26	D0	This is the output of the charge pump for the RF PLL. An RC network from this pin to ground is used to establish the PLL bandwidth. To minimize synthesizer settling time and phase noise, a dual loop bandwidth scheme is implemented. During the initial period of frequency acquisition, a wide loop bandwidth is used. RSHUNT is used to switch to a narrow loop bandwidth near the end of the frequency acquisition, providing improved VCO phase noise. The time at which the bandwidth switches is set by the PLLDel bits.	
27	RSHUNT	Switches the loop filter from wide to narrow bandwidth by shunting the midpoint of two external series resistors to ground.	
28	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Two inductors are required between RESNTR- and RESNTR+ to resonate with the internal capacitance. Inductance of traces from the RESNTR pins to the inductor should be taken into account in the board layout.	

Pin	Function	Description	Interface Schematic
29	RESNTR+	See pin 28.	
30	VREG	Voltage Regulator Output (2.2V). A bypass capacitor from this pin to ground is required. This voltage is used to bias the VCO through the tank circuit tied to pins 28 and 29.	
31	IFDGND	Ground connection for the digital IF circuits.	
32	VCC7	Supply voltage for the digital IF circuits.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 6-7, 9-17, 20-27, 30-32.	
Die Flag	GND	Ground connection for all circuits other than those grounded through dedicated pins. The die flag must be connected to the ground plane with very low inductance for best performance.	

Theory of Operation

The RF2968 is the first in a family of 2.4GHz transceivers developed specifically for *Bluetooth* applications. It operates as a Power Class 2 (+4dBm) or Class 3 (0dBm) *Bluetooth* device and is fully compliant to Version 1.0b of the *Bluetooth* Radio Specification. For Power Class 1 (+20dBm) applications, the RF2968 may be used with a power amplifier such as the RF2172. Processed in 0.35um silicon Bi-CMOS and packaged in a 5mm-square, industry-standard 32-pin leadless plastic package, the RF2968 provides high performance at a very low cost. With integrated IF filtering, the RF2968 requires minimal external components and eliminates the need for costly components such as IF SAW filters and baluns. The high impedance 'off' states of the receiver input and transmitter output also eliminate the need for an external transmit/receive (T/R) switch. A complete *Bluetooth* solution may be implemented with the RF2968 in conjunction with an antenna, RF bandpass filter, and baseband controller. In addition to the RF signal processing, the RF2968 also performs the baseband functions of data demodulation, DC compensation, and data and clock recovery while access code correlation takes place in the baseband device.

The RF2968 transmitter output is internally matched to 50Ω, and requires an AC-coupling capacitor. The receiver's low noise amplifier (LNA) input (**RXIN** pin) is internally matched to present a 50Ω impedance to the front end filter. A single front end filter may be shared by the transmitter and receiver by simply connecting the **TXOUT** coupling capacitor to **RXIN**. Alternatively, the transmit path may be externally amplified to +20dBm, which, in conjunction with the RF2968's transmit gain control and received signal strength indicator (RSSI), allows *Bluetooth*-compliant operation for Power Class 1. The RSSI data is accessed via the serial port and provides a 1dB resolution over the RX input power range of -20to-80dBm. Transmit gain control is adjustable in 4dB steps and is also set via the serial port.

Baseband data is sent to the transmitter via the **BDATA1** pin, which is a bidirectional pin, acting as an input in transmit mode and an output in receive mode. The RF2968 performs the Gaussian filtering of the baseband data, FSK-modulates the IF current controlled oscillator (ICO), and upconverts the IF to the RF channel frequency.

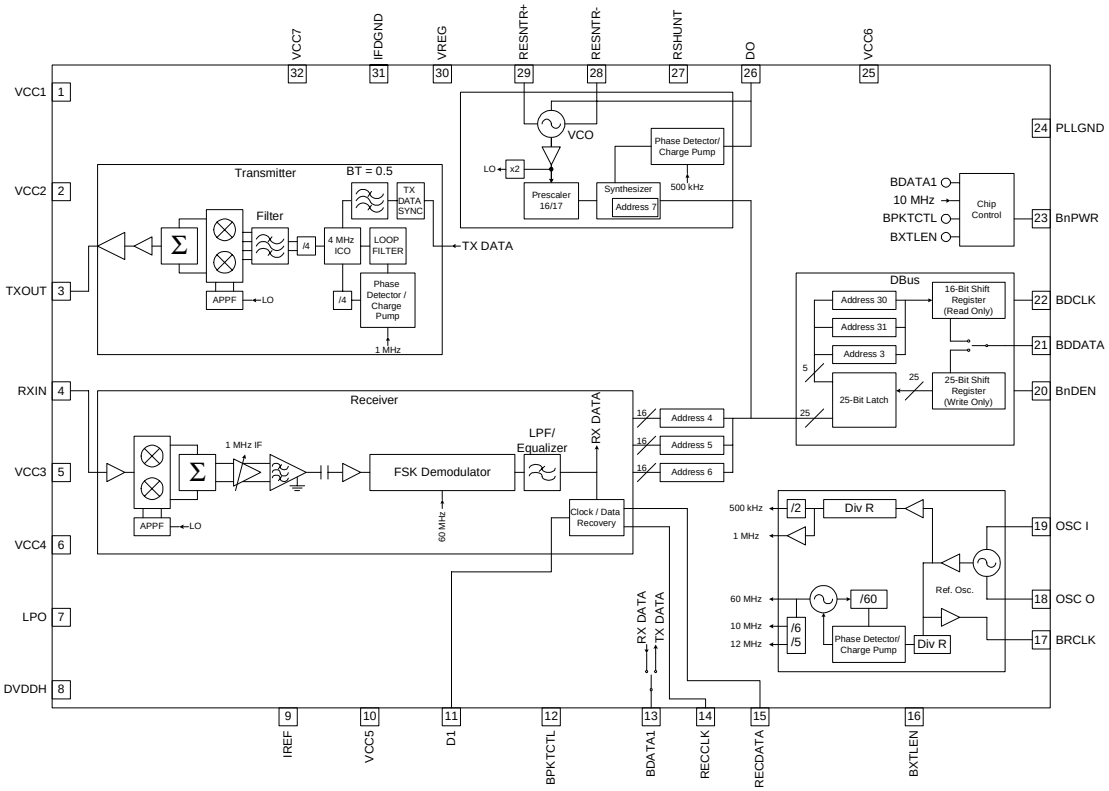
The on-chip voltage controlled oscillator (VCO) is frequency synthesized to one half of the required local oscillator (LO) frequency and then doubled to produce the correct LO frequency. Two external tank inductors between **RESNTR+** and **RESNTR-** set the tuning range of the VCO. Voltage is supplied to the VCO from an on-chip regulator that is connected to the midpoint of the two tank inductors through a filtering network. Due to the fast frequency hopping requirements of *Bluetooth*, the loop filter components (connected to pins **D0** and **RSHUNT**) are especially critical as they largely determine the hopping and settling time of the VCO. Use of the component values as given in the Application Schematic is strongly recommended.

The RF2968 may use either a 10MHz, 11MHz, 12MHz, 13MHz, or 20MHz reference clock frequency and can also support a reference clock at double these frequencies to provide a migration path toward smaller end-product designs. This clock may be supplied by an external reference applied directly to **OSC I** through a DC-blocking capacitor. If an external reference is not available, then a crystal and two capacitors may be used to complete the reference oscillator circuitry contained on-chip. For either an externally or internally generated referenced frequency, a resistor between **OSC I** and **OSC O** is required for proper biasing. The frequency tolerance of the reference clock must be 20ppm or better to assure that the maximum allowed system frequency error remains within the demodulation bandwidth of the RF2968. A selectable 3.2kHz or 32kHz low power mode clock is available at the **LPO** pin to supply the baseband device with a low frequency clock in sleep mode. Where minimal sleep mode power consumption is a concern and reference clock frequency selection is flexible, a 12MHz reference clock should be chosen.

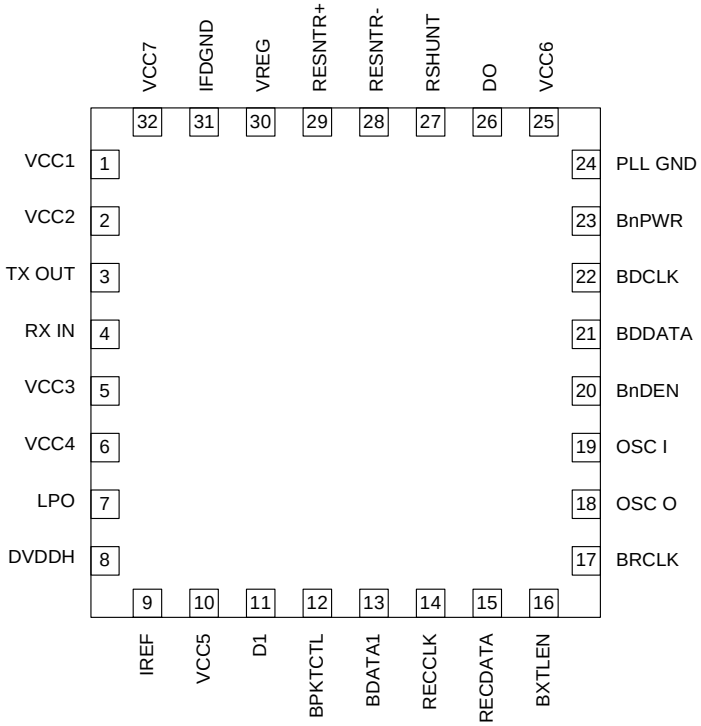
The receiver uses a low-IF architecture to minimize external component count. The RF signal is downconverted to 1MHz, allowing IF filtering to be incorporated on chip. Demodulated data is output at the **BDATA1** pin. Further data processing is performed by the data and clock recovery circuitry, which utilizes a baseband PLL. Pin **D1** is the loop filter connection for the baseband PLL. The synchronized data and clock are output at pins **RECDATA** and **RECCLK**. If the baseband device used with the RF2968 performs the clock recovery, then the **D1** loop filter components may be omitted.

The interface between the RF2968 and baseband device is described in the 'Application Information' section of the full-length datasheet available from the RFMD web site (www.rfmd.com).

Detailed Functional Block Diagram

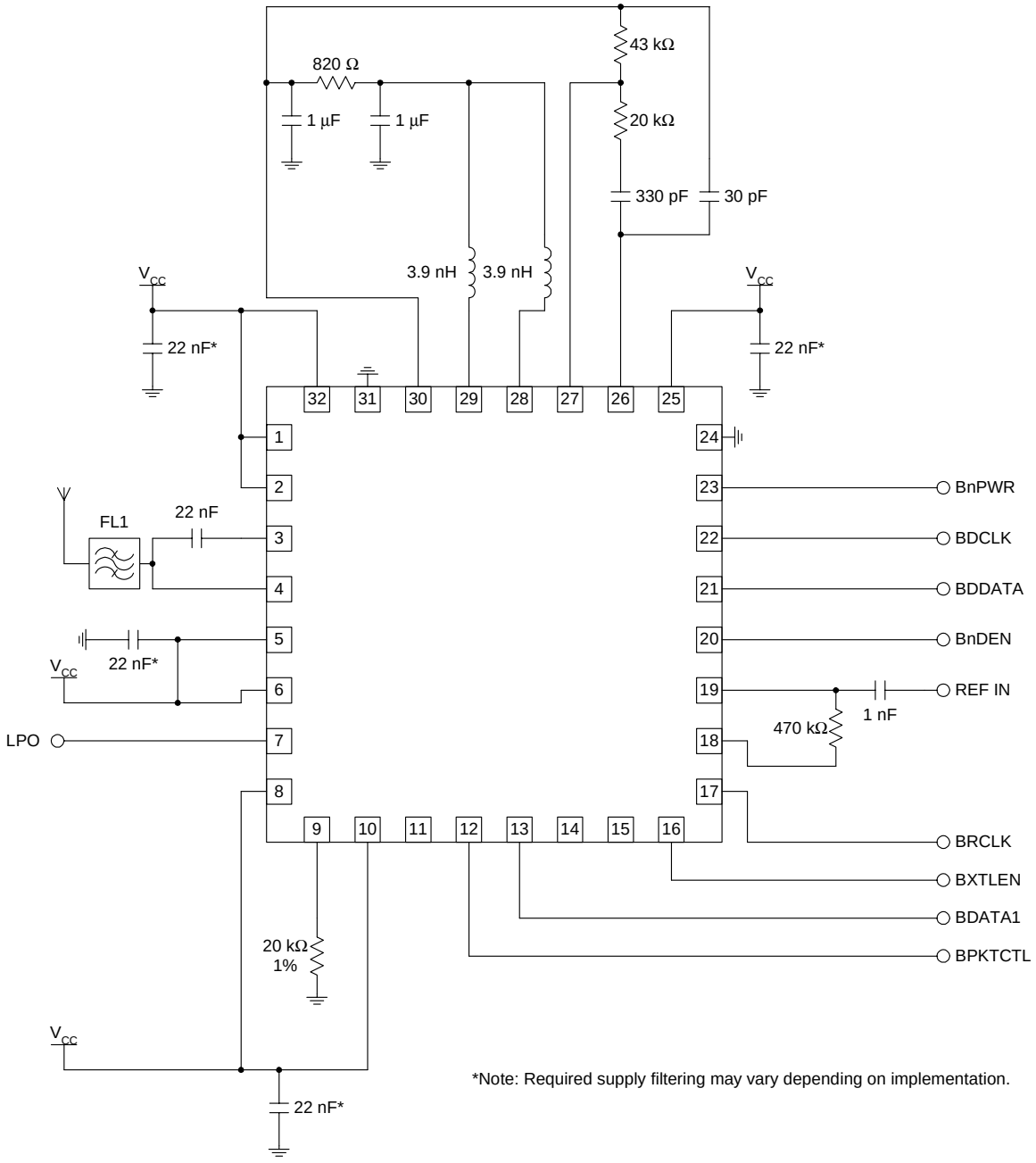


Pin Out



Application Schematic for Typical GSM Handset

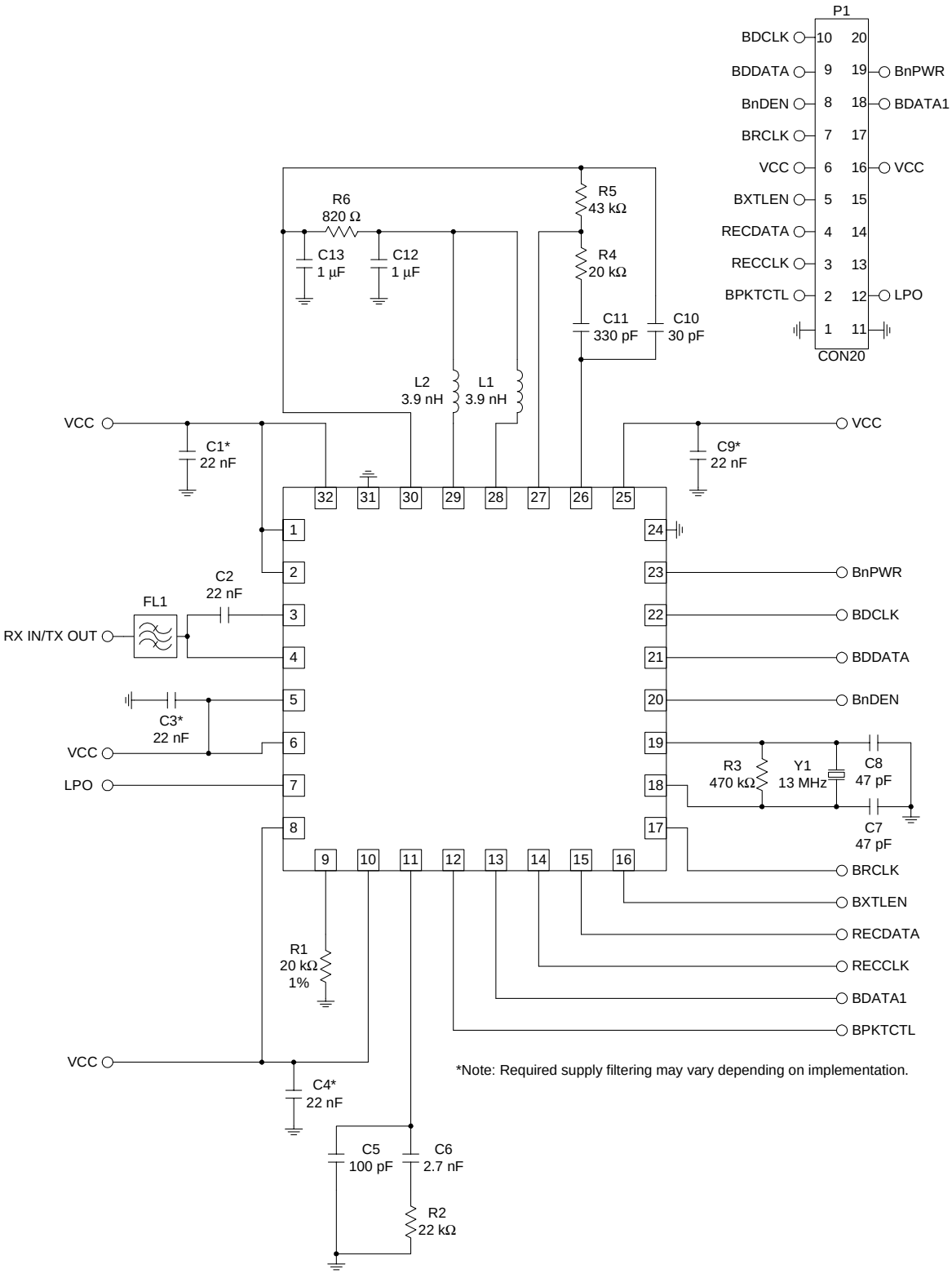
(Assumes Clock Recovery Performed by Baseband)



*Note: Required supply filtering may vary depending on implementation.

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



*Note: Required supply filtering may vary depending on implementation.

11 TRANSCEIVERS

Application Information

Baseband Interface

The RF2968 RF transceiver serves as the physical layer (PHY) in a *Bluetooth* system and supports the BlueRF interface between PHY and baseband devices. The RF2968 contains the data demodulation, DC compensation, and data and clock extraction circuitry while the access code correlator function takes place in the baseband.

There are two interfaces between the RF2968 and the baseband. The serial interface provides the path for control data exchange, and the bidirectional interface provides the path for modem, timing, and chip power control signals. Figure 1 shows bidirectional signals with arrowheads on both ends of the line.

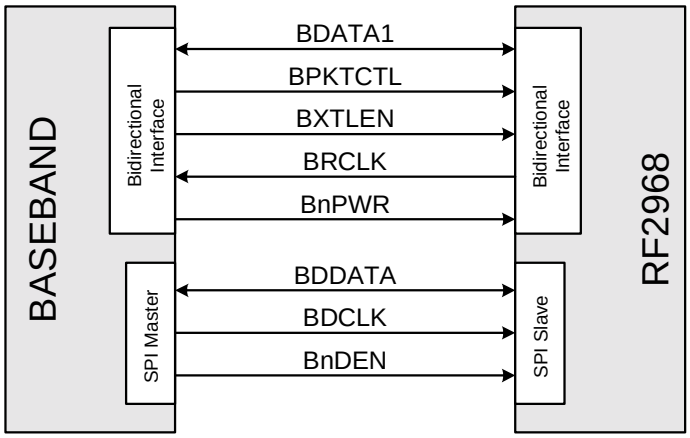


Figure1. Baseband/RF2968 Interface

Serial Interface

Control data is exchanged between the RF2968 and the baseband by means of the DBus serial interface protocol. **BDCLK**, **BDDATA**, and **BnDEN** are the signals comprising the serial interface. The baseband is the master device, initiating all accesses to the RF2968 registers. The data registers of the RF2968 are programmed or recalled according to the specified command format and address assignments. Data packets are transmitted MSB first.

Serial Data Packet Format

Field	Number of Bits	Comments
Device Address	3 [A7:A5]	"101" for PHY
Read/Write	1 [R/W]	"1"=Read, "0"=Write
Register Address	5 [A4:A0]	Maximum of 32 registers
Data	16 [D15:D0]	The RF2968 is programmed in Write mode and returns its register contents in Read mode.

During a write, the baseband drives out each bit of the packet on the falling edge of **BDCLK**. The RF2968's data register is updated with the shift register contents on the first falling edge of **BDCLK** after **BnDEN** is driven high. See Figure 2.

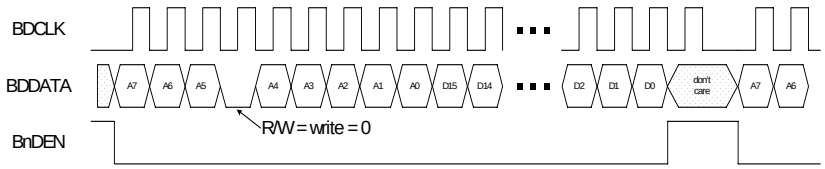


Figure 2. DBus Write Programming Diagram

In a read operation, the baseband sends the device address, READ bit (R/W = 1), and register address to the RF2968 followed by a “turn-around” bit which lasts half a clock cycle. This turn-around allows the RF2968 to drive its requested data, via **BDDATA**, on the rising edges of **BDCLK**. Following the transfer of the last data bit (D[0]), the baseband drives **BnDEN** high and resumes control of **BDDATA** on the falling edge of the first **BDCLK** pulse after **BnDEN** is driven high. See Figure 3.

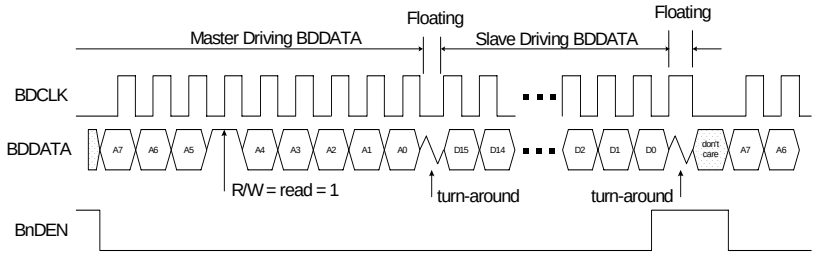


Figure 3. DBus Read Programming Diagram

Register Definition

The register address field allows up to 32 registers for various functions. The RF2968 implements only register addresses 3-7 and 30-31.

Register 3 - IF Register 1 (Read-Only)

Bit Number	Bit Name	Comments
7 - 15	N/A	Not Assigned
0 -6	RSSI[6:0]	The RSSI value indicates the average power measured during the first 10µs after a packet has been detected. The baseband reads this register to obtain the current received signal strength indicator measurement. The RSSI value may range from 0dBm to -127dBm in 1dB increments. (All 0’s indicates 0dBm; all 1’s indicates -127dBm.) The RSSI circuitry is designed to operate from -20dBm to -80dBm with an accuracy of 4dB at -60dBm. Example: RSSI[6:0]=[110101] indicates -53dBm.

Register 4 - IF Register 2 (Write-Only)

Bit Number	Bit Name	Comments
12-15	N/A	Not Assigned
11	ChopENB	Enables circuitry that significantly reduces the levels of RF PLL comparison frequency spurious responses. 1: Spur cancellation disabled. 0: Normal mode. Spur cancellation enabled.
10	Div2ENB	Enables an additional divide-by-two operation in the reference divider circuitry to accommodate the use of a 20MHz-40MHz crystal or clock. This allows a migration path to higher reference frequencies. 1: Normal mode. 10, 11, 12, 13, or 20MHz reference clock. 0: Expanded mode. Reference clock is double that allowed in normal mode.
8-9	LPO[1:0]	Determines the function of the low power mode clock (output at pin 7) when the device is in Sleep mode according to the table below. In non-Sleep modes, the output is disabled.
5-7	Gain[2:0]	Sets the gain of the transmitter path. The gain is normally programmed immediately after the register write to enter the WAIT DATA SYNC state in Power Class 1 applications. Gain is adjustable from 0dB to -28dB in 4dB steps. [All 0's indicates high gain (0dB attenuation); all 1's indicates low gain (28dB attenuation).] Example: Gain[2:0]=[011] indicates 12dB attenuation.
4	ENSlowAGCB	1: Slow AGC disabled. 0: Normal mode. Slow AGC enabled.
3	N/A	Not Assigned
2	TPL_AC	Selects a path in the RX data DC estimation circuit. 1: Selects the DC estimation path that is AC coupled and which is normally used for the payload part of packet. 0: Selects the fast DC estimation RX data path normally used for the access code of packet.
0-1	TDet[1:0]	Sets the receiver gain according to the table below.

LPO [1:0]:

LPO[1:0]	Output at LPO (Pin 7)
0 X	32kHz clock
1 0	3.2kHz clock
1 1	Clock disabled

TDet [1:0]:

TDet[1:0]	VGA Gain (dB)	Filter Gain (dB)	Total Gain (dB)	Step Size (dB)
11	-11	1.5	-9.5	
10	4.5	1.5	6.0	15.5
01	4.5	17	21.5	15.5
00	20	17	37.0	15.5

Register 5 - IF Register 3 (Write-Only)

Bit Number	Bit Name	Comments
15	BypassSM	Selects or bypasses the state machine. 1: Bypass mode. Internal power-up signals can be directly controlled by programming of the respective bits in this register [0:3, 6:7]. 0: Normal mode. All internally controlled power-up signals are derived from the state machine.
14	BBC	Selects baseband control or internal timer control for determining the time at which to perform DC estimation on the trailer bits. 1: Baseband control. The baseband drives BPKTCTL high at the end of the sync word. 0: Internal timer control.
13	N/A	Not assigned.
12	Test	IF test mode enable. Used only in IC verification; not for use in end product. 1: IF test mode 0: Normal mode
11	CalRxVGA	Calibration which compensates for the gain of the LNA, mixer, and VGA. See “Special Modes: Calibration”.
10	Cal_Tx_PLL	Calibrates the K_0 (gain of the current controlled oscillator) of the TX PLL and, by nature of the design, calibrates the K_0 of the RX PLL. See “Special Modes: Calibration”.
9	Cal_Gauss_Cell	Calibration which compensates for the offset and the amplitude of the Gaussian TX data that modulates the TX PLL ICO. See “Special Modes: Calibration”.
8	Loopback	1: Loopback mode. The TX IF output is looped back to the RX IF input. 0: Normal mode
7	PU_XTAL	Powers up the crystal oscillator circuitry. See “BypassSM” bit. 1: Power on 0: Power off
6	PU_MULT	Powers up the frequency multiplier for the FM demodulator clock. See “Bypass SM” bit. 1: Power on 0: Power off
5	CalRxFil	Calibrates the channel filter, demodulator low pass filter, and AC coupling filter in the DC estimation circuit in the receiver, as well as the Gaussian filter and GFSK harmonic filter in the transmitter. See “Special Modes: Calibration”.
4	CalRXPLL_Int	Calibration which compensates for the offset of the RX data path in the RX PLL interface circuit. See “Special Modes: Calibration”.
3	PU_PA	Powers up the transmit output amplifier. See “BypassSM” bit. 1: Power on 0: Power off
2	PU_RX	Powers up all receiver and synthesizer circuits. See “BypassSM” bit. 1: Power on 0: Power off
1	PLL_BW	Selects the loop bandwidth of the RF PLL by controlling the state of the RSHUNT pin. Under state machine control, this switch is executed according to the setting of the PLLDel[1:0] bits. 1: Narrow bandwidth. RSHUNT is short-circuited to ground. 0: Wide bandwidth. RSHUNT is a high impedance.
0	PU_TX	Powers up all transmitter and synthesizer circuits except for the output amplifier. See “BypassSM” bit. 1: Power on 0: Power off

Register 6 - IF Register 4 (Write-Only)

Bit Number	Bit Name	Comments
0-15	N/A	Not Assigned

Register 7 - PLL Control (Write-Only)

Bit Number	Bit Name	Comments
15	Set_Tx_PLL_LF_Ext	Configures the LPO pin as a test pin when bits LPO[1:0] are set high. 1: Test mode. LPO is connected to the IF PLL loop filter of the transmitter. (See “Special Modes: Transmitter Test Mode”.) 0: Normal mode. LPO is not connected to the IF PLL loop filter of the transmitter.
13 - 14	PLLDel [1:0]	Determines the time in which the PLL remains in high bandwidth mode before switching to low bandwidth mode. In high bandwidth mode, the PLL loop bandwidth is optimized for fast frequency locking. In low bandwidth mode, the loop bandwidth is optimized for low phase noise. See below. See also pin descriptions of D0 and RSHUNT, and bit PLL_BW (Register 5, Bit 1).
12	RSSI_Test	Configures the RSSI circuitry to operate continuously for test purposes. 1: Test mode. Continuous operation. 0: Normal mode. Packet-based operation.
9 - 11	DivR [2:0]	Selects the external crystal frequency. See below.
8	TX_EN	Powers up the TX voltage and current bias circuits and the TX PLL’s ICO voltage threshold set circuit.
7	RX_EN	Powers up the RX voltage and current bias circuits.
0 - 6	PLL [6:0]	Sets the RF PLL frequency. See below.

PLLDel [1:0]:

PLLDel [1:0]	Delay (us)
00	0
01	50
10	100
11	150

DivR [2:0]:

DivR [2:0]	Crystal Freq (MHz)
011	12
100	10
101	11
110	13
111	20

PLL[6:0]:

These bits determine the local oscillator (LO) frequency (i.e., the frequency at the doubler output) for both RX and TX modes. The LO frequency is set 1MHz above the channel center frequency. The PLL [6:0] data bits represent the frequency offset (F_{OFFSET}) in MHz from a base frequency of 2400MHz. For the normal *Bluetooth* frequency range of 2402MHz to 2480MHz, F_{OFFSET} will range from 3 to 81; for the optional extended *Bluetooth* range (up to 2497MHz), F_{OFFSET} will range from 3 to 98 (high-side injection assumed in both cases).

Example:
Assume a channel frequency of 2448MHz.
The LO frequency is then: 2448+1=2449MHz,
and F_{OFFSET} is: 2449-2400=49.
PLL [6:0] is then:0110001

Register 30 - Manufacturer's ID Code LSB's (Read-Only)

Bit Number	Bit Name	Comments
0 - 15	ID_Code [15:0]	Lower 16 bits of manufacturer's code. The fixed "1" LSB of the manufacturer code is read at bit 0.

Register 31 - Manufacturer's ID Code MSB's (Read-Only)

Bit Number	Bit Name	Comments
0 - 15	ID_Code [31:16]	Upper 16 bits of manufacturer's code. The MSB of the version number is read at bit 15. The RF2968 code is hex10B9825D.

Bidirectional Interface

Data Exchange and Timing

All bidirectional timing may be derived from **BRCLK**, which is generated by the RF2968. The RF2968 uses the falling edges of **BRCLK**, and the baseband uses the rising edges. Figure 4 shows the general timing for the case of data being transferred from the RF2968 to the baseband.

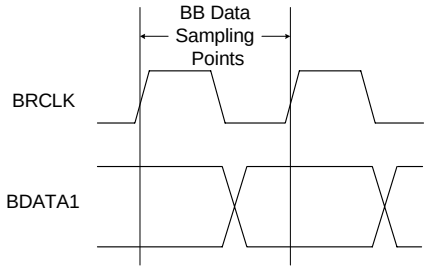


Figure 4. General Bidirectional Timing (RF2968 writing to baseband)

State Machine Control

The chip control circuitry of the RF2968 places the device into the required transmit, receive or power saving mode by controlling the power down and reset states of all other circuits in the device. The chip control inputs come from the baseband device (**BnPWR**, **BXTLEN**, **BPKTCTL**, **BDATA1**) via the bidirectional interface and from the registers at the output of the DBus block (**RXEN**, **TXEN**). State machines in the baseband and the RF2968 maintain the state which controls the direction of the bidirectional lines. The baseband controls the state machine in the RF2968 and ensures that data contentions do not occur during reset and normal operation. The control of individual sections of the RF2968 in each state is as follows.

State	Description
OFF	All circuits are powered down and reset; configuration data is lost. (CLRB=0)
PWRON WAIT XTL	Reset is released (CLRB=1) and the oscillator is turned on (PDXTAL=1).
HOLD XTL	This mode is entered when the oscillator has settled. Configuration data can be read through the DBus interface.
IDLE	This is a standby mode. Data can be read into the control registers (through the DBus) and the oscillator remains on. All other circuits are powered down.
SLEEP	The device normally enters this mode from IDLE, in which case every circuit is powered down but not reset, so that configuration data is retained. The device may also enter this mode from any other except PWRON WAIT XTL or HOLD XTL, but the TXEN and RXEN functions are not overridden, so that TX and RX circuits may remain on.
WAIT XTL	The oscillator is turned on (PDXTAL=1) and allowed to settle before returning to IDLE mode.
WAIT DATA SYNC	This is the start of the transmit sequence. This mode is entered by the baseband writing to the control registers (through the DBus). When this happens, TXEN goes high, turning on the synthesizer and initializing a fixed delay, after which all the transmit circuits (except for the PA) are turned on (PD_TX=1). The baseband waits 175µs before it starts sending transmit data to the RF2968 (to allow the synthesizer to settle). The device cannot be in both transmit and receive modes at the same time, so RXEN must be low to enter this mode.
DATA SYNC	A transition on BDATA1 (0 to 1) starts the synchronization of data between the RF2968 and the baseband device.
ENABLE PA	The PA is powered up (PDPA=1) and ready to begin transmitting.
TX DATA	Data is transmitted in this mode. (The synthesizer has settled and the data path synchronized.)
DISABLE PA	The PA is powered down (PDPA=0). 1µs later, the synthesizer and the rest of the transmit circuits are powered down (PD_TX=0). This delay prevents any “unwanted transmission” during power down. The device then returns to IDLE mode when the baseband writes to the control registers and drives TXEN low.
RX PLL WAIT	This is the start of the receive sequence and is entered from IDLE mode when a control register write from the baseband forces RXEN high. This turns on the synthesizer and starts a timer which powers up the receive path circuits after a fixed delay (PD_RX=1). The baseband device expects to receive data 175µs after the control register write.
RX DATA	Received data is sent to the baseband device via BDATA1 (unsynchronized) and RECDATA (synchronized with RECCLK). Within this state, there are two DC estimation modes. In the “access code” mode, the RF2968 uses a fast DC estimation to adjust for large frequency offsets. An internal timer (or alternatively BPKTCTL) signals the end of the sync word, placing the DC estimation circuitry in the “payload” mode, in which compensation is made for small frequency offsets. A control register write from the baseband drives RXEN low and returns the device to IDLE mode. This turns off the receive path (PD_RX=0) and the synthesizer.

State Machine

The RF2968 state machine is clocked with a 1MHz signal which is derived from the reference oscillator. (The mark - space ratio of this 1MHz clock and its precise frequency are not important.) The inputs and outputs for all the states are summarized in the table below.

Table 1. State Machine Inputs and Outputs

Previous State	Present State[a]	Inputs						Outputs				
		BnPWR	BXTLEN	BDATA1	BPKTCTL	RXEN	TXEN	PDXTAL	CLRB	PDTX	PDPA	PDRX
X	OFF	0	X	X	X	X	X	0	0	0	0	0
OFF	PWRON WAIT	1	0	1	X	X	X	1	1	0	0	0
PWRON WAIT	HOLD XTL	1	1	1	X	0	0	1	1	0	0	0
HOLD XTL	IDLE	1	1	X	X	0	0	1	1	0	0	0
IDLE	SLEEP	1	0	X	X	0	0	0	1	0	0	0
SLEEP	WAIT XTL	1	1	X	X	0	0	1	1	0	0	0
WAIT XTL	IDLE	1	1	X	X	0	0	1	1	0	0	0
IDLE	WAIT DATA SYNC	1	1	X	0[e]	0	1	1	1	1[b]	0	0
WAIT DATA	DATA SYNC	1	1	X	0[e]	X	1	1	1	1	0	0
DATA SYNC	ENABLE PA	1	1	X	1	X	1	1	1	1	1	0
ENABLE PA	TX DATA	1	1	X	1	X	1	1	1	1	1	0
TX DATA	DISABLE PA	1	1	X	0	X	1	1	1	0[c]	0	0
DISABLE PA	IDLE	1	1	X	X	X[f]	0	1	1	0	0	0
IDLE	RX PLL WAIT	1	1	X	X	1	0	1	1	0	0	1[d]
RX PLL WAIT	RX DATA	1	1	X	X	1	0	1	1	0	0	1
RX DATA	IDLE	1	1	X	X	0	X	1	1	0	0	0

Notes:

a. When the inputs try to force the controller into an undefined or illegal state, the state machine will remain in its present state (e.g., if the present state is IDLE and the inputs try to force the device to TX DATA, the chip will stay in IDLE mode).
b. PD_TX goes high after a fixed delay following TXEN going high.
c. 1µs delay from the PD_PA going low to PD_TX going low.
d. PD_RX goes high after a fixed delay following RXEN going high.
e. BPKTCTL must be low to distinguish DATA SYNC from ENABLE PA.
f. If RXEN=1 when entering IDLE from DISABLE PA, then IDLE is held for 1µs, after which the state transitions to RX PLL WAIT.

Special Modes of Operation

Calibration

When the RF2968 is *Reset* (CLRB=0), all calibration values are cleared. Therefore, after the RF2968 is powered up from the OFF state, it must be instructed to perform its self-calibration. Circuits requiring calibration include the RX variable gain amplifier (VGA), TX and RX PLL's, RX channel filter, RX data paths, and TX Gaussian filter.

Calibration instructions are sent from the baseband to the RF2968 via the serial port (addressing Registers 5 and 7) and must be performed in the order shown in the table below. After a calibration instruction is sent, the baseband must delay for the length of time indicated before sending the next calibration instruction; this allows time for the RF2968 circuits to settle and execute the instruction. At initialization, BypassSM, PU_XTAL, PU_MULT, and TX_EN are set high and remain so for the duration of the calibration. Register 7 is only addressed during initialization to set TX_EN and configure the reference frequency and RF PLL frequency.

Calibration Steps	Register	Bit Settings for Calibration Sequence[a]																Required Time (usec)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Initialization of PLL	7	0	0	0	0	x[b]	x[b]	x[b]	1	0	x[c]	x[c]	x[c]	x[c]	x[c]	x[c]	x[c]	0[d]
Initialization of Chip Control	5	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	2500
Calibrate K_O of TX and RX IF PLL's	5	1	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1024
Calibrate Gaussian TX and RX VGA	5	1	0	0	0	1	0	1	0	1	1	0	0	0	1	0	1	285
Calibrate IF Filters	5	1	0	0	0	0	0	0	0	1	1	1	0	0	1	0	1	608
Calibrate RX Offsets	5	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	64
Return Chip Control to State Machine	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
										Total Calibration Time:								4481

Notes:

a) Shaded cells indicate no change from previous state.

b) Set according to reference frequency.

c) Set RF PLL frequency to a valid frequency (LO=2403 to 2481MHz).

d) Register 5 may be programmed immediately after Register 7.

Transmitter Test Mode:

During normal TX mode, the transmitter's IF PLL is opened for modulation of the current controlled oscillator (ICO) for a short period of time (0.4 to 3ms). For development purposes, open-loop modulation may be performed for an indefinite period of time by externally supplying the required ICO control voltage. This allows the ICO to maintain a locked condition.

Transmitter Test Mode utilizes the LPO pin, which is switched to the output of the internal loop filter of the transmitter's IF ICO when Set_Tx_PLL_LF_Ext (Register 7, Bit 15) is set high and the 3.2kHz/32kHz low power oscillator is not in use. This pin may be used either to monitor the control voltage during a packet transmission or to externally supply the control voltage for an extended or continuous transmission. When monitoring the ICO control voltage, the voltage on the LPO pin will drift from its initial voltage as the transmission time increases, but should remain in the range of 0.7V to 0.9V. When supplying the ICO control voltage, the voltage to be applied to the LPO pin should be equal to the initial voltage measured when monitoring.