RICOH

Version 1.4
May. 13,1998

RL5C476A PCI-CARDBUS BRIDGE DATA SHEET

1 OVERVIEW

The RL5C476A is a PC card controller offering a single chip solution as a bridge between PCI bus and CardBus. The RL5C476A includes two PC Card 95 compliant sockets interface and a bridge function to the PCI bus of 33Mhz. The RL5C476A can support the 32-bit CardBus(Card-32) and the 16-bit PC card(Card-16) without external buffers.

Concerning the card control interface, the RL5C476A's register is compatible with the Intel 82365SL and Ricoh's RF5C396/366 in order to maintain backward compatibility with the existing 16-bit PC Card compliant with PCMCIA2.1/JEIDA4.2. All PC card interface signals are individually buffered to allow direct connection to CardBus and Hot insertion/removal without external buffers. The RL5C476A also allows direct connection to PCI bus.

The PCI interface and PC card socket interface have their own power supply terminals that can be powered at either 3.3V or 5V for compatibility with 3.3V and 5V signaling environments. The core logic is powered at 3.3V.

The RL5C476A allows the system to be equipped with the high performance multimedia PC cards like the Video capture card.

- PC97 compliant
  - PC97 Design Guide compliant (Subsystem ID, Subsystem Vender ID)
  - ACPI 1.0 and PCI Bus Power Management 1.0 compliant
- Low Power consumption
  - Hardware Suspend (Non shared Hardware Suspend Input)
  - CLKRUN#,CCLKRUN# support
- High-performance
- Single Chip PCI-CardBus Bridge
  - 2 PCMCIA PC-Card 95 sockets support
  - CardBus(Card-32) Card and 16-bit(PCMCIA2.1/JEIDA4.2) Card work at the same time
  - Bridge function between PCI bus and CardBus
- PCI Bus Interface
- Compliant with PCI Local Bus Specification 2.1
  - the maximum frequency 33MHz
  - PCI Master/Target protocol support
  - Separated PCI configuration each socket
  - Direct connection to PCI bus

- CardBus PC card Bridge
  - Compliant with PCMCIA PC Card 95/CardBus Standard Specification
  - Compliant with Yenta register set Rev2.2
  - the maximum frequency 33MHz
  - CardBus Master/Target protocol support
  - Transfer transactions
    - All memory read/write transaction(bi-direction)
    - I/O read/write transaction(bi-direction)
    - Configuration read/write transaction(PCI → Card)
  - 2 programmable memory windows
  - 2 programmable I/O windows

- PC Card-16 Bridge
  - Compliant with PCMCIA PC Card 95 CardBus(PC Card-16) Standard Specification
  - 5 programmable memory windows
  - 2 programmable I/O windows
  - Compliant with i82365SL compatible register set / ExCA TM

- System Interrupt
  - INTA#,INTB# support for PCI system interrupt (Non shared INT# pin)
  - IRQn support for ISA system interrupt (Non shared IRQn pins)
  - Serialized IRQ support

- 3.3V/5V Mixed Voltage Operation at 33Mhz

- GPIO support

- Posting Write and Prefetching Read support

- Plug and Play support

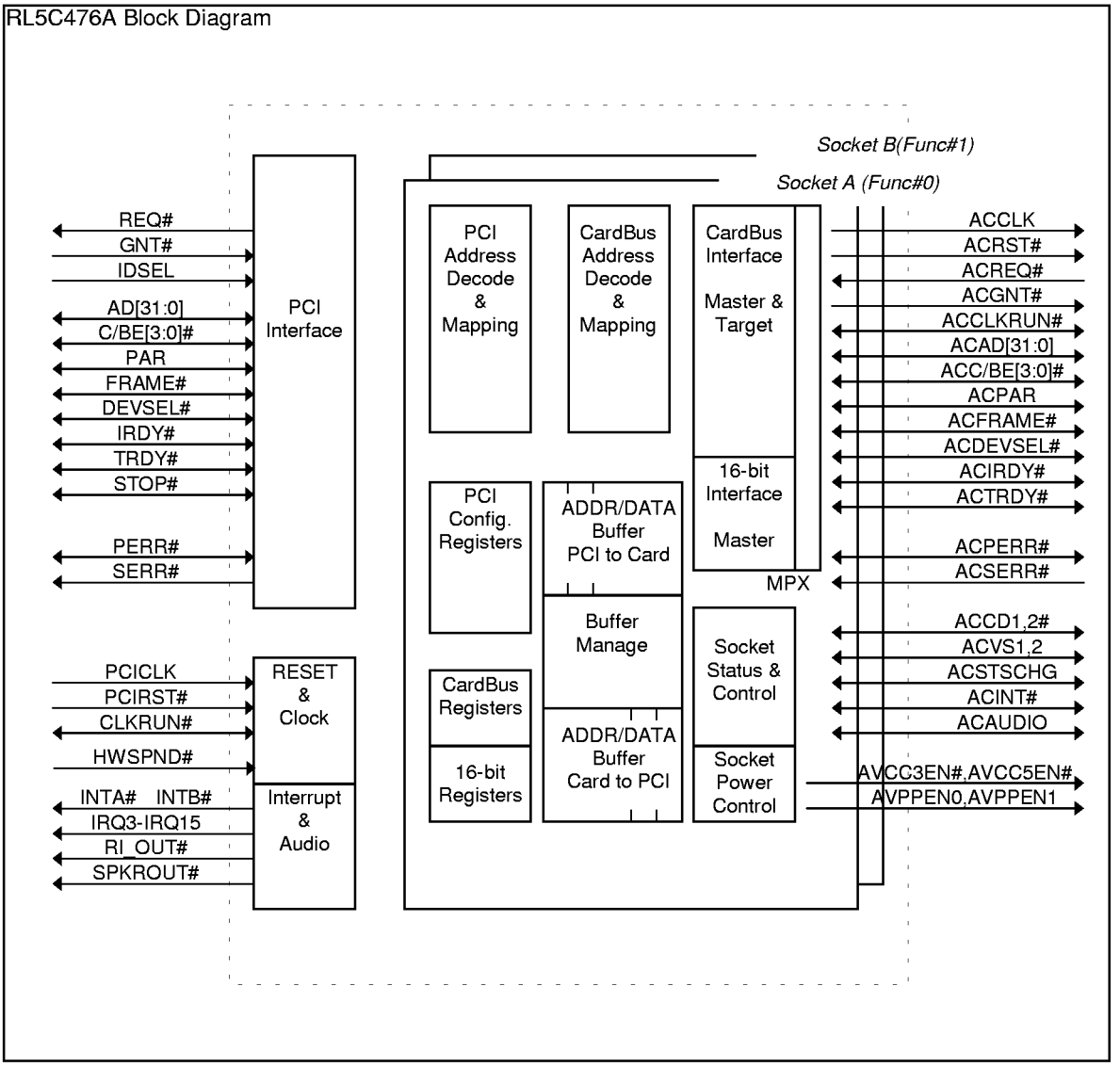
- 16-bit Legacy mode (3E0/3E2 I/O port) support

- Zoomed Video Port support
  - Bypass type

- PCIway Legacy DMA support

- Package
  - 208pin LQFP 0.5P t=1.7mm

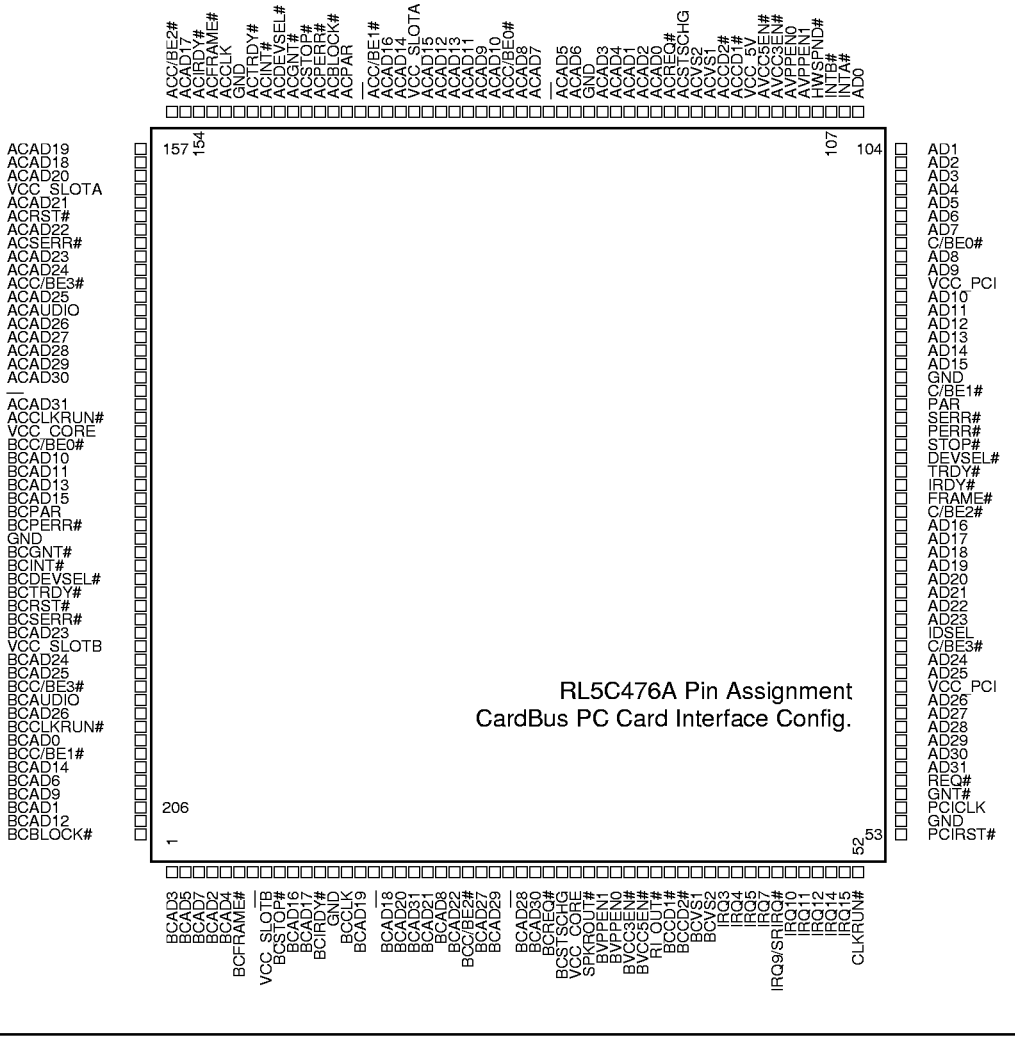
2 BLOCK DIAGRAM



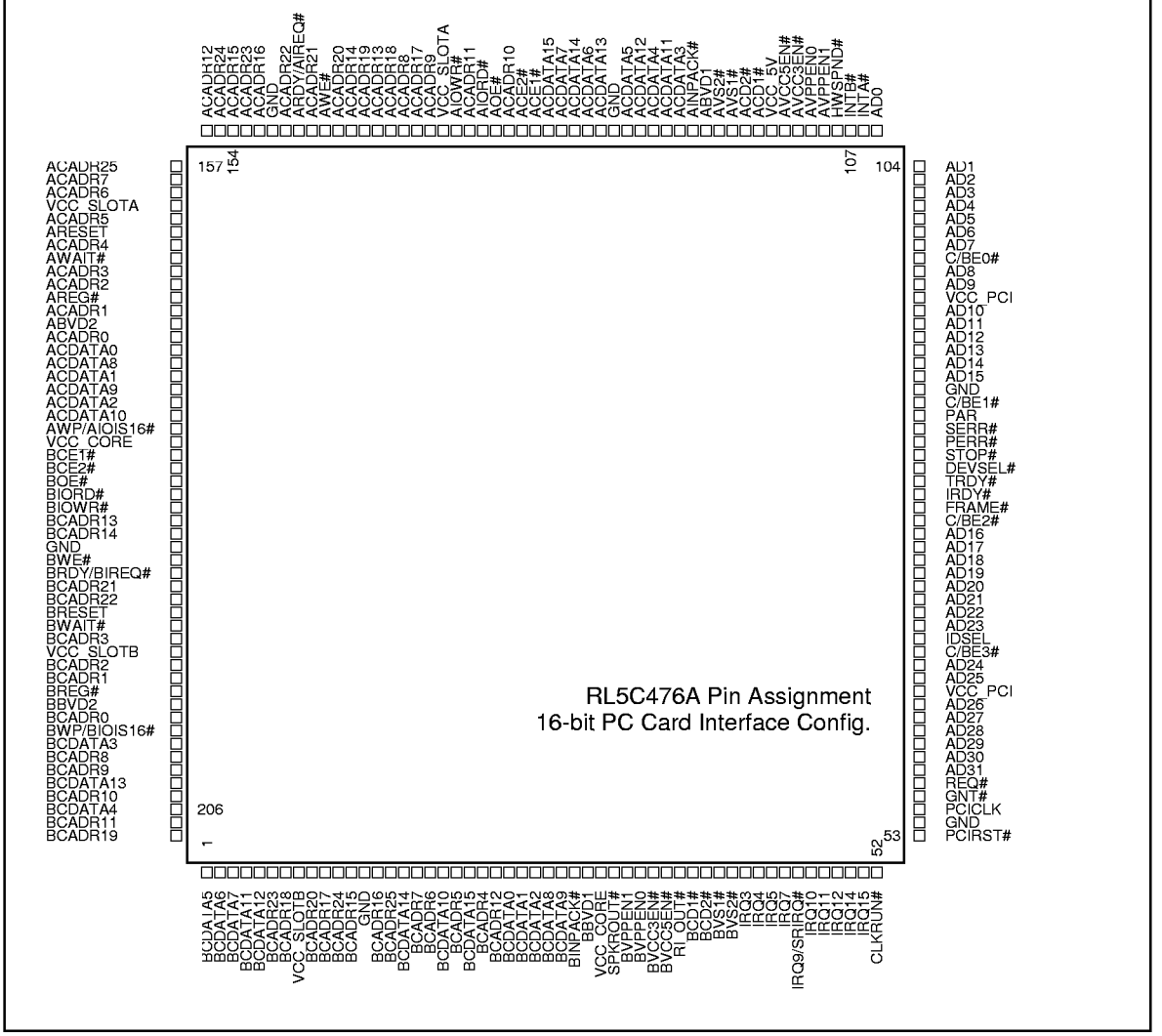
3 PIN DESCRIPTION

3.1 Pin Assignments

RL5C476A PIN ASSIGNMENT(TOP VIEW)



RL5C476A PIN ASSIGNMENT(TOP VIEW)



3.2 Pin Characteristics

RL5C476A pin characteristics

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
	Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
1	BCDATA5	I/O	BCAD3	I/O	I/O(PD)	B	PD		8mA	1
2	BCDATA6	I/O	BCAD5	I/O	I/O(PD)	B	PD		8mA	1
3	BCDATA7	I/O	BCAD7	I/O	I/O(PD)	B	PD		8mA	1
4	BCDATA11	I/O	BCAD2	I/O	I/O(PD)	B	PD		8mA	1
5	BCDATA12	I/O	BCAD4	I/O	I/O(PD)	B	PD		8mA	1
6	BCADR23	O	BCFRAME#	I/O	I/O	B			8mA	
7	BCADR18	O	—	—	O(TS)	B			8mA	
8	VCC_SLOTB	DC	VCC_SLOTB	DC	PWR	B			—	
9	BCADR20	O	BCSTOP#	I/O	I/O(PU)	B		PU	8mA	2
10	BCADR17	O	BCAD16	I/O	I/O	B			8mA	
11	BCADR24	O	BCAD17	I/O	I/O	B			8mA	
12	BCADR15	O	BCIRDY#	I/O	I/O(PU)	B		PU	8mA	2
13	GND	DC	GND	DC	PWR	G			—	
14	BCADR16	O	BCCLK	O	O(TS)	B			CB	
15	BCADR25	O	BCAD19	I/O	I/O	B			8mA	
16	BCDATA14	I/O	—	—	I/O(PD)	B	PD		8mA	1
17	BCADR7	O	BCAD18	I/O	I/O	B			8mA	
18	BCADR6	O	BCAD20	I/O	I/O	B			8mA	
19	BCDATA10	I/O	BCAD31	I/O	I/O(PD)	B	PD		8mA	1
20	BCADR5	O	BCAD21	I/O	I/O	B			8mA	
21	BCDATA15	I/O	BCAD8	I/O	I/O(PD)	B	PD		8mA	1
22	BCADR4	O	BCAD22	I/O	I/O	B			8mA	
23	BCADR12	O	BCC/BE2#	I/O	I/O	B			8mA	
24	BCDATA0	I/O	BCAD27	I/O	I/O(PD)	B	PD		8mA	1
25	BCDATA1	I/O	BCAD29	I/O	I/O(PD)	B	PD		8mA	1
26	BCDATA2	I/O	—	—	I/O(PD)	B	PD		8mA	1
27	BCDATA8	I/O	BCAD28	I/O	I/O(PD)	B	PD		8mA	1
28	BCDATA9	I/O	BCAD30	I/O	I/O(PD)	B	PD		8mA	1
29	BINPACK#	I	BCREQ#	I	I(PU)	B	PU	PU	—	
30	BBVD1/ BSTSCHG# BRI#	I	BCSTCHG	I	I(PU)/ I(PD)	B	PU	PD		3
31	VCC_CORE	DC	VCC_CORE	DC	PWR	C			—	
32	SPKROUT#	O	SPKROUT#	O	O	5			4mA	
33	BVPPEN1	O	BVPPEN1	O	O	5			4mA	
34	BVPPEN0	O	BVPPEN0	O	O	5			4mA	
35	BVCC3EN#	O	BVCC3EN#	O	O	5			4mA	
36	BVCC5EN#	O	BVCC5EN#	O	O	5			4mA	

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
	Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup 16	Pulldown CB	Drive	
37	RI_OUT#	O	RI_OUT#	O	O(TS)	5			4mA	
38	BCD1#	I	BCCD1#	I	I(PU)	5	PU	PU	—	
39	BCD2#	I	BCCD2#	I	I(PU)	5	PU	PU	—	
40	BVS1#	I/O	BCVS1	I/O	I/O	5			1mA	
41	BVS2#	I/O	BCVS2	I/O	I/O	5			1mA	
42	IRQ3	I/O	IRQ3	I/O	I/O	P			8mA	
43	IRQ4	I/O	IRQ4	I/O	I/O	P			8mA	
44	IRQ5	I/O	IRQ5	I/O	I/O	P			8mA	
45	IRQ7	I/O	IRQ7	I/O	I/O	P			8mA	
46	IRQ9/SRIRQ#	I/O	IRQ9/IRQS#	I/O	I/O	P			8mA	
47	IRQ10	O	IRQ10	O	O(TS)	P			8mA	
48	IRQ11	O	IRQ11	O	O(TS)	P			8mA	
49	IRQ12	O	IRQ12	O	O(TS)	P			8mA	
50	IRQ14	O	IRQ14	O	O(TS)	P			8mA	
51	IRQ15	O	IRQ15	O	O(TS)	P			8mA	
52	CLKRUN#	I/O	CLKRUN#	I/O	I/O	P			PCI21	
53	PCIRST#	I	PCIRST#	I	I	P			—	
54	GND	DC	GND	DC	PWR	G			—	
55	PCICLK	I	PCICLK	I	I	P			—	
56	GNT#	I	GNT#	I	I	P			—	
57	REQ#	O	REQ#	O	O(TS)	P			PCI21	
58	AD31	I/O	AD31	I/O	I/O	P			PCI21	
59	AD30	I/O	AD30	I/O	I/O	P			PCI21	
60	AD29	I/O	AD29	I/O	I/O	P			PCI21	
61	AD28	I/O	AD28	I/O	I/O	P			PCI21	
62	AD27	I/O	AD27	I/O	I/O	P			PCI21	
63	AD26	I/O	AD26	I/O	I/O	P			PCI21	
64	VCC_PCI	DC in	VCC_PCI	DC in	PWR	P			—	
65	AD25	I/O	AD25	I/O	I/O	P			PCI21	
66	AD24	I/O	AD24	I/O	I/O	P			PCI21	
67	C/BE3#	I/O	C/BE3#	I/O	I/O	P			PCI21	
68	IDSEL	I	IDSEL	I	I	P			—	
69	AD23	I/O	AD23	I/O	I/O	P			PCI21	
70	AD22	I/O	AD22	I/O	I/O	P			PCI21	
71	AD21	I/O	AD21	I/O	I/O	P			PCI21	
72	AD20	I/O	AD20	I/O	I/O	P			PCI21	
73	AD19	I/O	AD19	I/O	I/O	P			PCI21	
74	AD18	I/O	AD18	I/O	I/O	P			PCI21	
75	AD17	I/O	AD17	I/O	I/O	P			PCI21	
76	AD16	I/O	AD16	I/O	I/O	P			PCI21	

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
	Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
77	C/BE2#	I/O	C/BE2#	I/O	I/O	P			PCI21	
78	FRAME#	I/O	FRAME#	I/O	I/O	P			PCI21	
79	IRDY#	I/O	IRDY#	I/O	I/O	P			PCI21	
80	TRDY#	I/O	TRDY#	I/O	I/O	P			PCI21	
81	DEVSEL#	I/O	DEVSEL#	I/O	I/O	P			PCI21	
82	STOP#	I/O	STOP#	I/O	I/O	P			PCI21	
83	PERR#	I/O	PERR#	I/O	I/O	P			PCI21	
84	SERR#	O	SERR#	O	O(OD)	P			PCI21	
85	PAR	I/O	PAR	I/O	I/O	P			PCI21	
86	C/BE1#	I/O	C/BE1#	I/O	I/O	P			PCI21	
87	GND	DC	GND	DC	PWR	G			—	
88	AD15	I/O	AD15	I/O	I/O	P			PCI21	
89	AD14	I/O	AD14	I/O	I/O	P			PCI21	
90	AD13	I/O	AD13	I/O	I/O	P			PCI21	
91	AD12	I/O	AD12	I/O	I/O	P			PCI21	
92	AD11	I/O	AD11	I/O	I/O	P			PCI21	
93	AD10	I/O	AD10	I/O	I/O	P			PCI21	
94	VCC_PCI	DC	VCC_PCI	DC	PWR	P			—	
95	AD9	I/O	AD9	I/O	I/O	P			PCI21	
96	AD8	I/O	AD8	I/O	I/O	P			PCI21	
97	C/BE0#	I/O	C/BE0#	I/O	I/O	P			PCI21	
98	AD7	I/O	AD7	I/O	I/O	P			PCI21	
99	AD6	I/O	AD6	I/O	I/O	P			PCI21	
100	AD5	I/O	AD5	I/O	I/O	P			PCI21	
101	AD4	I/O	AD4	I/O	I/O	P			PCI21	
102	AD3	I/O	AD3	I/O	I/O	P			PCI21	
103	AD2	I/O	AD2	I/O	I/O	P			PCI21	
104	AD1	I/O	AD1	I/O	I/O	P			PCI21	
105	AD0	I/O	AD0	I/O	I/O	P			PCI21	
106	INTA#	O	INTA#	O	O(OD)	P			PCI21	
107	INTB#	O	INTB#	O	O(OD)	P			PCI21	
108	HWSPND#	I	HWSPND#	I	I	5			—	
109	AVPPEN1	O	AVPPEN1	O	O	5			4mA	
110	AVPPEN0	O	AVPPEN0	O	O	5			4mA	
111	AVCC3EN#	O	AVCC3EN#	O	O	5			4mA	
112	AVCC5EN#	O	AVCC5EN#	O	O	5			4mA	
113	VCC_5V	DC in	VCC_5V	DC in	PWR	5			—	
114	ACD1#	I	ACCD1#	I	I(PU)	5	PU	PU	—	
115	ACD2#	I	ACCD2#	I	I(PU)	5	PU	PU	—	

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
	Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
116	AVS1#	I/O	ACVS1	I/O	I/O	5			1mA	
117	AVS2#	I/O	ACVS2	I/O	I/O	5			1mA	
118	ABVD1/ ASTSCHG#/ ARI#	I	ACSTSCHG	I	I(PU)/ I(PD)	A	PU	PD	—	3
119	AINPACK#	I	ACREQ#	I	I(PU)	A	PU	PU	—	
120	ACDATA3	I/O	ACAD0	I/O	I/O(PD)	A	PD		8mA	1
121	ACDATA11	I/O	ACAD2	I/O	I/O(PD)	A	PD		8mA	1
122	ACDATA4	I/O	ACAD1	I/O	I/O(PD)	A	PD		8mA	1
123	ACDATA12	I/O	ACAD4	I/O	I/O(PD)	A	PD		8mA	1
124	ACDATA5	I/O	ACAD3	I/O	I/O(PD)	A	PD		8mA	1
125	GND	DC	GND	DC	PWR	G			—	
126	ACDATA13	I/O	ACAD6	I/O	I/O(PD)	A	PD		8mA	1
127	ACDATA6	I/O	ACAD5	I/O	I/O(PD)	A	PD		8mA	1
128	ACDATA14	I/O	—	—	I/O(PD)	A	PD		8mA	1
129	ACDATA7	I/O	ACAD7	I/O	I/O(PD)	A	PD		8mA	1
130	ACDATA15	I/O	ACAD8	I/O	I/O(PD)	A	PD		8mA	1
131	ACE1#	O	ACC/BE0#	I/O	I/O	A			8mA	
132	ACE2#	O	ACAD10	I/O	I/O	A			8mA	
133	ACADR10	O	ACAD9	I/O	I/O	A			8mA	
134	AOE#	O	ACAD11	I/O	I/O	A			8mA	
135	AIORD#	O	ACAD13	I/O	I/O	A			8mA	
136	ACADR11	O	ACAD12	I/O	I/O	A			8mA	
137	AIOWR#	O	ACAD15	I/O	I/O	A			8mA	
138	VCC_SLOTA	DC	VCC_SLOTA	DC	PWR	A			—	
139	ACADR9	O	ACAD14	I/O	I/O	A			8mA	
140	ACADR17	O	ACAD16	I/O	I/O	A			8mA	
141	ACADR8	O	ACC/BE1#	I/O	I/O	A			8mA	
142	ACADR18	O	—	—	O(TS)	A			8mA	
143	ACADR13	O	ACPAR	I/O	I/O	A			8mA	
144	ACADR19	O	—	I/O	I/O(PU)	A		PU	8mA	2
145	ACADR14	O	ACPERR#	I/O	I/O(PU)	A		PU	8mA	2
146	ACADR20	O	ACSTOP#	I/O	I/O(PU)	A		PU	8mA	2
147	AWE#	O	ACGNT#	O	O(TS)	A			8mA	
148	ACADR21	O	ACDEVSEL#	I/O	I/O(PU)	A		PU	8mA	2
149	ARDY/ AIREQ#	I	ACINT#	I	I(PU)	A	PU	PU	—	
150	ACADR22	O	ACTRDY#	I/O	I/O(PU)	A		PU	8mA	2
151	GND	DC	GND	DC	PWR	G			—	
152	ACADR16	O	ACCLK	O	O(TS)	A			CB	

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
	Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
153	ACADR23	O	ACFRAME#	I/O	I/O	A			8mA	
154	ACADR15	O	ACIRDY#	I/O	I/O(PU)	A		PU	8mA	2
155	ACADR24	O	ACAD17	I/O	I/O	A			8mA	
156	ACADR12	O	ACC/BE2#	I/O	I/O	A			8mA	
157	ACADR25	O	ACAD19	I/O	I/O	A			8mA	
158	ACADR7	O	ACAD18	I/O	I/O	A			8mA	
159	ACADR6	O	ACAD20	I/O	I/O	A			8mA	
160	VCC_SLOTA	DC	VCC_SLOTA	DC	PWR	A			—	
161	ACADR5	O	ACAD21	I/O	I/O	A			8mA	
162	ARESET	O	ACRST#	O	O(TS)	A			4mA	
163	ACADR4	O	ACAD22	I/O	I/O	A			8mA	
164	AWAIT#	I	ACSERR#	I	I(PU)	A	PU	PU	—	
165	ACADR3	O	ACAD23	I/O	I/O	A			8mA	
166	ACADR2	O	ACAD24	I/O	I/O	A			8mA	
167	AREG#	O	ACC/BE3#	I/O	I/O	A			8mA	
168	ACADR1	O	ACAD25	I/O	I/O	A			8mA	
169	ABVD2/ ASPKR#	I	ACAUDIO	I	I(PU)	A	PU	PU	—	
170	ACADR0	O	ACAD26	I/O	I/O	A			8mA	
171	ACDATA0	I/O	ACAD27	I/O	I/O(PD)	A	PD		8mA	1
172	ACDATA8	I/O	ACAD28	I/O	I/O(PD)	A	PD		8mA	1
173	ACDATA1	I/O	ACAD29	I/O	I/O(PD)	A	PD		8mA	1
174	ACDATA9	I/O	ACAD30	I/O	I/O(PD)	A	PD		8mA	1
175	ACDATA2	I/O	—	—	I/O(PD)	A	PD		8mA	1
176	ACDATA10	I/O	ACAD31	I/O	I/O(PD)	A	PD		8mA	1
177	AWP/ AIOIS16#	I	ACCLKRUN#	I/O	I/O(PU)	A		PU	8mA	2
178	VCC_CORE	DC	VCC_CORE	DC	PWR	C			—	
179	BCE1#	O	BCC/BE0#	I/O	I/O	B			8mA	
180	BCE2#	O	BCAD10	I/O	I/O	B			8mA	
181	BOE#	O	BCAD11	I/O	I/O	B			8mA	
182	BIORD#	O	BCAD13	I/O	I/O	B			8mA	
183	BIOWR#	O	BCAD15	I/O	I/O	B			8mA	
184	BCADR13	O	BCPAR	I/O	I/O	B			8mA	
185	BCADR14	O	BCPERR#	I/O	I/O(PU)	B		PU	8mA	2
186	GND	DC in	GND	DC in	PWR	G			—	
187	BWE#	O	BCGNT#	O	O(TS)	B			8mA	
188	BRDY/ BIREQ#	I	BCINT#	I	I(PU)	B	PU	PU	—	
189	BCADR21	O	BCDEVSEL#	I/O	I/O(PU)	B		PU	8mA	2
190	BCADR22	O	BCTRDY#	I/O	I/O(PU)	B		PU	8mA	2

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
	Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
191	BRESET	O	BCRST#	O	O(TS)	B			4mA	
192	BWAIT#	I	BCSERR#	I	I(PU)	B	PU	PU	—	
193	BCADR3	O	BCAD23	I/O	I/O	B			8mA	
194	VCC_SLOTB	DC	VCC_SLOTB	DC	PWR	B			—	
195	BCADR2	O	BCAD24	I/O	I/O	B			8mA	
196	BCADR1	O	BCAD25	I/O	I/O	B			8mA	
197	BREG#	O	BCC/BE3#	I/O	I/O	B			8mA	
198	BBVD2/ BSPKR#	I	BCAUDIO	I	I(PU)	B	PU	PU	—	
199	BCADR0	O	BCAD26	I/O	I/O	B			8mA	
200	BWP/ BIOIS16#	I	BCCLKRUN#	I/O	I/O(PU)	B		PU	8mA	2
201	BCDATA3	I/O	BCAD0	I/O	I/O(PD)	B	PD		8mA	1
202	BCADR8	O	BCC/BE1#	I/O	I/O	B			8mA	
203	BCADR9	O	BCAD14	I/O	I/O	B			8mA	
204	BCDATA13	I/O	BCAD6	I/O	I/O(PD)	B	PD		8mA	1
205	BCADR10	O	BCAD9	I/O	I/O	B			8mA	
206	BCDATA4	I/O	BCAD1	I/O	I/O(PD)	B	PD		8mA	1
207	BCADR11	O	BCAD12	I/O	I/O	B			8mA	
208	BCADR19	O	—	I/O	I/O(PU)	B		PU	8mA	2

Pin Type

I: Input Pin, O: Output Pin, I/O: Input Output Pin,
I(PU): Input Pin with Internal Pullup Resister,
I(PD): Input Pin with Internal Pulldown Resister,
I/O(PU): Input Output Pin with Internal Pullup Resister,
I/O(PD): Input Output Pin with Internal Pulldown Resister,
O(TS): Three State Output Pin, O(OD): Open Drain Output Pin

Power Rail

P: VCC_PCI, C: VCC_CORE, A: VCC_SLOTA,
B: VCC_SLOTB, 5: VCC_5V

Drive

PCI21: PCI2.1 Compliant,
CB: PCMCIA CardBus PC Card Compliant

Note

1: Pull down is attached when PC Card Interface is configured as 16-bit Interface Mode.
2: Pull up is attached when PC Card Interface is configured as a CardBus Interface Mode.
3: Pull up or Pull down is configured according to the type of a card inserted.

3.3 Pin Functions Outline & Description

In this chapter, the detailed signal pins in RL5C476A are explained. Every signal is divided according to their relational interface.

Card Interface signal pin is multi-functional pin. Card Interface mode is configured automatically by the card insertion ; CardBus card or 16-bit card. And the pin function is redefined again.

mark means the signal is on either active or asserted when the signal is low-level. Otherwise, no-mark means the signal is asserted when the signal is high-level.

The following the notations are used to describe the signal type.

IN	Input Pin
OUT	Output Pin
OUT(TS)	Three State Output Pin
OUT(OD)	Open Drain Output Pin
I/O	Input Output Pin
I/O(OD)	Input Output Pin (Output is Open Drain)
s/h/z	Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives an s/h/z pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving a s/h/z signal any sooner than one clock after the previous owner tri-state is.

3.4 PCI Local Bus interface

Pin Name	Type	Description
		PCI Bus Interface Pin Descriptions
PCICLK	IN	***PCI CLOCK:*** PCICLK provides timing for all transactions on PCI. All other PCI signals are sampled on the rising edge of PCICLK.
CLKRUN#	I/O(OD)	***PCI CLOCK RUN:*** This signal indicates the status of PCICLK and an open drain output to request the starting or speeding up of PCICLK. This pin complies with Mobile PCI specification. This signal has no meaning for 16bit card. Tie to GND if not used.
PCIRST#	IN	***PCI RESET:*** This input is used to initialize all registers, sequences and signals of the RL5C476A to their rest states. All of the outputs of the RL5C476A will be tri-stated during PCIRST is asserted.
AD[31:0]	I/O	***ADDRESS AND DATA:*** Address and Data are multiplexed on the same PCI pins.
C/BE[3:0]#	I/O	***BUS COMMAND AND BYTE ENABLES:*** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
PAR	I/O	***PARITY:*** Parity is even parity across AD[31:0] and C/BE[3:0]#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. The master drives PAR for address and write data phases; the target drives PAR for read data phases.
FRAME#	I/O s/h/z	***CYCLE FRAME:*** This signal is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has complete.
TRDY#	I/O s/h/z	***TARGET READY:*** This signal indicates the initialing agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
IRDY#	I/O s/h/z	***INITIATOR READY:*** This signal indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31:0]. During a read, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
STOP#	I/O s/h/z	***STOP:*** This signal indicates the current target is requesting the master to stop the current transaction.
IDSEL	IN	***INITIALIZATION DEVICE SELECT:*** This signal is used as a chip select during configuration read and write transactions.
DEVSEL#	I/O s/h/z	***DEVICE SELECT:*** When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
PERR#	I/O s/h/z	***PARITY ERROR:*** This signal is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The RL5C476A drives this output active "low" if it detects a data parity error during a write phase.
SERR#	OUT(OD)	***SYSTEM ERROR:*** This signal is pure open drain. The RL5C476A actively drives this output for a single PCI clock when it detects an address parity error on either the primary bus or the secondary bus.
REQ#	OUT(TS)	***REQUEST:*** This signal indicates to the arbiter that the RL5C476A desires use of the bus. This is a point to point signal.
GNT#	IN	***GRANT:*** This signal indicates the RL5C476A that access to the bus has been granted. This is a point to point signal.

3.5 System Interrupt Signals

Pin Name	Type	Description
		System Interrupt Pin Descriptions
INTA#	OUT(OD)	***PCI INTERRUPT REQUEST A:*** This signal indicates a programmable interrupt request generated from the card socket A interface. This signal is connected PCI bus INTA# interrupt line.
INTB#	OUT(OD)	***PCI INTERRUPT REQUEST B:*** This signal indicates a programmable interrupt request generated from the card socket B interface. This signal is connected PCI bus INTB# interrupt line.
IRQ3/GPIO0 IRQ4/GPIO1 IRQ5/GPIO2 IRQ7/GPIO3 IRQ9/SRIRQ# IRQ10/LEDA# IRQ11/LEDB# IRQ12/ LEDOUT IRQ14/ AZVEN# IRQ15/ BZVEN#	OUT(TS)	***SYSTEM INTERRUPT REQUEST IRQ 3-15:*** These signals indicate the interrupts requests from one of the cards and are connected to the ISA bus IRQx signal. IRQ12 is reassigned as an LED output when LED enable bit in ATA control register is set to one. When Serial IRQ Enable bit in Misc Control register is set to one, IRQ9 is reassigned as SRIRQ# signal, at the same time IRQ14,15 are reassigned as AZVEN#, BZVEN# signals ; ZV port buffer control signal, and IRQ10,11 are reassigned as LEDA#, LEDB# signals. When Serial IRQ signal is enabled, IRQ3,4,5 and 7 are assigned as GPIO (General Purpose I/O) pins. These are input/output pins determined by user without effect on the controller transaction.
RI_OUT# /PME#	OUT	***RING INDICATE OUTPUT:*** When 16-bit card is inserted, this signal is assigned as RI_OUT# from a socket's RI# input when Ring Indicate Enable bit in Interrupt and General control register is set to one. ***POWER MANAGEMENT EVENT:*** This signal is reassigned as a signal equivalent to Power Management Event when PME Enable bit in Power Management Control/Status register is set to one. PCI Bus Power Management Spec requires for PME# to be open drain output. An external gate is required to become an open drain output because this pin outputs "H" or "L".

3.6 16-bit PC Card Interface Signals

Pin Name	Type	Description
		16-bit PC Card Interface Pin Descriptions
ACDATA[15:0] BCDATA[15:0]	I/O	***16-bit Card DATA BUS SIGNALS [15:0]:*** Input buffer is disabled when the card socket power supply is off or card is not inserted.
ACADR[25:0] BCADR[25:0]	OUT(TS)	***16-bit Card ADDRESS BUS SIGNALS [25:0]:***
AIOR# BIOR#	OUT(TS)	***16-bit Card I/O READ:***
AIOW# BIOW#	OUT(TS)	***16-bit Card I/O WRITE:***
AOE# BOE#	OUT(TS)	***16-bit Card OUTPUT ENABLE:***
AWE# BWE#	OUT(TS)	***16-bit Card WRITE ENABLE:***
ACE1# BCE1#	OUT(TS)	***16-bit Card CARD ENABLE 1:***
ACE2# BCE2#	OUT(TS)	***16-bit Card CARD ENABLE 2:***

Pin Name	Type	Description
		16-bit PC Card Interface Pin Descriptions
AREG# BREG#	OUT(TS)	***16-bit Card ATTRIBUTE MEMORY SELECT:*** Memory access is limited to Attribute memory when this signal is "low". During normal access for I/O, this signal is kept "low" and "high" for DMA transfers.
AREADY/ AIREQ# BREADY/ BIREQ#	IN	***16-bit Card READY/BUSY or INTERRUPT REQUEST:*** This signal has two different functions. READY/BUSY# input on the memory PC card, and IREQ# input on the I/O card.
AWP/ AIOIS16# BWP/ BIOIS16#	IN	***16-bit Card WRITE PROTECT or CARD IS 16-BIT PORT:*** This signal has two different functions. Write Protect Switch input on the memory PC card, and IOIS16 input on the I/O card.
ARESET BRESET	OUT(TS)	***16-bit Card CARD RESET:***
AWAIT# BWAIT#	IN	***16-bit Card BUS CYCLE WAIT:***
ABVD1/ ASTSCHG#/ ARI# BBVD1/ BSTSCHG#/ BRI#	IN	***16-bit Card BATTERY VOLTAGE DETECT 1 or STATUS CHANGE:*** This signal has three different functions. The battery voltage detect input 1 on the memory PC card, and Card Status Change#/Ring Indicate# input on the I/O card.
ABVD2/ ASPKR#/ ALED BBVD2/ BSPKR#/ BLED	IN	***16-bit Card BATTERY VOLTAGE DETECT 2 or DIGITAL AUDIO or LED INPUT:*** This signal has three different functions. The battery voltage detect input 2 on the memory PC card, and SPEAKER# input or LED input on the I/O card.
AINPACK# BINPACK#	IN	***16-bit Card INPUT ACKNOWLEDGE:***
ACD1# BCD1#	IN	***16-bit Card CARD DETECT 1:*** CD[2:1]# pins are used to detect the card insertion. CD[2:1]# pins are used in conjunction with VS[2:1]# to decode card type information.
ACD2# BCD2#	IN	***16-bit Card CARD DETECT 2:*** CD[2:1]# pins are used to detect the card insertion. CD[2:1]# pins are used in conjunction with VS[2:1]# to decode card type information.
AVS1# BVS1#	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 1:*** VS[2:1]# pins are used in conjunction with CD[2:1] to decode card type information.
AVS2# BVS2#	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 2:*** VS[2:1]# pins are used in conjunction with CD[2:1]# to decode card type information.

3.7 CardBus PC Card Interface Signals

Pin Name	Type	Description
		CardBus PC Card Interface Pin Descriptions
ACCLK BCCLK	OUT(TS)	***CardBus Clock:*** This signal provides timing for all transactions on the PC Card Standard 95 interface and it is an input to every PC Card Standard 95 device. All other CardBus PC Card signals, except CRST# (upon assertion), CCLKR, CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD[2:1]#, and CVS[2:1], are sampled on the rising edge of CCLK, and all timing parameters are defined with respect to this edge.
ACCLKRUN# BCCLKRUN#	I/O s/h/z	***CardBus Clock Run:*** This signal is used by cards to request starting (or speeding up) clock ; CCLK. CCLKRUN# also indicates the clock status. For PC cards, CCLKRUN# is an open drain output and it is also an input. The RL5C467 indicates the clock status of the primary bus to the CardBus card.
ACRST# BCRST#	OUT(TS)	***CardBus Card Reset:*** This signal is used to bring CardBus Card specific registers, sequencers and signals to a consistent state. Anytime CRST# is asserted, all CardBus card output signals will be driven to their begin state.
ACAD[31:0] BCAD[31:0]	I/O	***CardBus Address/Data:*** These signals are multiplexed on the same CardBus card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus card supports both read and write bursts. CAD[31:0] contain a physical address (32 bits). For I/O, this is a byte address ; for configuration and memory it is a DWORD address. During data phases, CAD[7:0] contain the east significant byte(LSB) and CAD[31:24] contain the most significant byte(MSB). Write data is stable and valid when CIRDY# is asserted and read data is stable and valid when CTRDY# is asserted. Data is transferred during those clocks where both CIRDY# and CTRDY# are asserted.
ACC/BE[3:0]# BCC/BE[3:0]#	I/O	***CardBus Command/Bye Enables:*** These signals are multiplexed on the same CardBus card pins. During the address phase of a transaction, CC/BE[3:0]# define the bus command. During the data phase, CC/BE[3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CC/BE[0]# applies to byte 0 (LSB) and CC/BE[3]# applies to byte 3 (MSB).
ACPAR BCPAR	I/O	***CardBus Parity:*** This signal is even parity across CAD[31:0] and CC/BE[3:0]#. Parity generation is required by all CardBus card agents. CPAR is stable and valid clock after either CIRDY# is asserted on a write transaction or CTRDY# is asserted on a read transaction. Once CPAR is valid, it remains valid until one clock after the completion of the current data phase. (CPAR has the same timing as CAD[31:0] but delayed by one clock.) The master drives CPAR for address and write data phases ; the target drives CPAR for read data phases.
ACFRAME# BCFRAME#	I/O s/h/z	***CardBus Cycle Frame***: This signal is driven by the current master to indicate the beginning and duration of a transaction. CFRAME# is asserted to indicate that a bus transaction is beginning. While CFRAME# is asserted, data transfers continue. When CFRAME# is deasserted, the transaction is in the final data phase.
ACIRDY# BCIRDY#	I/O s/h/z	***CardBus Initiator Ready:*** This signal indicates the initiating agent's(bus master's) ability to complete the current data phase of the transaction. CIRDY# is used in conjunction with CTRDY#. A data phase is completed on any clock both CIRDY# and CTRDY# are sampled asserted. During a write, CIRDY# indicates that valid data is present on CAD[31:0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
ACTRDY# BCTRDY#	I/O s/h/z	***CardBus Target Ready:*** This signal indicates the agent's(selected target's) ability to complete the current data phase of the transaction. CTRDY# is used in conjunction with CIRDY#. A data phase is completed on any clock both CTRDY# and CIRDY# are sampled asserted. During a read, CTRDY# indicates that valid data is present on CAD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
ACSTOP# BCSTOP#	I/O s/h/z	***CardBus Stop:*** This signal indicates the current target is requesting the master to stop the current transaction.
ACDEVSEL# BCDEVSEL#	I/O s/h/z	***CardBus Device Select:*** This signal indicates the driving device has decoded its address as the target of the current access when actively driven. As an input, CDEVSEL# indicates whether any device on the bus has been selected.
ACREQ# BCREQ#	IN	***CardBus Request:*** This signal indicates to the arbiter that this agent desires use of the bus. Every master has its own CREQ#.

Pin Name	Type	Description
CardBus PC Card Interface Pin Descriptions (Continued)		
ACGNT# BCGNT#	OUT	***CardBus Grant:*** This signal indicates to the agent that access to the bus has been granted. Every master has its own CGNT#.
ACPERR# BCPERR#	I/O s/h/z	***CardBus Parity Error:*** This signal is only for the reporting of data parity errors during all CardBus Card transactions except a Special Cycle. An agent cannot report a CPERR# until it has claimed the access by asserting CDEVSEL# and completed a data phase.
ACSERR# BCSERR#	IN	***CardBus System Error:*** This signal is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result could be catastrophic.
ACINT# BCINT#	IN	***CardBus Interrupt Request:*** This signal is an input signal from CardBus card. It is level sensitive, and asserted low (negative true), using an open drain output driver. The assertion and deassertion of CINT# is asynchronous to CCLK.
ACSTSCHG BCSTSCHG	IN	***CardBus Card Status Change:*** This signal is an input signal used to alert the system to changes in the READY, WP, or BVD[2:1] conditions of the card. It is also used for the system and/or CardBus card interface Wake up. CSTSCHG is asynchronous to CCLK.
ACAUDIO BCAUDIO	IN	***CardBus Card Audio:*** This signal is a digital audio input signal from a CardBus Card to the system's speaker. CAUDIO has no relationship to CCLK.
ACCD1# BCCD1#	IN	***CardBus Card Detect 1:*** CCD[2:1]# pins are used to detect the card insertion. CCD[2:1]# pins are used in conjunction with CVS[2:1] to decode card type information.
ACCD2# BCCD2#	IN	***CardBus Card Detect 2:*** CCD[2:1]# pins are used to detect the card insertion. CCD[2:1]# pins are used in conjunction with CVS[2:1] to decode card type information.
ACVS1 BCVS1	I/O	***CardBus Card Voltage Sense 1:*** CVS[2:1] pins are used in conjunction with CCD[2:1]# to decode card type information.
ACVS2 BCVS2	I/O	***CardBus Card Voltage Sense 2:*** CVS[2:1] pins are used in conjunction with CCD[2:1]# to decode card type information.

3.8 Socket Power Control Signals

Pin Name	Type	Description
		Socket Power Control Signal Descriptions
AVCC5EN# BVCC5EN#	OUT	***VCC 5V ENABLE:***
AVCC3EN# BVCC3EN#	OUT	***VCC 3.3V ENABLE:***
AVPPEN0 BVPPEN0	OUT	***VPP ENABLE 0:***
AVPPEN1 BVPPEN1	OUT	***VPP ENABLE 1:***

3.9 Audio

Pin Name	Type	Description
		Audio Pin Descriptions
SPKROUT#	OUT(TS)	***SPEAKER OUTPUT:*** This signal is a digital audio output from SPKR#.

3.10 Hardware Suspend

Pin Name	Type	Description
		Hardware Suspend
HWSPND#	IN	***Hardware Suspend:*** This signal works as HWSPND# input. PCIRST# is not accepted as long as HWSPND# is asserted so that VCC_PCI can be powered off. When Serial IRQ mode is set, HWSPND# must be asserted after Serial IRQ mode on the chip-set has been deasserted. When Hardware Suspend mode is off, HWSPND# must be deasserted before Serial IRQ mode is enabled.

3.11 Power and GND

Pin Name	Type	Description
		Power Pin Descriptions
VCC_PCI	PWR	***PCI VCC :*** Power Supply pins for PCI interface signals. This pin can be powered at either 3.3V or 5V.
VCC_CORE	PWR	***CORE VCC :*** Power Supply pins for the internal core logic. This pin must be powered at 3.3V only.
VCC_SLOTA	PWR	***SLOTA VCC :*** Power Supply for Card socket A. This pin can be powered at either 3.3V or 5V.
VCC_SLOTB	PWR	***SLOTB VCC :*** Power Supply for Card socket B. This pin can be powered at either 3.3V or 5V.
VCC_5V	PWR	***5V VCC:*** This supply pin is connected to 5V. In systems where 5V is not available, this pin is connected to 3.3V.
GND	PWR	***GND :***

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum rating

Symbol	Parameter	Min	Unit	Condition	note
Vcc 1	Supply Voltage Range 1	-0.3 ~ 6.6	V	GND=0V	1
Vcc 2	Supply Voltage Range 2	-0.3 ~ 5.0	V	GND=0V	2
Vte	Voltage on Any Pin	-0.3 ~ Vcc+0.3	V	GND=0V	
Topr	Ambient Temperature under bias	-40 ~ 85	°C		
Tstg	Storage Temperature Range	-55 ~ 125	°C		

note 1 : Applied for Vcc_xxx except for Vcc_core .
note 2 : Applied for Vcc_core only.

Note: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

4.2 DC Characteristics

4.2.1 Recommended Operating Conditions for Power Supply

Power Pin	Parameter	Min	Typ	Max	Unit	Note
VCC_PCI, VCC_ZV	Supply Voltage for PCI interface (5.0V Operation)	4.75	5.0	5.25	V	
VCC_PCI, VCC_ZV	Supply Voltage for PCI interface (3.3V Operation)	3.0	3.3	3.6	V	
VCC_CORE	Supply Voltage for Core Logic	3.0	3.3	3.6	V	
VCC_5V	Supply Voltage for 5V Control Signals	3.0	5.0	5.25	V	
VCC_SLOT A/B	Supply Voltage for Card Socket A/B (5.0V Operation)	4.75	5.0	5.25	V	
VCC_SLOT A/B	Supply Voltage for Card Socket A/B (3.3V Operation)	3.0	3.3	3.6	V	

4.2.2 PCI Interface

For 5V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.0	Vcc_PCI +0.5	V		1
VIL	Input Low Voltage	-0.5	0.8	V		1
VOH	Output High Voltage	2.4		V	Iout=-2mA	1
VOL	Output Low Voltage		0.55	V	Iout=6mA	1
IIH	Input High Leakage Current		70	μA	Vin=2.7V	1
IIL	Input Low Leakage Current		-70	μA	Vin=0.5V	1
Cin	Input Pin Capacitance		10	pF		1
Cclk	PCICLK Pin Capacitance		12	pF		1

For 3.3V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.5Vcc_PCI	Vcc_PCI+0.5	V		1
VIL	Input Low Voltage	-0.5	0.3Vcc_PCI	V		1
VOH	Output High Voltage	0.9Vcc_PCI		V	Iout=-500μA	1
VOL	Output Low Voltage		0.1Vcc_PCI	V	Iout=1500μA	1
IILk	Input Leakage Current		±10	μA	Vin=0~Vcc_PCI	1
Cin	Input Pin Capacitance		10	pF		1
Cclk	PCICLK Pin Capacitance		12	pF		1

Note 1: Applied for PCICLK, CLKRUN#, PCIRST#, AD[31:0], C/BE#[3:0], PAR, FRAME#, IRDY#, TRDY#,STOP#, DEVSEL#, IDSEL, PERR#, SERR#, REQ#, GNT#, INTA#, INTB# pins

4.2.3 16-bit PC Card Interface

For 5V signaling

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.4		Vcc_SLOT +0.3	V		2
VIL	Input Low Voltage	-0.3		0.8	V		2
VOH1	Output High Voltage	2.4			V	Iout=-8mA	2
VOH2	Output High Voltage	2.4			V	Iout=-4mA	2,3
VOL1	Output Low Voltage			0.4	V	Iout=8mA	2
VOL2	Output Low Voltage			0.4	V	Iout=4mA	2,3
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_SLOTA/B	2
IIL1	Input Leakage Current (Pull-up)		-120		μA	Vin=0	2,4
IIL2	Input Leakage Current (Pull-down)		25		μA	Vin=Vcc_SLOTA/B	2,5
Cin	Input Pin Capacitance			10	pF		2

For 3.3V signaling

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.0		Vcc_SLOT +0.3	V		2
VIL	Input Low Voltage	-0.3		0.6	V		2
VOH1	Output High Voltage	2.4			V	Iout=-4mA	2
VOH2	Output High Voltage	2.4			V	Iout=-2mA	2,3
VOL1	Output Low Voltage			0.4	V	Iout=4mA	2
VOL2	Output Low Voltage			0.4	V	Iout=2mA	2,3
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_SLOTA/B	2
IIL1	Input Leakage Current (Pull-up)		-50		μA	Vin=0	2,4
IIL2	Input Leakage Current (Pull-down)		10		μA	Vin=Vcc_SLOTA/B	2,5
Cin	Input Pin Capacitance			10	pF		2

Note 2: Applied for CADR[25:0], CDATA[15:0], CE[2:1]#, IOR#, IOW#, OE#, WE#, REG#, RDY/IREQ#, WAIT#, WP/IOIS16#, RESET, BVD1/STSCHG#/RI#, BVD2/SPKR#, INPACK# pins, if Card interface is configured as a 16-bit Card Socket.
Note 3: Applied for RESET pins
Note 4: Applied for RDY/IREQ#, WAIT#, BVD1/STSCHG#/RI#, BVD2/SPKR#, INPACK# pins
Note 5: Applied for CDATA[15:0]pins

4.2.4 CardBus PC Card Interface

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.475x Vcc_SLOTA/B		Vcc_SLOT +0.5	V		6
VIL	Input Low Voltage	-0.5		0.325x Vcc_SLOT	V		6
VOH	Output High Voltage	0.9Vcc_SLOTA/B			V	Iout=-150μA	6
VOL	Output Low Voltage			0.1Vcc_SLOT	V	Iout=700μA	6
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_SLOTA/B	6
IIL1	Input Leakage Current (Pull-up)		-230		μA	Vin=0	6,7
Cin	Input Pin Capacitance			10	pF		6

Note 6: Applied for CCLK, CCLKRUN#, CRST#, CAD[31:0], CC/BE#[3:0], CPAR, CFRAME#, CIRDY#,CTRDY#,CSTOP#, CDEVSEL#, CBLOCK#, CPERR#, CSERR#, CREQ#, CGNT#, CINT#, CAUDIO, CSTSCHG pins, if Card interface is configured as a CardBus Card Socket.
Note 7 : Applied for CCLKRUN#, CIRDY#,CTRDY#,CSTOP#, CDEVSEL#, CPERR#, CSERR#, CREQ#, CINT#, CAUDIO pins
Note 8 : Applied for CSTSCHG pins

4.2.5 PC Card Interface Card detect Pins and System Interface Pins

PC Card Interface Card Detect Pins and System Interface Pins

(VCC_CORE=3.0~3.6V, VCC_5V=4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.4		Vcc_5V+0.3	V		9,11
VIL	Input Low Voltage	-0.3		0.8	V		9,11
VOH1	Output High Voltage	2.4			V	Iout=-4mA	10
VOH2	Output High Voltage	2.4			V	Iout=-1mA	11
VOL1	Output Low Voltage			0.4	V	Iout=4mA	10
VOL2	Output Low Voltage			0.4	V	Iout=1mA	11
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_5V	11
IIL1	Input Leakage Current (Pull-up)		-140		μA	Vin=0	9
IOZ	Hi-Z Output Leakage Current			±10	μA	Vout=0~Vcc_5V	10

Note 9: Applied for CD1#(CCD1#), CD2#(CCD2#) pins
Note 10: Applied for RI_OUT#, SPKROUT#,VCC5EN#, VCC3EN#, VPPEN0, VPPEN1 pins
Note 11: Applied for VS1#(CVS1#), VS2#(CVS2#), pins

4.2.6 IRQ3-15 pin

For PCI 5V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VOH	Output High Voltage	2.4		V	Iout=-8mA	12
VOL	Output Low Voltage		0.4	V	Iout=8mA	12
IOZ	Hi-Z Output Leakage Current		±10	μA	Vout=0~Vcc_PCI	12

For PCI 3.3V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VOH	Output High Voltage	2.4		V	Iout=-4mA	12
VOL	Output Low Voltage		0.4	V	Iout=4mA	12
IOZ	Hi-Z Output Leakage Current		±10	μA	Vout=0~Vcc_PCI	12

Note 12: Applied for IRQ3-15 pins

4.2.7 Power Consumption

Power Supply Current

Power Pin	Parameter	Min	Typ	Max	Unit	Condition
Iccstd	Power Supply Current, Standby			50	μA	fclk(PCICLK)=0, Vin=0or Vcc
Iccsusp	Power Supply Current, Hardware Suspend Mode			30	μA	Mode = H/W Bridge Suspend VCC_SLOT=5.0V VCC_5V=5.0V VCC_PCI=0V VCC_CORE=3.3V Vin=0 or Vcc
Icc	Power Supply Current, Operating			50	mA	fclk(PCICLK)=33Mhz VCC_SLOT=5.0/3.3V VCC_5V=5.0V VCC_PCI=5.0V VCC_CORE=3.3V Vin=0 or Vcc

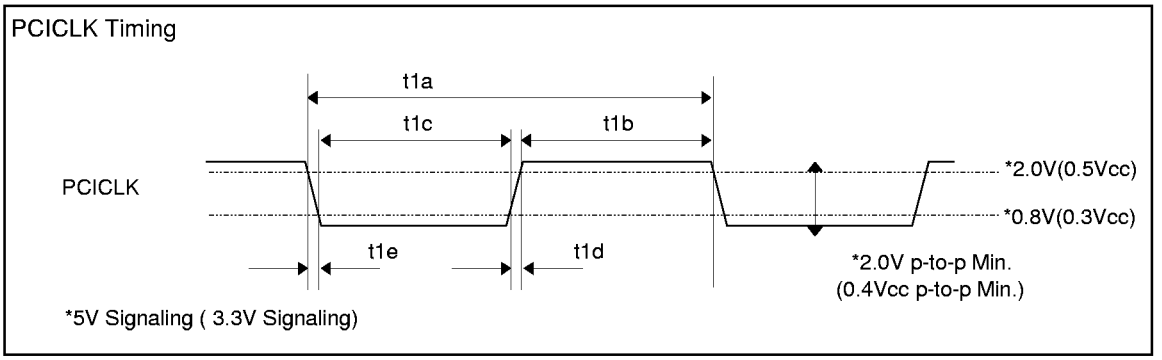
4.3 AC Characteristics

4.3.1 PCI Interface Signals

PCI Clock

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	PCICLK				
t1a	Cycle Time, PCICLK	30		ns	
t1b	Pulse Width Duration, PCICLK High	11		ns	
t1c	Pulse Width Duration,PCICLK Low	11		ns	
t1d	Slew Rate, PCICLK Rising Edge	1	4	V/ns	
t1e	Slew Rate, PCICLK Falling Edge	1	4	V/ns	

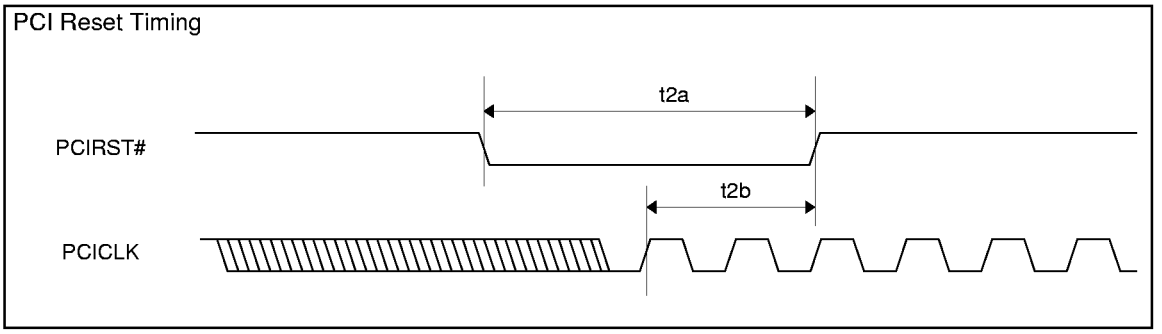


PCICLK Timing

PCI Reset

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	PCIRST#				
t2a	Pulse Duration, PCIRST#	1		ms	
t2b	Setup Time,PCICLK active at PCIRST# Negation	100		µs	

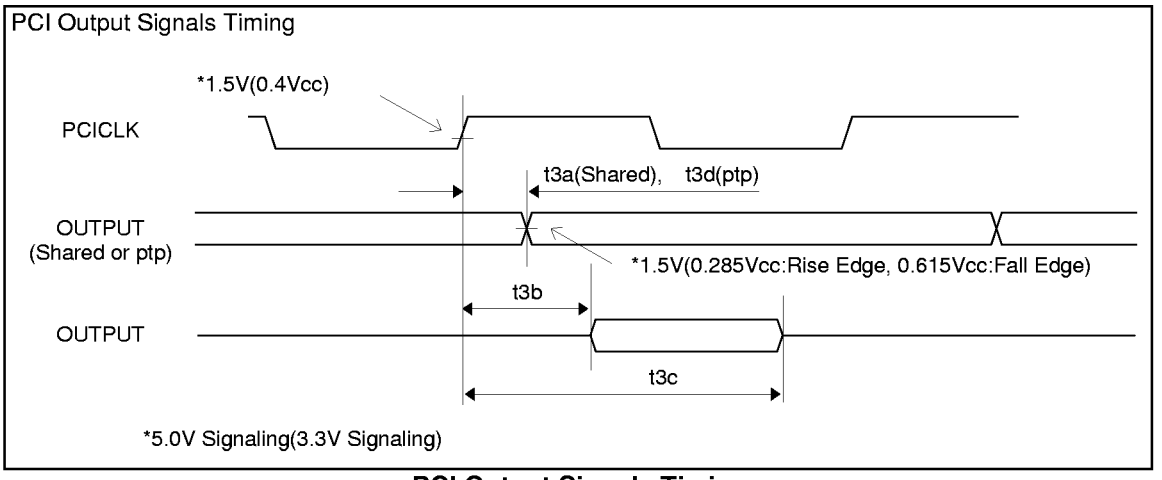


PCI Reset Timing

PCI Interface Output Signals

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	AD[31:0], C/BE#[3:0], PAR, FRAME#,DEVSEL#, IRDY#, TRDY#,STOP#, PERR#, SERR#, CLKRUN#				
t3a	Shared Signal Valid delay time from PCICLK	2	11	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)
t3b	Enable Time, Hi-Z to active delay from PCICLK	2		ns	
t3c	Disable Time, Active to Hi-Z delay from PCICLK		28	ns	
	REQ#				
t3d	Point to Point Signal Valid delay time from PCICLK	2	12	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)

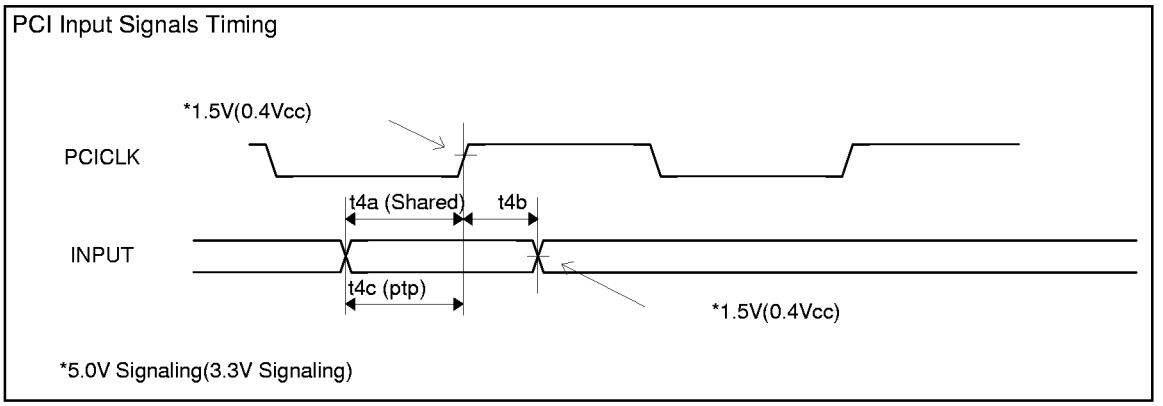


PCI Output Signals Timing

PCI Interface Input Signals

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD[31:0], C/BE#[3:0], PAR, FRAME#,DEVSEL#, IRDY#, TRDY#,STOP#, IDSEL, PERR#, SERR#, CLKRUN#				
t4a	Setup Time, Shared Signal Valid before PCICLK	7		ns	
t4b	Hold Time,Shared Signal Hold Time after PCICLK High	0		ns	
	GNT#				
t4c	Setup Time, Point to Point Signal Valid before PCICLK	10		ns	



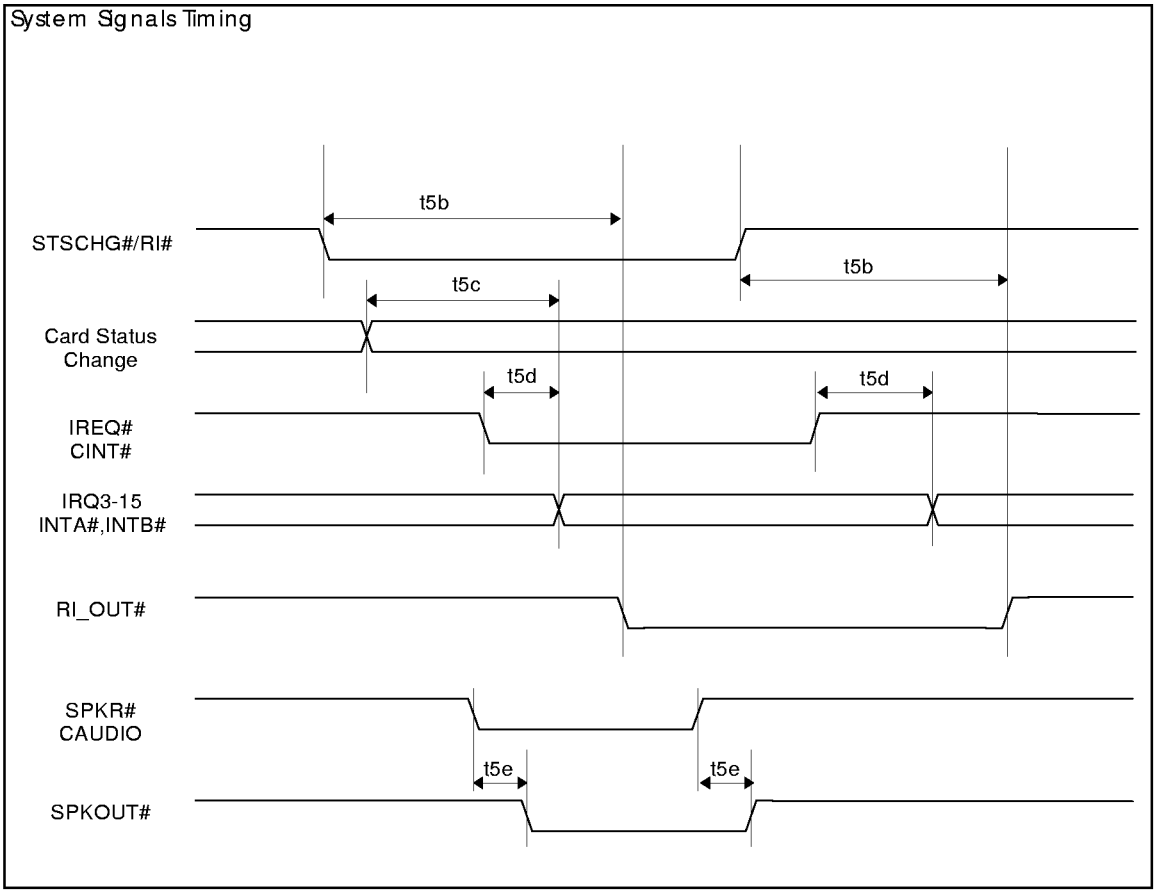
PCI Input Signals Timing

4.3.2 System Interface Signals

System Interface Signals AC Characteristics
(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, VCC_SLOTA/B=3.0~3.6V or 4.75~5.25V, VCC_5V= 4.75~5.25V,Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	RI_OUT#, IRQ3-15, INTA#, INTB#				
t5b	RI# to RI_OUT# Delay		50	ns	
t5c	Card Status Change to IRQ3-15/INTA#,INTB# Delay		2Tcyc+0	ns	1
t5d	Card IREQ#/CINT# to IRQ3-15/INTA#,INTB# Delay		50	ns	
	SPKOUT#				
t5e	SPKR#/CAUDIO to SPKOUT# Delay		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)



System Signals Timing

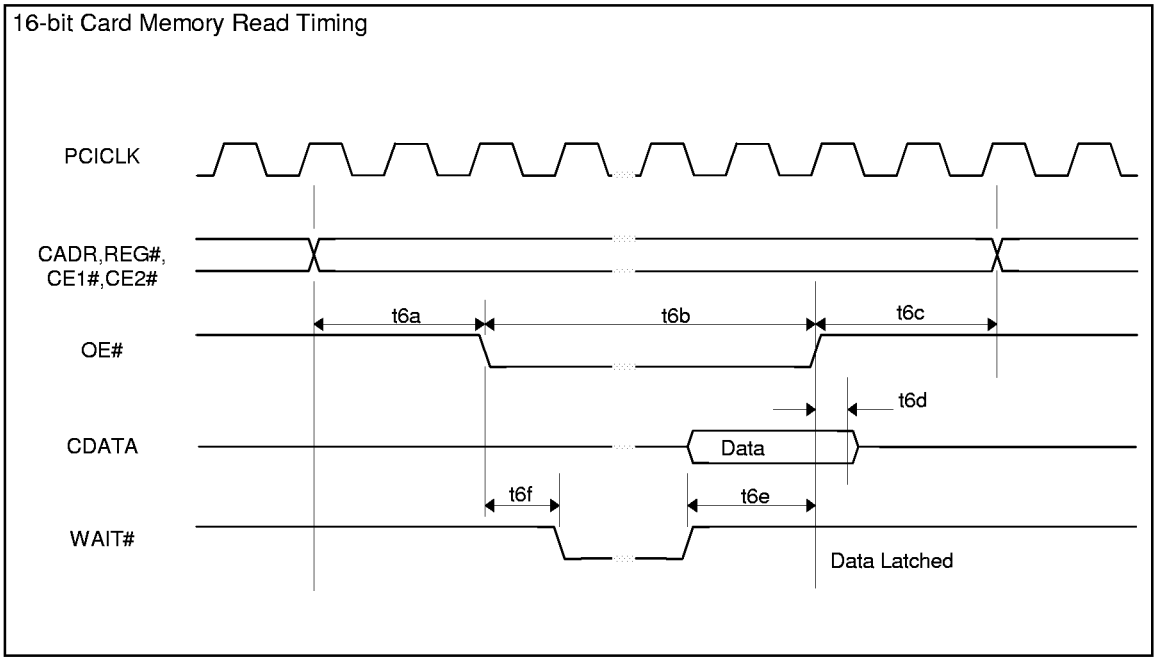
4.3.3 16-bit PC Card Interface Signals

Memory Read

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#, CE[2:1]#				
t6a	Setup Time, CADR[25:0], REG# and CE[2:1]# before OE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t6c	Hold Time, CADR[25:0], REG# and CE[2:1]# after OE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	OE#				
t6b	Pulse Duration, OE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA[15:0]				
t6d	Hold Time, CDATA[15:0] after OE# High	0		ns	
	WAIT#				
t6e	Hold Time, OE# Low after WAIT# High	1Tcyc+0		ns	1
t6f	Valid Delay, OE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)
Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.



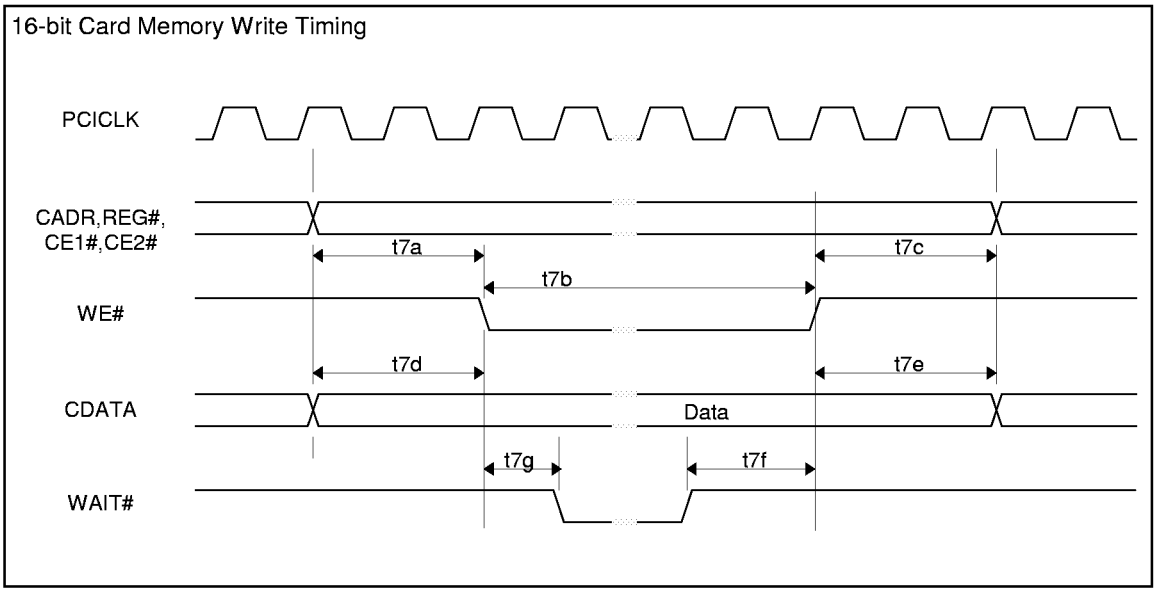
16-bit Card Memory Read Timing

Memory Write

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#, CE[2:1]#				
t7a	Setup Time, CADR[25:0], REG# and CE[2:1]# before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7c	Hold Time, CADR[25:0], REG# and CE[2:1]# after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WE#				
t7b	Pulse Duration, WE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA[15:0]				
t7d	Setup Time, CDATA[15:0] before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7e	Hold Time, CDATA[15:0] after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WAIT#				
t7f	Hold Time, WE# Low after WAIT# High	Tcyc+0		ns	1
t7g	Valid Delay, WE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)
Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.



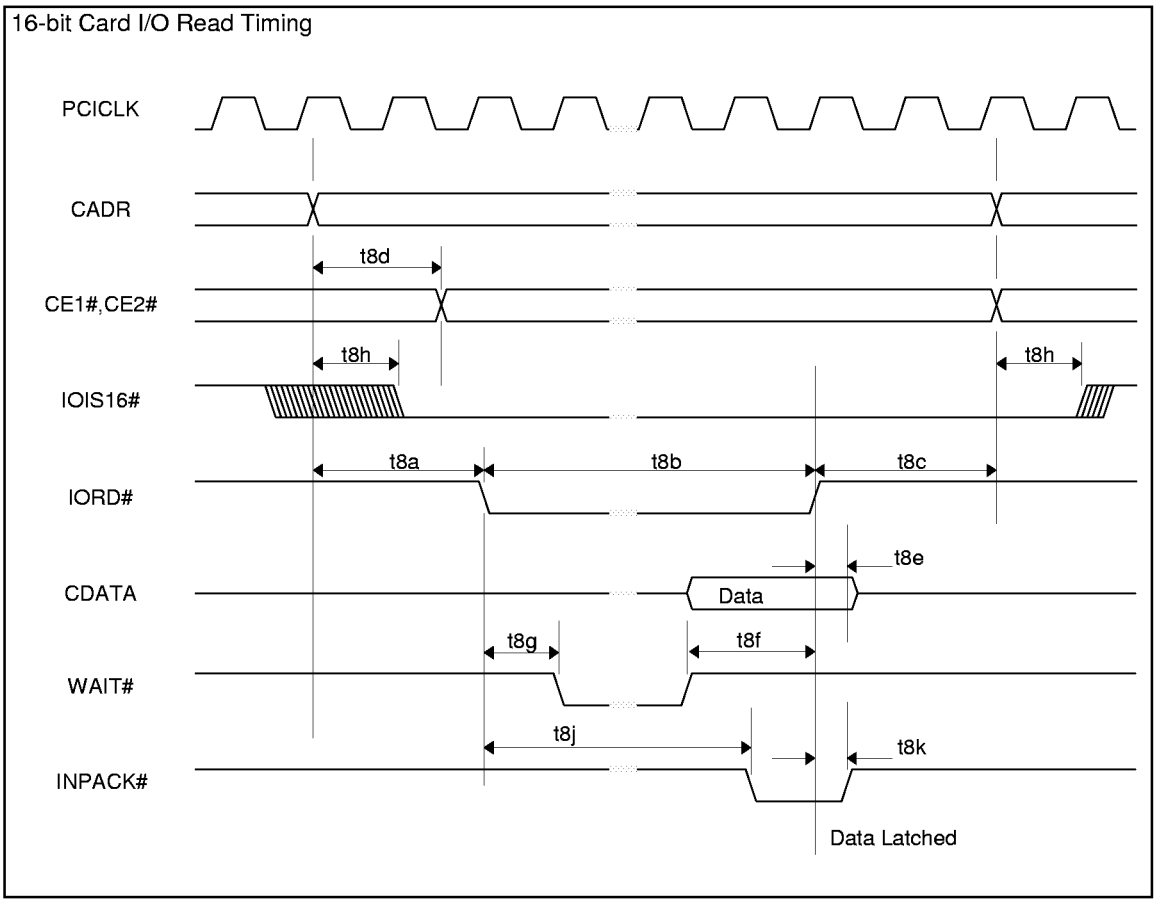
16-bit Card Memory Write Timing

I/O Read

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#				
t8a	Setup Time, CADR[25:0] and REG# before IORD# Low	Tsu-20		ns	1,3 Tsu=2~7Tcyc Programmable
t8c	Hold Time, CADR[25:0] and REG# after IORD # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	IORD#				
t8b	Pulse Duration, IORD # Low	Tpw-20		ns	1,3 Tpw=3~31Tcyc Programmable
	CE[2:1]#				
t8d	Valid Delay, CADR[15:0] and REG# to CE[2:1]#	1Tcyc-10		ns	1
	CDATA[15:0]				
t8e	Hold Time, CDATA[15:0] after IORD # High	0		ns	
	WAIT#				
t8f	Hold Time, IORD # Low after WAIT# High	1Tcyc+0		ns	1
t8g	Valid Delay, IORD # Low to WAIT# Low		50	ns	
	IOIS16#				
t8h	Valid Delay, CADR[25:0] to IOIS16# Low		50	ns	
	INPACK#				
t8k	Hold Time, INPCK# Low afterIORD# High	0		ns	
t8j	Valid Delay, IORD # Low to INPACK# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)
Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.



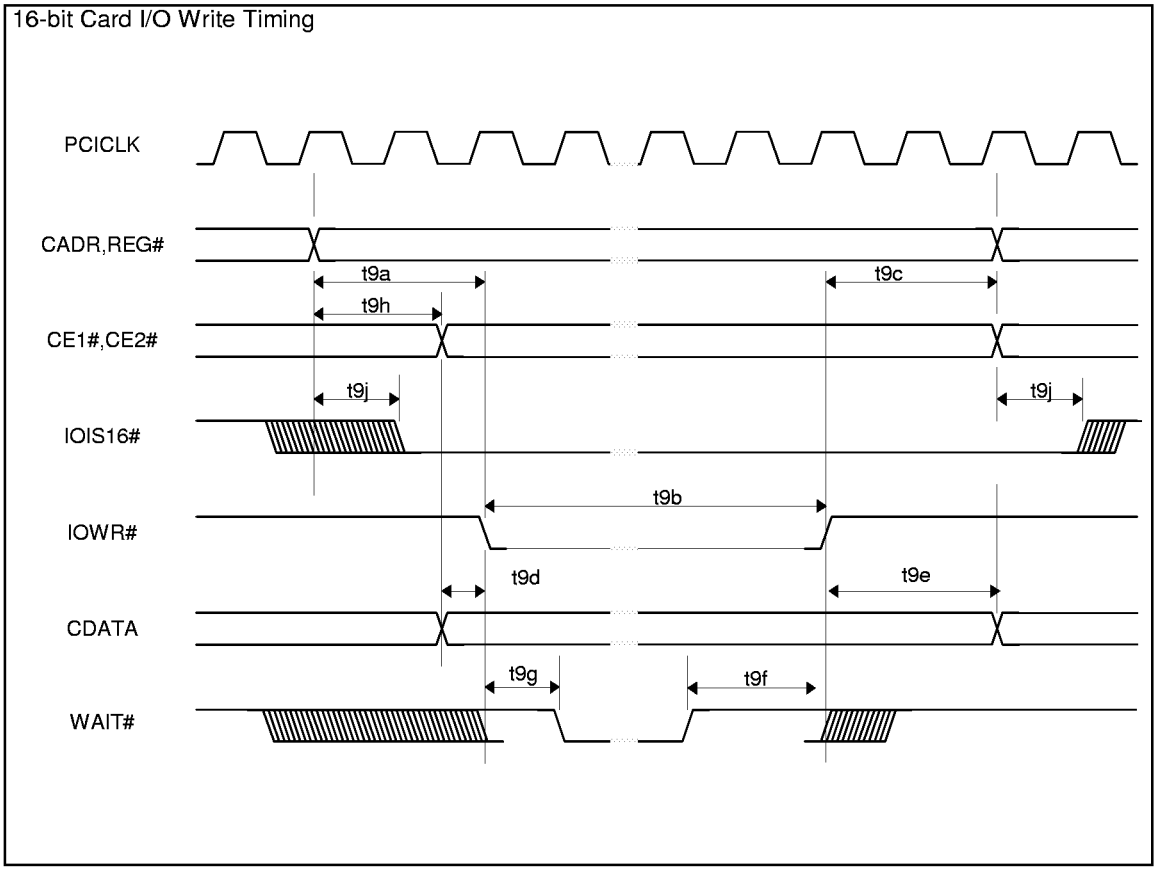
16-bit Card I/O Read Timing

I/O Write

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V or 4.75~5.25V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#				
t9a	Setup Time, CADR[25:0], REG# and CE[2:1]# before IOWR # Low	Tsu-20		ns	1,3 Tsu=2~7Tcyc Programmable
t9c	Hold Time, CADR[25:0], REG# and CE[2:1]# after IOWR # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	IOWR#				
t9b	Pulse Duration, IOWR# Low	Tpw-20		ns	1,3 Tpw=3~31Tcyc Programmable
	CE[2:1]#				
t9h	Valid Delay, CADR[15:0] and REG# to CE[2:1]#	1Tcyc-10		ns	3
	CDATA[15:0]				
t9d	Setup Time, CDATA[15:0] before IOWR # Low	Tsu-2Tcyc-10		ns	1,3 Tsu=3~7Tcyc Programmable
t9e	Hold Time, CDATA[15:0] after IOWR # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	WAIT#				
t9f	Hold Time, IOWR # Low after WAIT# High	1Tcyc+0		ns	3
t9g	Valid Delay, IOWR # Low to WAIT# Low		50	ns	
	IOIS16#				
t9j	Valid Delay, CADR[25:0] and REG# to IOIS16# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)
Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.



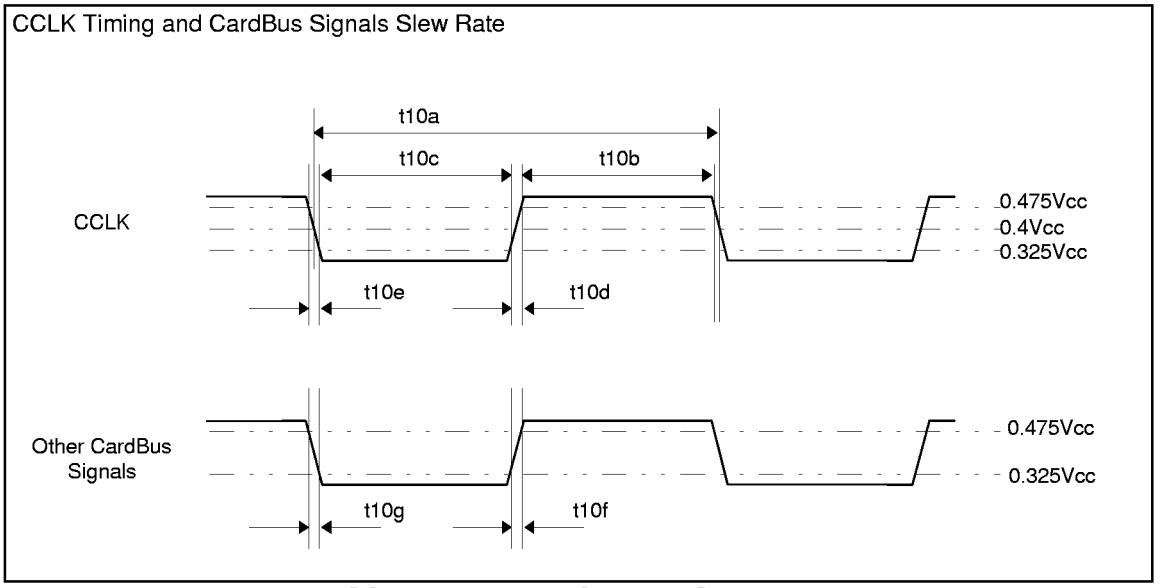
16-bit Card I/O Write Timing

4.3.4 CardBus PC Card Interface Signals

Clock and Signal Slew Rate

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CCLK				
t10a	Cycle Time, CCLK	30		ns	
t10b	Pulse Width Duration, CCLK High	12		ns	
t10c	Pulse Width Duration, CCLK Low	12		ns	
t10d	Slew Rate, CCLK Rising Edge	1	4	V/ns	
t10e	Slew Rate, CCLK Falling Edge	1	4	V/ns	
	Other CardBus Signals				
t10f	Slew Rate, Rising Edge	0.25	1	V/ns	
t10g	Slew Rate, Falling Edge	0.25	1	V/ns	

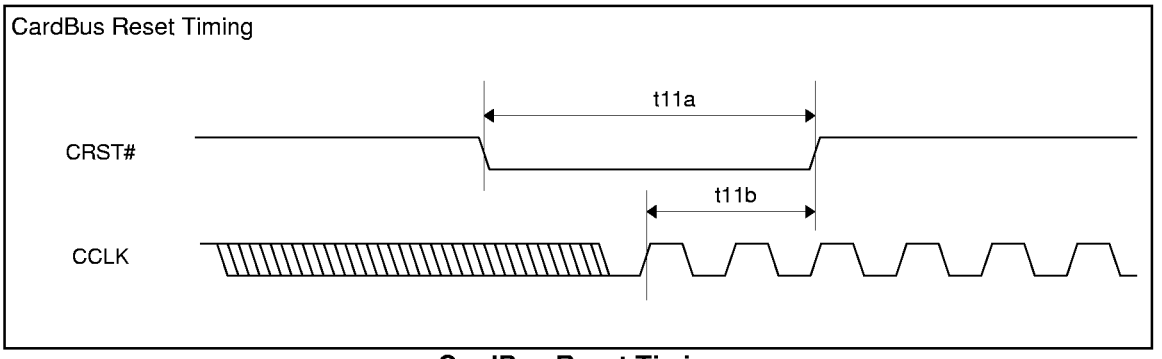


CCLK Timing and CardBus Slew Rate

Card Reset

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CRST#				
t11a	Pulse Duration, CRST#	1		ms	
t11b	Setup Time,CCLK active at CRST# Negation	100		µs	

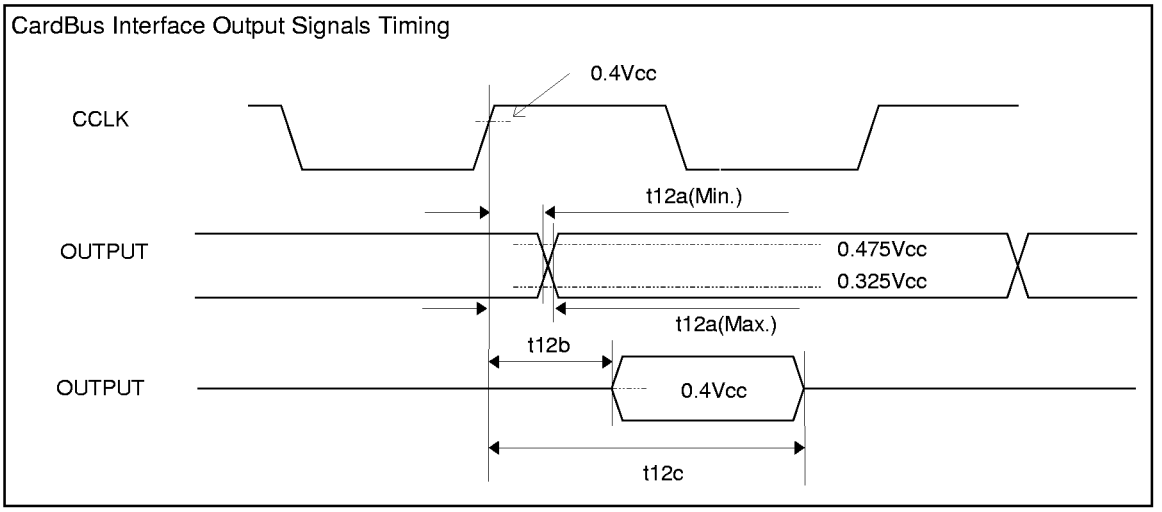


CardBus Reset Timing

Card Output

(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD[31:0], CC/BE#[3:0], CPAR, CFRAME#,CDEVSEL#, CIRDY#, CTRDY#,CSTOP#, CBLOCK#, CPERR#, CSERR#, CCLKRUN#, CGNT#				
t12a	Valid delay time from CCLK	2	18	ns	Min: CL=0 pF Max: CL=30 pF
t12b	Enable Time, Hi-Z to active delay from CCLK	2		ns	
t12c	Disable Time, Active to Hi-Z delay from CCLK		28	ns	

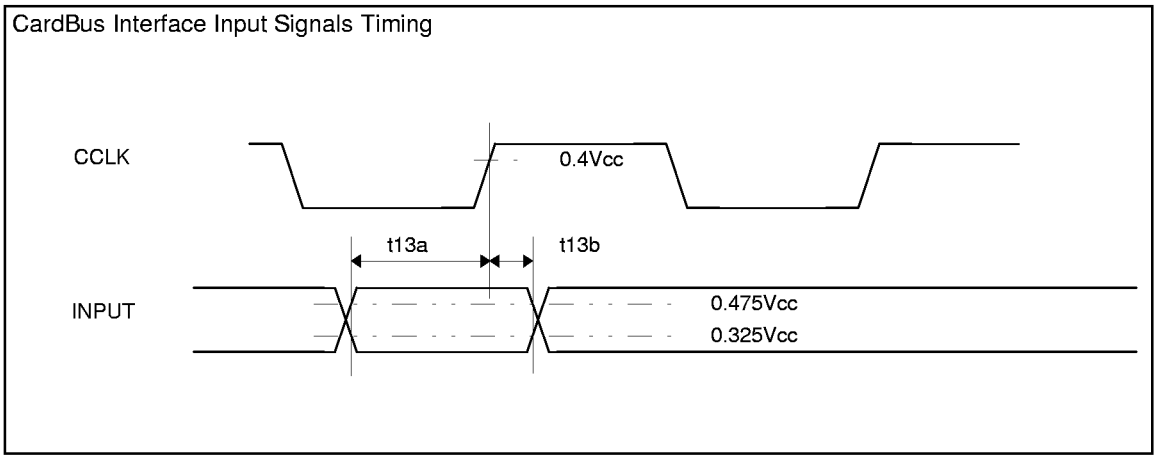


CardBus Interface Output Signals Timing

Card Input

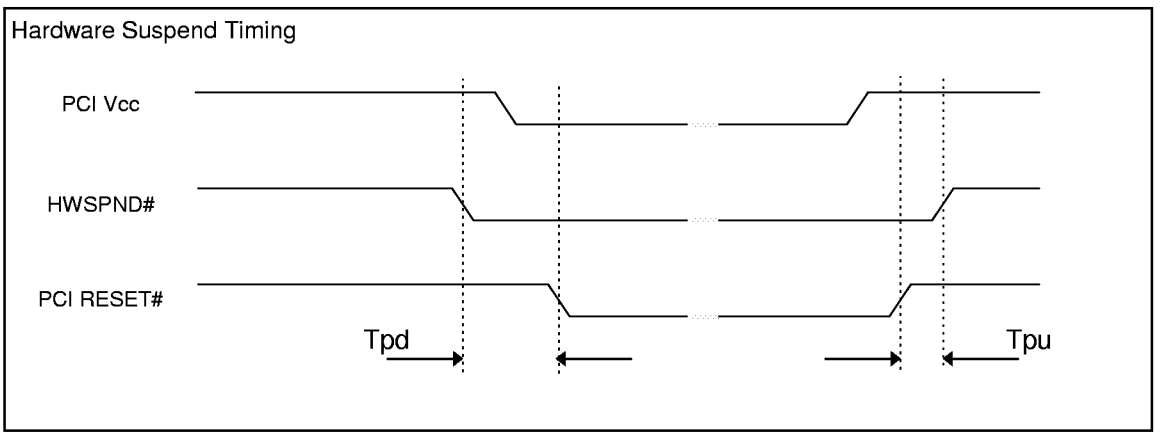
(VCC_CORE=3.0~3.6V, VCC_SLOTA/B=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD[31:0], CC/BE#[3:0], CPAR, CFRAME#,CDEVSEL#, CIRDY#, CTRDY#,CSTOP#, CBLOCK#, CPERR#, CSERR#, CCLKRUN#, CREQ#				
t13a	Setup Time, Signal Valid before CCLK	7		ns	
t13b	Hold Time, Signal Hold Time after CCLK High	0		ns	



CardBus Input Signals Timing

4.3.5 Hardware Suspend mode

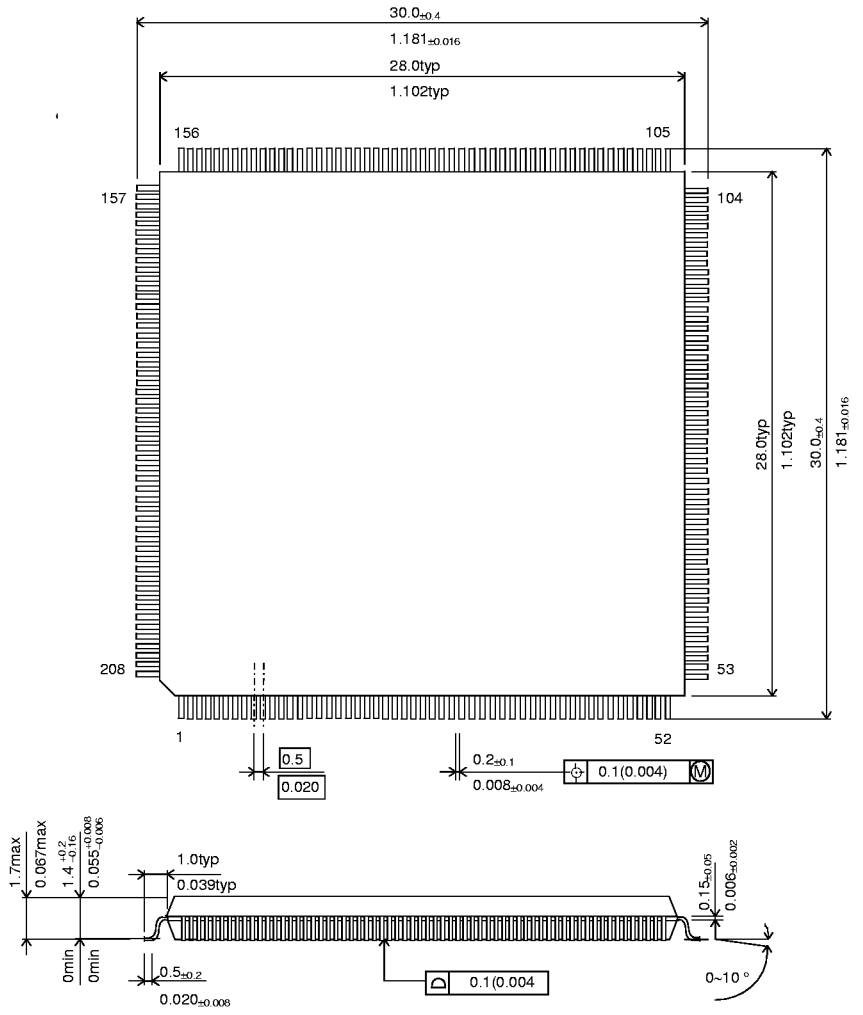


Symbol	Parameter	Min	Typ	Max	Unit
Tpd	HWSPND# to PCIRESET# delay	100			ns
Tpu	HWSPND# to PCIRESET# delay	100			ns

5 MECHANICAL PACKAGE OUTLINE

5.1 208 pin LQFP

PACKAGE CODE	LQFP-208-P11(2828)



Reference

UNIT : MM / INCH

TITLE	LQFP-208PIN(P11) PACKAGE OUTLINE		
DATE	1998, 4, 27	PART NO.	DF-208LQFP-003(W)A
CHECKED	T.SEIGENJI	DRAWN	N.TAKEMURA

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June 1995