8-bit serial in, parallel out driver IC
BU2050F

The BU2050F is a driver IC that is comprised of an 8-bit shift register and a latch (serial in / parallel out). The data read into the shift register can be asynchronously latched. The CMOS outputs can provide 25mA (Max.) of current per output, making this IC ideal for a wide range of applications including driving LEDs.

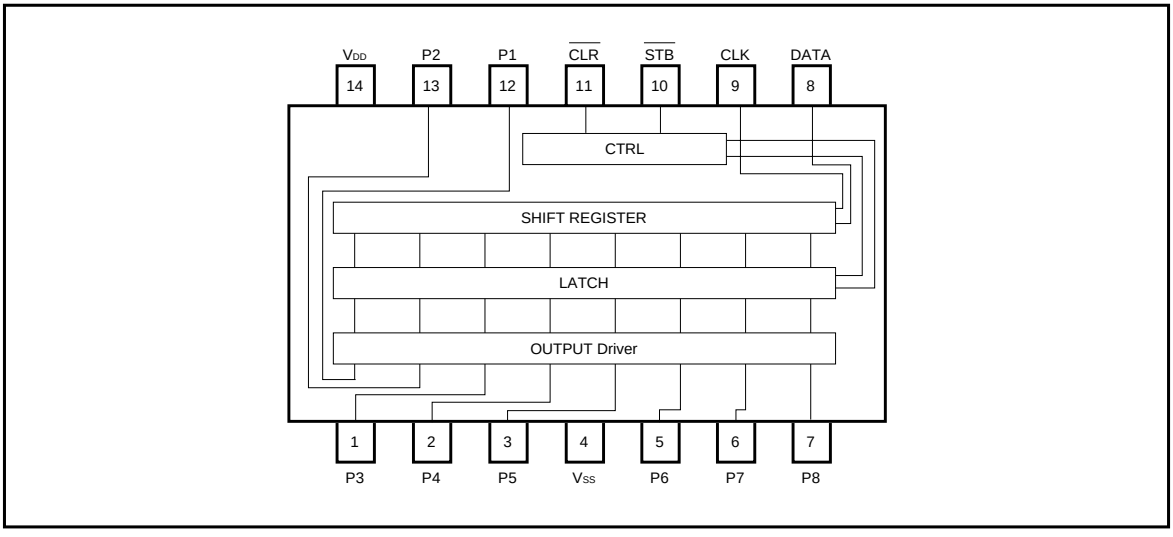
●Applications

Printers, mini-component stereo systems, car audio systems, and musical instruments

●Features

1) Regardless of the clock and data input, the $\overline{CLR}$ pin resets the latch circuit, and sets all outputs to the low level.
2) Output drive capacity: 25mA / output (Max.).
3) Input pin hysteresis: 0.5V (Typ.).

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	P3	Parallel data output
2	P4	Parallel data output
3	P5	Parallel data output
4	V_{SS}	GND
5	P6	Parallel data output
6	P7	Parallel data output
7	P8	Parallel data output
8	DATA	Serial data input
9	CLK	Clock signal input
10	$\overline{STB}$	Strobe signal input When STB is low, the contents of the shift register are output. When STB is high, the contents of the latch circuit and output do not change.
11	$\overline{CLR}$	Reset signal input When CLR is low, the latch circuit is reset, and all outputs (P1 to P8) are set to low. Normally, CLR is high.
12	P1	Parallel data output
13	P2	Parallel data output
14	V_{DD}	Power supply voltage

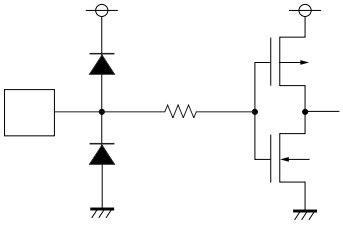
●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	– 0.3 ~ + 7.0	V
Input voltage	I_{SINK}	V_{SS} – 0.3 ~ V_{DD} + 0.5	mA
output voltage	Vo	V_{SS} – 0.3 ~ V_{DD} + 0.5	V
Power dissipation*1	Pd	450	mW
Operating temperature	Topr	– 25 ~ + 85	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

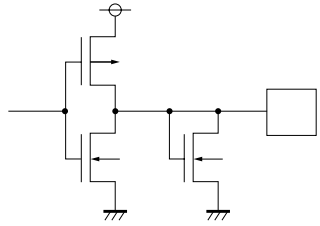
Note: These voltage value ranges are the destruction limits for the IC. They are not the guaranteed operating ranges for the IC.
*1 Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.

●Input / output circuits

(1) DATA, CLK, $\overline{STB}$, $\overline{CLR}$



(2) P1 ~ P8



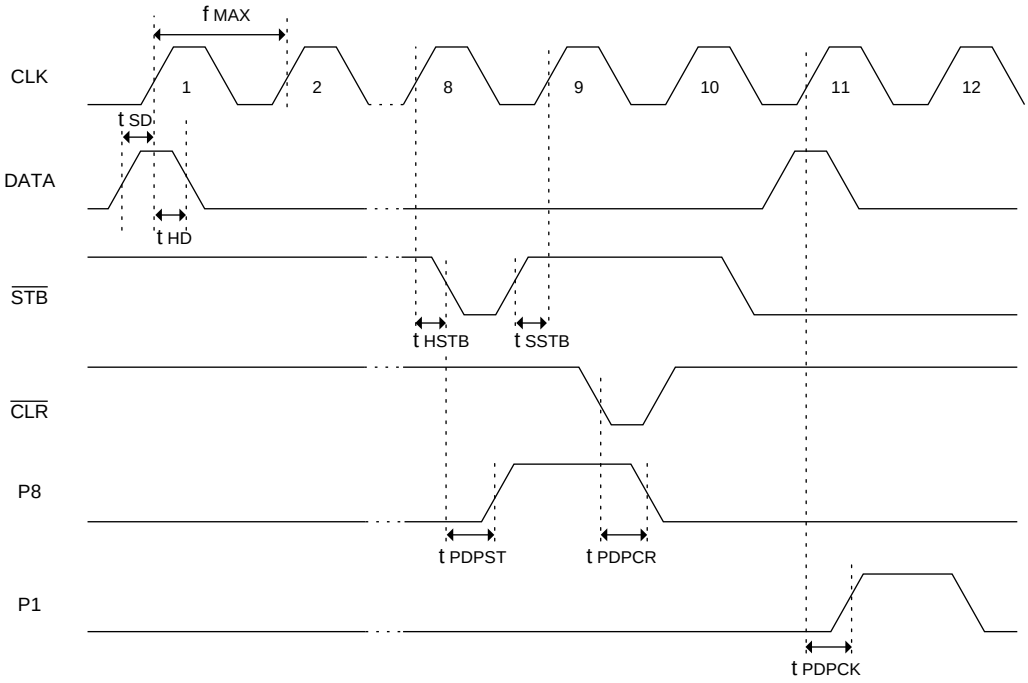
●Electrical characteristics (unless otherwise noted, V_{DD} = 4.5V ~ 5.5V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	I_{DD}	—	—	0.1	mA	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
Input high level voltage	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V	—
Input low level voltage	V_{IL}	V_{SS}	—	$0.3V_{DD}$	V	—
Input leak current	I_{LI}	– 10	—	10	μA	$V_1 = 0 \sim V_{DD}$
Output high level voltage	V_{OHD}	V_{DD} – 1.5	—	V_{DD}	V	I_{OH} = – 25mA
		V_{DD} – 1.0	—	V_{DD}	V	I_{OH} = – 15mA
		V_{DD} – 0.5	—	V_{DD}	V	I_{OH} = – 10mA
Output low level voltage	V_{OLD}	V_{SS}	—	1.5	V	I_{OL} = + 25mA
		V_{SS}	—	0.8	V	I_{OL} = + 15mA
		V_{SS}	—	0.4	V	I_{OL} = + 10mA

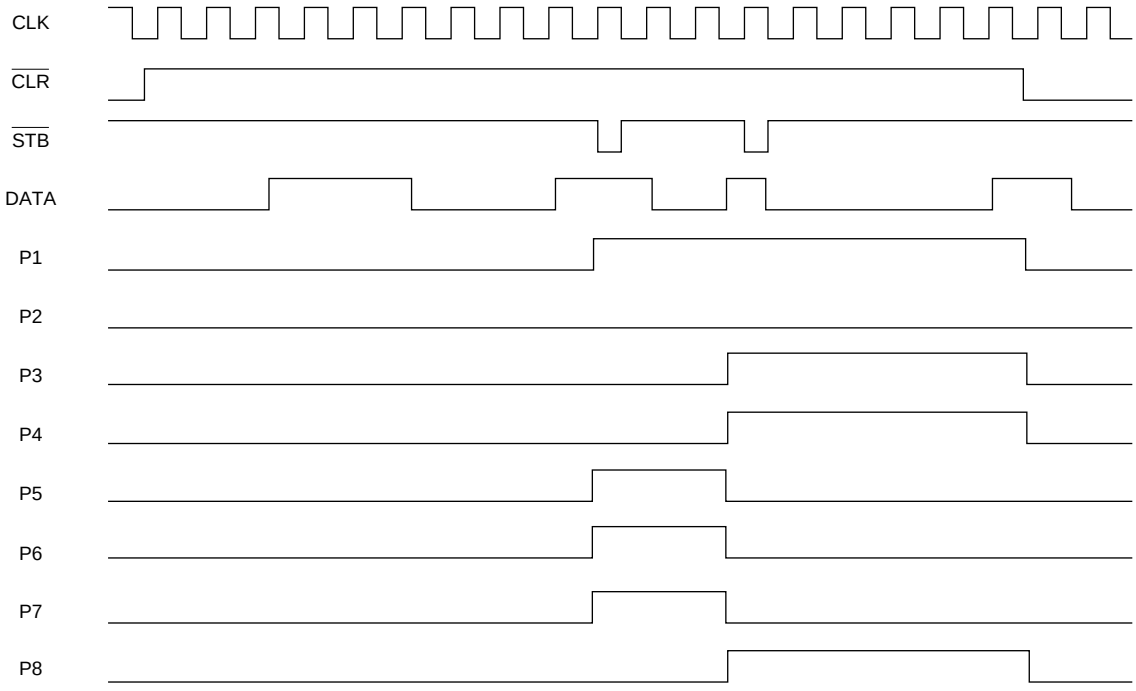
●Switching characteristics (unless otherwise noted, V_{DD} = 4.5V ~ 5.5V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Setup time (DATA-CLK)	t_{SD}	20	—	—	ns	—
Hold time (DATA-CLK)	t_{HD}	20	—	—	ns	—
Setup time ($\overline{STB}$-CLK)	t_{SSTB}	30	—	—	ns	—
Hold time ($\overline{STB}$-CLK)	t_{HSTB}	30	—	—	ns	—
Transmission delay time (CLK-P1 ~ P8)	t_{PDPCK}	—	—	100	ns	—
Transmission delay time ($\overline{STB}$-P1 ~ P8)	t_{PDPSTB}	—	—	80	ns	—
Transmission delay time ($\overline{CLR}$-P1 ~ P8)	t_{PDPCLR}	—	—	80	ns	—
Max. operating frequency	f_{MAX}	5	—	—	MHz	—

●Switching characteristics



●Timing chart



●Circuit operation

This IC is made up of an 8-bit shift register, a latch, and an output driver.

The four input pins (data (DATA), strobe ($\overline{STB}$), latch reset ($\overline{CLR}$), and ckock (CLK)) are all hysteresis inputs (0.5V Typ.).

The reset function applies to all bits in the latch circuit. When $\overline{CLR}$ is low, the latch circuit is reset asynchronously, regardless of the other inputs, and all outputs are set to low. The $\overline{CLR}$ pin is normally high.

The serial data input to the data pin is synchronously read into the shift register on the rising edge of the clock.

When $\overline{STB}$ is low ($\overline{CLR}$ is high), the data in the shift register is transferred to the latch circuit, and output on the parallel data output pins (P1 ~ P8).

When $\overline{STB}$ is high, the latch circuit and output data does not change.

●Electrical characteristic curves

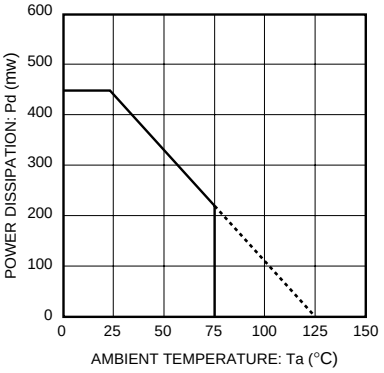


Fig. 1 Thermal derating characteristics

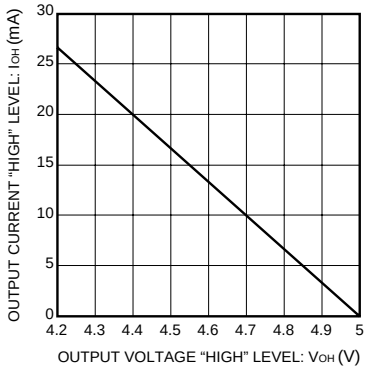


Fig. 2 Output high level current vs. output high level voltage

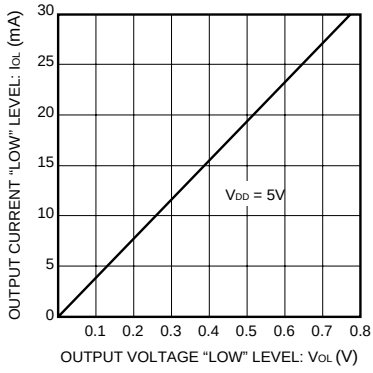
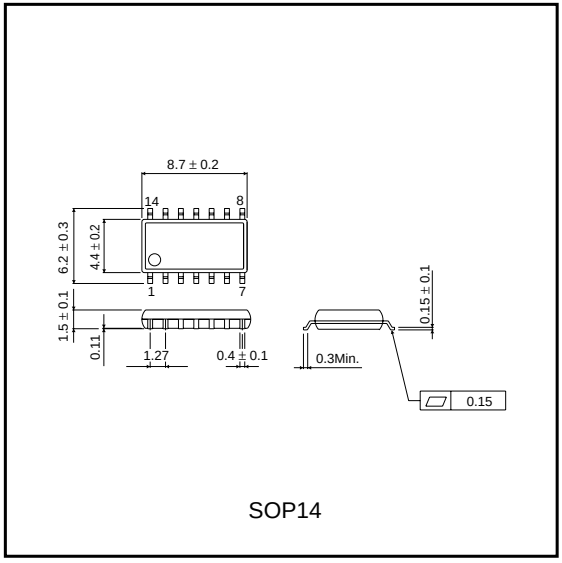


Fig. 3 Output low level current vs. output low level voltage

●External dimensions (Units: mm)



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