System control servo
BU38603 / BU38703 / BU38803

The BU38603, BU38703 and BU38803 are servo controller ICs for VCRs. They contain a high-speed, 8-bit CPU and perform the processing required for the drum, capstan, FV and PV completely in software, allowing a large reduction in the number of external components required. They also contain high-performance linear amplifiers, eliminating the need for interface ICs. Specialized hardware is included for items that require high-speed processing, to allow efficient utilization of the CPU.

●Applications
VHS VCRs and camcorders

●Features
1) CPU
   499 commands (69 types)
   Memory-mapped I / O
   Minimum command execution time: 250ns (8MHz)
2) ROM capacity
                  BU38603: 16384 × 8 bit
                  BU38703: 24576 × 8 bit
                  BU38803: 32768 × 8 bit
3) RAM capacity: 512 × 8bit
4) Interrupt
   Pattern generator: 1
   Watch-dog timer: 1
   External interrupts: 1
   FG interrupts: 5
   Internal interrupts: 7
   Two timers, serial transmission, interrupt, VHSW,
   CTL interval timer (fixed) / VISS
   ∗ Multi-layer interrupts possible.
5) Free-running counter: 19 bit
6) PWM output: 12 bit × 2
7) Pattern generator
   17 bits from FRC MSB used.
   Output
                  Internal: 3 bit
                  External (PO): 5 bit
                  External (PIO): 6 bit
8) Programmable pre-scaler
                  CFG: 7 bit
                  CTL: 6 bit

9) Head amplifier / chroma rotary
    Generated from pattern generator output.
10) Built-in AGC. Five-bits used to switch the gain
    control registers for the CTL amplifier.
11) CTL counter: 1 / 30 or 1 / 25
12) Data shift PLL calculation: 24 bit
13) Timer: 8 bit × 2
14) Synchronous serial input/output: 8 bit × 1
15) VH PULSE
                  V separeted from composite synchronous snal.
                  Pseudo V generated from pattern generator
                  output.
                  Superimposed pseudo H synchronized with
                  the composite synchronous signal.
16) VISS / VASS
                  VASS 0 / 1 discrimination
                  VISS discrimination threshold: 3
                  Aspect discrimination.
                  D / A CTL switching.
17) Standard I / O
                  Parallel I / O (PIO): 32 bit
                  Parallel output (PO): 6 bit
18) A / D converter: 8 bits × 8 channels
    Can be masked-programmed to be parallel inputs.
19) Watch-dog timer
                  Setting period: 4
20) Linear circuits
                  DFG: amplifier / comparator
                  CFG: amplifier / comparator
                  CTL: differential amplifier / comparator
                  DPG: comparator

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}, V_{DDA}, V_{DAD}	0.3 ~ 7.0[*2]	V
Pin applied voltage	V_{IN}	$V_{SS} - 0.3$ ~ $V_{DD} + 0.3$	V
Power dissipation	Pd	500[*1]	mW
Storage temperature	Tstg	− 55 ~ + 125	°C

*1 Reduced by 5mW for each increase in Ta of 1°C over 25°C.
*2 Use with $V_{SS} = V_{SSA} = V_{SAD}$, and $V_{DD} = V_{DDA} = V_{DAD}$.

● Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}, V_{DDA}, V_{DDB}	4.5 ~ 5.5	V
Clock frequency	F_{CK}	8	MHz
Operating temperature	Topr	− 25 ~ + 75	°C

● Block diagram
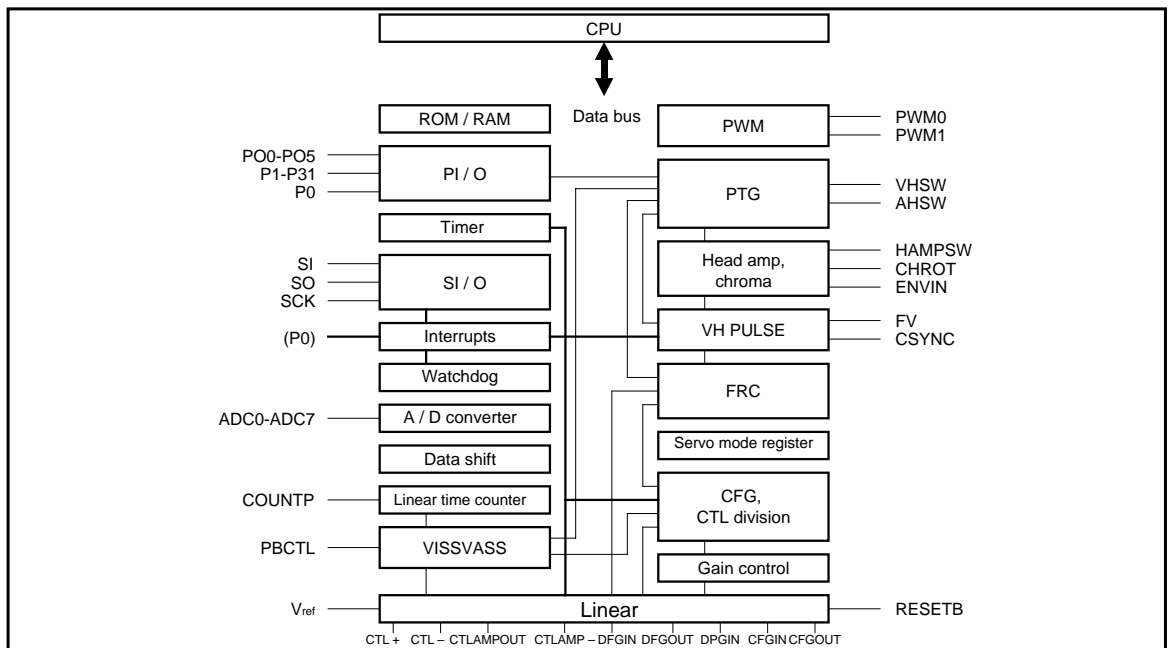
●Pin descriptions

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	VSAD	A / D convertor circuit GND.	41	CHROT	Chroma rotary switch output
2	ADC0		42	FV	Pseudo Vsync output
3	ADC1		43	V_{DD}	Logic circuit power supply
4	ADC2	Can be optionally mask – programmed	44	PWM0	PWM output
5	ADC3	to be either A / D or parallel inputs.	45	PWM1	
6	ADC4		46	P21	
7	ADC5		47	P20	
8	ADC6		48	P19	
9	ADC7		49	P18	
10	VDAD	A / D convertor circuit power supply.	50	P17	
11	DFGOUT	Drum FG amplifier output	51	P16	Parallel I / O
12	DFGIN	Drum FG amplifier input	52	P15	
13	DPGIN	Drum PG comparator input	53	P14	
14	CFGIN	Capstan FG amplifier input	54	P13	
15	CFGOUT	Capstan FG amplifier output	55	P12	
16	VSSA	Linear circuit GND	56	P11	
17	V_{ref}	Internal BIAS and power-on reset pin	57	P10	
18	CTLAMP –	CTL amplifier – input	58	P9	
19	CTLAMPOUT	CTL amplifier output	59	PO2	
20	CTL –	CTL coil – connection	60	PO1	Parallel output
21	CTL +	CTL coil + connection	61	PO0	
22	VDDA	Linear circuit power supply	62	CLOCKO	For connection of oscillator
23	RESETB	Power supply reset	63	CLOCKI	
24	TEST	Test mode input (normally GND)	64	V_{SS}	Logic circuit GND
25	PO5	Parallel output	65	P8	
26	PO4		66	P7	
27	P31		67	P6	
28	P30	Parallel I / O	68	P5	
29	P29		69	P4	Parallel I / O
30	P28		70	P3	
31	P27		71	P2	
32	P26		72	P1	
33	P25	Parallel I / O and pattern generator output	73	P0	Parallel I / O and external interrupt
34	P24		74	SI	Serial I / O data input
35	P23		75	SO	Serial I / O data I / O
36	P22		76	SCK	Serial I / O clock I / O
37	PO3	Parallel output and pattern generator output	77	ENVIN	Envelope detector logic input
38	VHSW	Pattern generator VHSW output	78	CSYNC	Composite signal logic input
39	AHSW	Pattern generator AHSW output	79	COUNTP	CTL counter pulse output
40	HAMPSW	Head amplifier switch output	80	PBCTL	CTL logic output

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5V and f_{OSC} = 8MHz)

| Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
[Logic block] (Logic: pins 24 to 80)							
Operating supply current	I_{DD}	—	12	19	mA	No load, when reset	Fig.1
⟨Logic I / O⟩							
Output high level voltage	V_H	4.0	4.5	—	V	I = 2mA: except pins 66 to 73 I = 1mA: 66 to 73pin	Fig.2
Output low level voltage	V_L	—	0.5	1.0	V	I = 2mA	Fig.2
Max. output low level current	I_{LL}	10.0	16.0	—	mA	66 to 73pin	Fig.2
Input high level voltage	V_{IH}	4.0	—	—	V		Fig.2
Input low level voltage	V_{IL}	—	—	1.0	V		Fig.2
Input high level current	I_H	—	0	1.0	μA	$V_{IN} = V_{DD}$	Fig.2
Input low level current	I_L	− 1.0	0	—	μA	$V_{IN} = 0$	Fig.2
⟨Serial I / O⟩							
Input data hold	T_{SH}	0.16	—	—	μs		—
Input data setup	T_{SS}	0.16	—	—	μs		—
Output data delay	T_D	—	—	0.3	μs	Between CLOCK and DATA	—
[Linear block] (Linear: pins 11 to 23)							
Operating supply current	I_{LI}	—	10	26	mA	No load	Fig.1
[A / D block] (A / D: pins 1 to 10)							
Operating supply current	I_{AD}	—	0.6	2.0	mA		Fig.1
Linearity error	E_L	− 3	0	3	LSB		Fig.3
Input high level voltage	V_{ADPH}	4.0	—	—	V	When P input selected	Fig.3
Input low level voltage	V_{ADPL}	—	—	1.0	V	When P input selected	Fig.3
Input high level current	I_{ADPH}	—	0	1.0	μA	When P input selected, $V_{IN} = V_{DD}$	Fig.3
Input low level current	I_{ADPL}	− 1.0	0	—	μA	When P input selected, $V_{IN} = 0$	Fig.3

ROHM

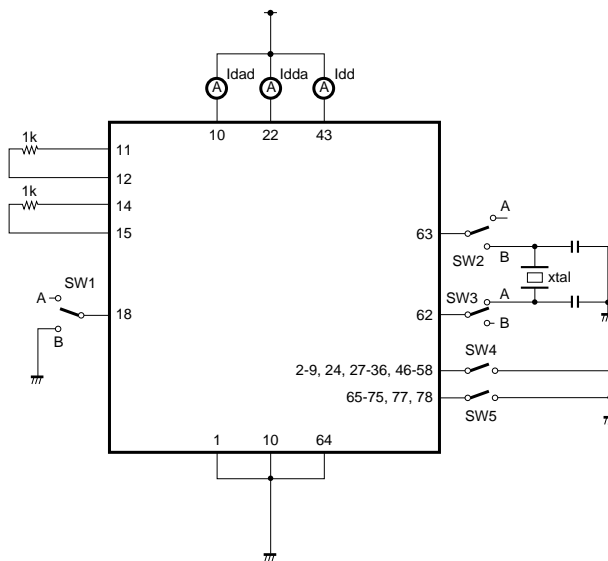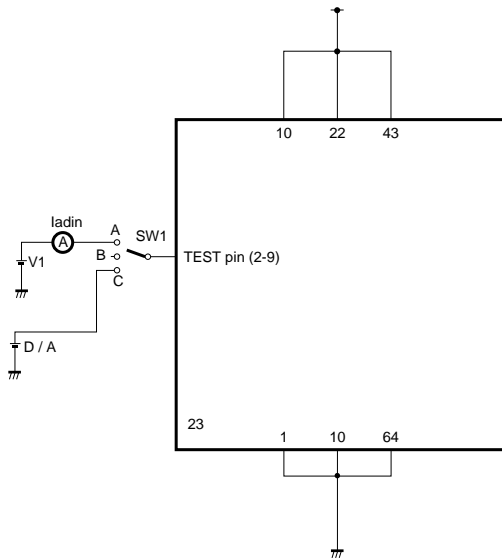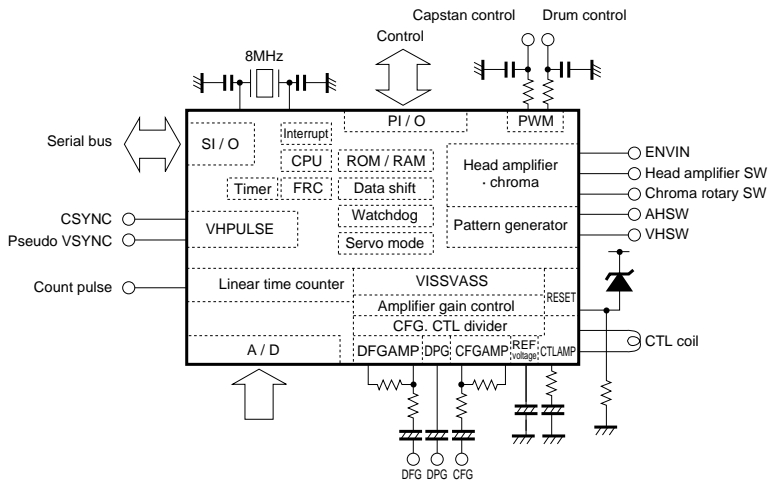●Measurement circuits
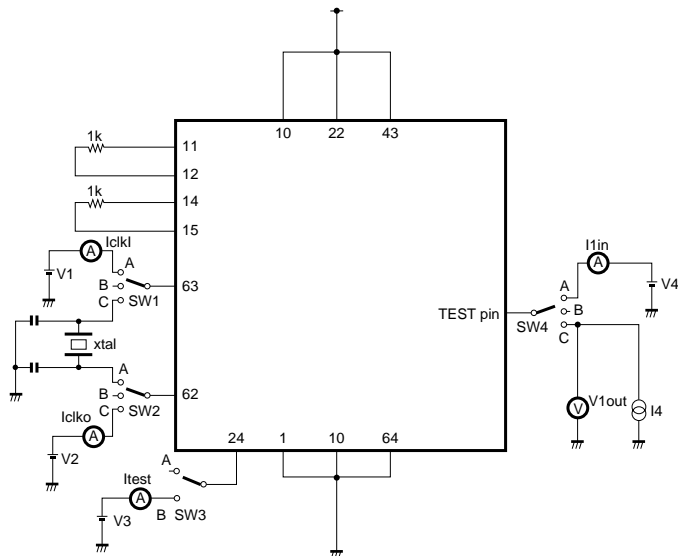
Fig.1

Fig.2

Fig.3

●Application example

Fig.4

ROHM

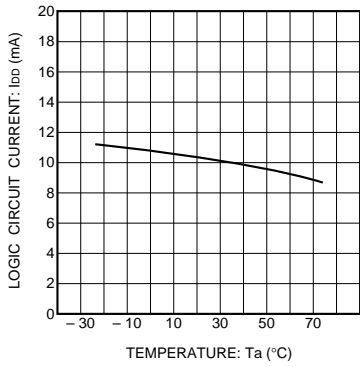● Electrical characteristic curves

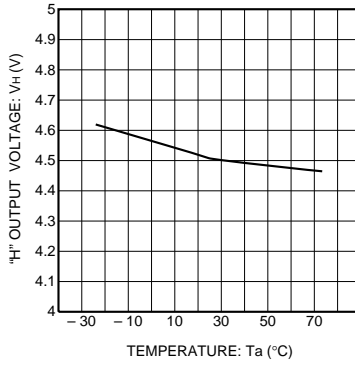Fig. 5 Logic circuit current.

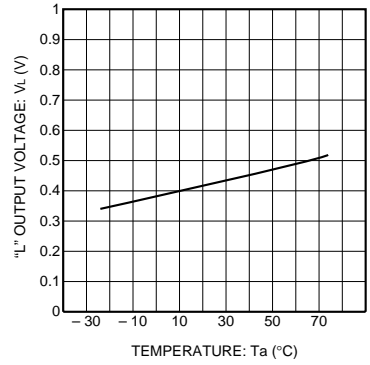Fig. 6 Logic "H" output voltage.
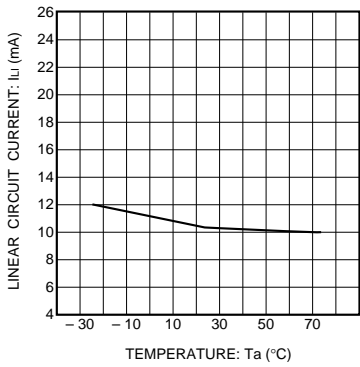
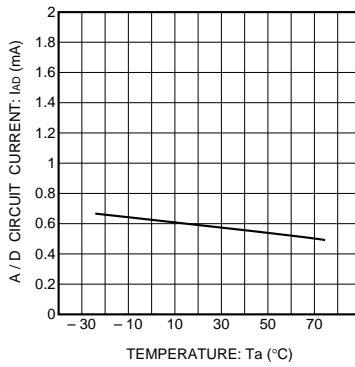Fig. 7 Logic "L" output voltage.

Fig. 8 Linear circuit current.

Fig. 9 A / D circuit current.

● External dimensions (Units: mm)

QFP80