

Digital transistors (built-in resistors)

DTC113ZUA / DTC113ZKA / DTC113ZSA

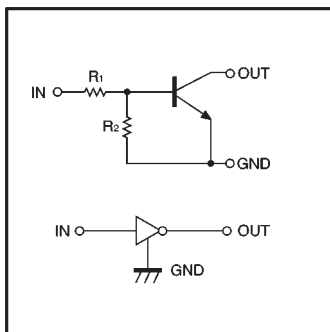
●Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) Each bias resistor is a thin-film resistor. Since they are completely insulated, the input can be negatively biased. The insulation also eliminates most of the parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making device design easy.

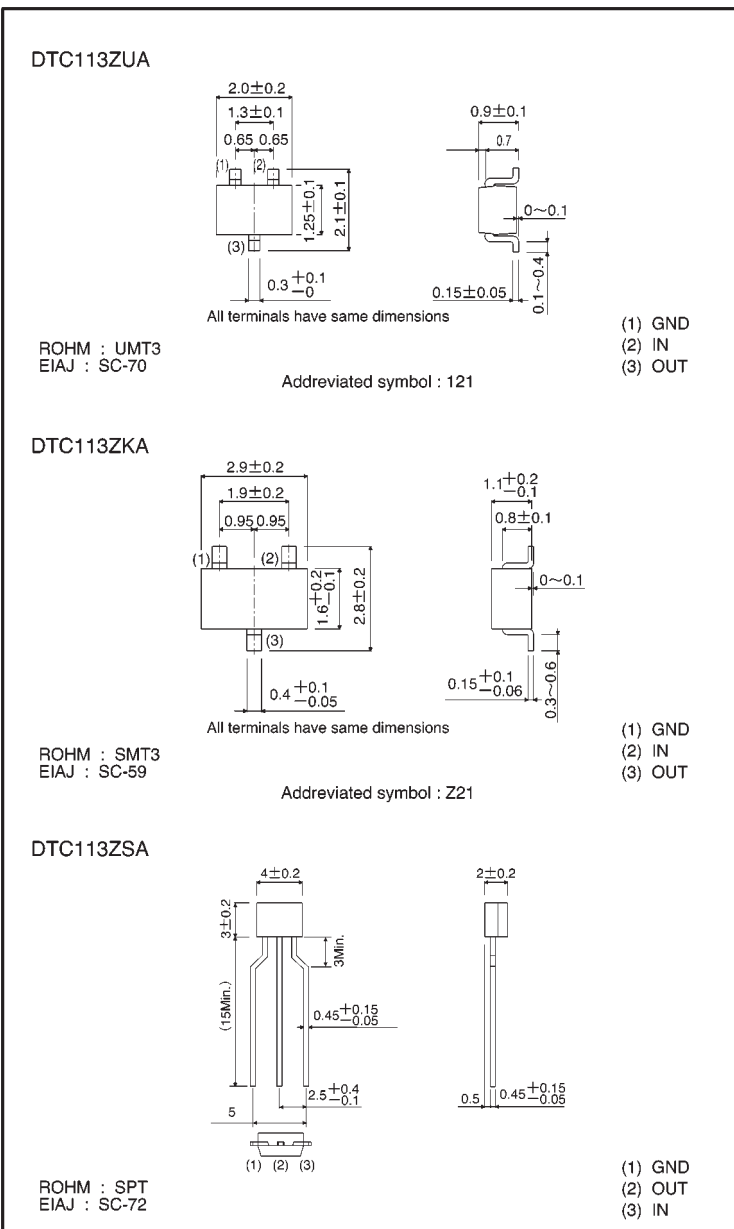
●Structure

NPN digital transistor
(with built in resistors)

●Equivalent circuit



●External dimensions (Units: mm)



● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits(DTC113Z□)			Unit
		UA	KA	SA	
Supply voltage	V _{CC}	50			V
Input voltage	V _{IN}	-5~+10			V
Output current	I _o	100			mA
	I _{c(Max.)}	100			
Power dissipation	P _d	200	300		mW
Junction temperature	T _j	150			°C
Storage temperature	T _{stg}	-55~+150			°C

● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input voltage	V _{I(off)}	—	—	0.3	V	V _{CC} =5V, I _o =100 μA
	V _{I(on)}	3	—	—		V _o =0.3V, I _o =20mA
Output voltage	V _{O(on)}	—	0.1	0.3	V	I _o /I _i =10mA/0.5mA
Input current	I _i	—	—	7.2	mA	V _i =5V
Output current	I _{o(off)}	—	—	0.5	μA	V _{CC} =50V, V _i =0V
DC current gain	G _i	33	—	—	—	V _o =5V, I _o =5mA
Input resistance	R _i	0.7	1	1.3	kΩ	—
Resistance ratio	R _z /R _i	8	10	12	—	—
Transition frequency	f _t	—	250	—	MHz	V _{CE} =10V, I _E =-5mA, f=100MHz *

* Transition frequency of the device

● Packaging specifications

Part No.	Package	EMT3	UMT3	SMT3	SPT
	Packaging type	Taping	Taping	Taping	Taping
	Code	TL	T106	T146	TP
	Basic ordering unit (pieces)	3000	3000	3000	5000
DTC113ZUA	—	○	—	—	
DTC113ZKA	—	—	○	—	
DTC113ZSA	—	—	—	○	

●Electrical characteristic curves

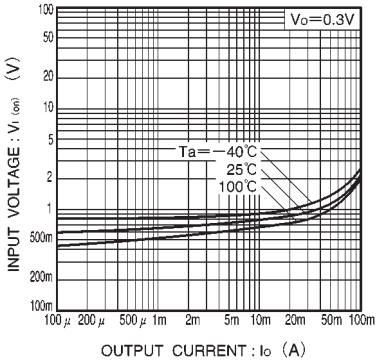


Fig.1 Input voltage vs. output current (ON characteristics)

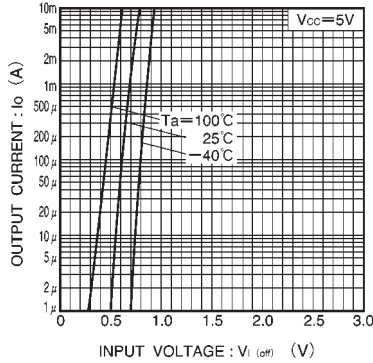


Fig.2 Output current vs. input voltage (OFF characteristics)

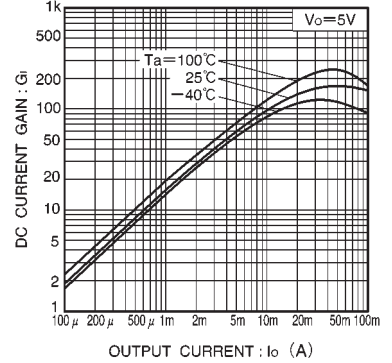


Fig.3 DC current gain vs. output current

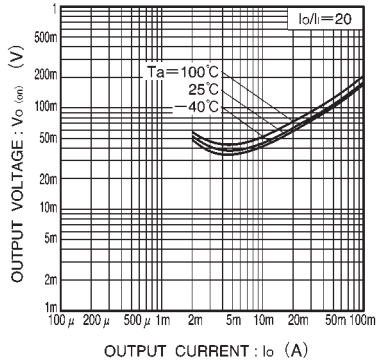


Fig.4 Output voltage vs. output current