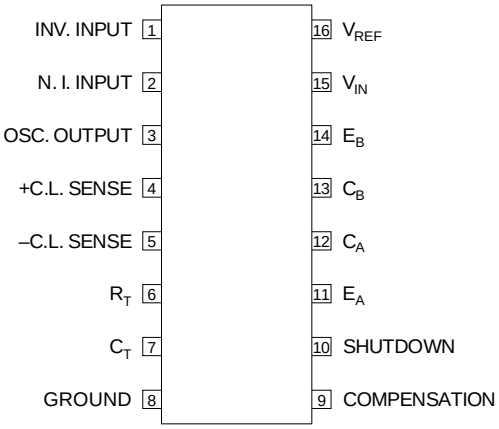
IP1524B SERIES

REGULATING PULSE WIDTH MODULATORS

TOP VIEW



J Package – 16 Pin Ceramic DIP
N Package – 16 Pin Plastic DIP
D Package – 16 Pin Plastic (300) SOIC

FEATURES

- **Pin Compatible with IP1524 Series**
- **7 to 40 volt operation**
- **5 volt reference trimmed to ±1%**
- **Undervoltage lockout**
- **Excellent external sync capability**
- **Wide current limit common mode range**
- **+5 Volt error amplifier common mode**
- **PWM data latch**
- **Full double-pulse suppression logic**
- **50ns shutdown function**
- **Dual 200mA, 60V output transistors**
- **Fully specified over temperature**

Order Information

Part Number	J–Pack 16 Pin	N–Pack 16 Pin	D–16 16 Pin	Temp. Range
IP1524B	✔			-55 to +125°C
IP2524B	✔	✔	✔	-25 to +85°C
IP3524B	✔	✔	✔	0 to +70°C

Note:
To order, add the package identifier to the part number.
eg. IP1524BJ
IP3524BD–16

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

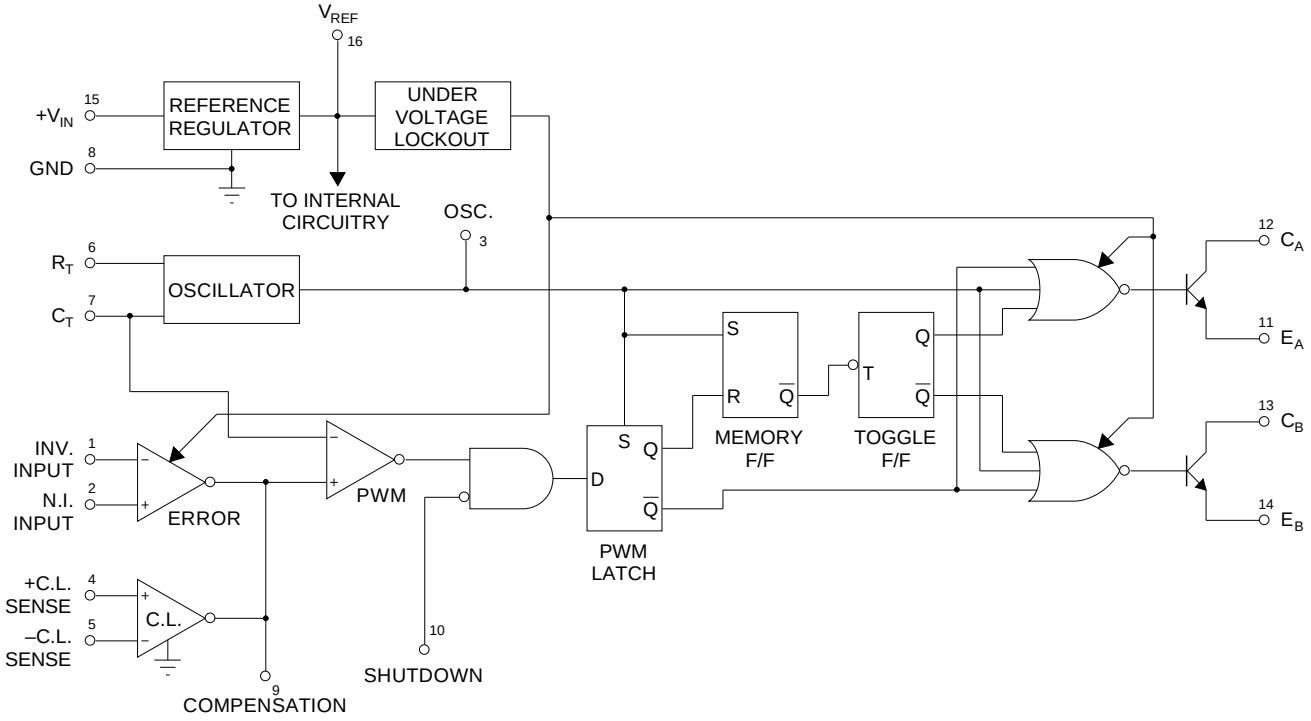
$+V_{IN}$	Input Voltage		+40V
	Collector Voltage		+60V
	Logic Inputs		–0.3 to +5.5V
	Current Limit Sense Inputs		–0.3 to $+V_{IN}$
	Oscillator Charging Current		5mA
P_D	Power Dissipation	T_A = 25°C	1W
		Derate @ T_A > 50°C	10mW/°C
P_D	Power Dissipation	T_C = 25°C	2W
		Derate @ T_C > 25°C	16mW/°C
T_J	Operating Junction Temperature		See Ordering Information
T_{STG}	Storage Temperature Range		–65 to +150°C
T_L	Lead Temperature	(soldering, 10 seconds)	+300°C

IP1524B SERIES

DESCRIPTION

The IP1524B is a pulse width modulator for switching power supplies which features improved performance over industry standards like the SG1524. A direct pin-for-pin replacement for the earlier device, it combines advanced processing techniques and circuit design to provide improved reference accuracy/ and extended common mode range at the error amplifier and current limit inputs. A DC-coupled flip-flop eliminates triggering and glitch problems, and a PWM data latch prevents edge oscillations. The circuit incorporates true digital shutdown for high speed response, while an undervoltage lockout circuit prevents spurious outputs when the supply voltage is too low for stable operation. Full double-pulse suppression logic insures alternating output pulses when the shutdown pin is used for pulse-by-pulse current limiting.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{IN}	Input Voltage		+7 to +40V
	Collector Voltage		0 to +60V
	Error Amp Common Mode Range		+2.3 to V_{REF}
	Current Limit Sense Common Mode Range		0 to V_{IN} – 2.5V
	Output Current	(each transistor)	0 to 200mA
	Reference Load Current		0 to 20mA
	Oscillator Charging Current		25µA to 1.8mA
	Oscillator Frequency Range		50Hz to 500kHz
R_T	Oscillator Timing Resistor		2kΩ to 150kΩ
C_T	Oscillator Timing Capacitor		1nF to 0.1µF
	Operating Ambient Temperature Range	IP1524B	–55 to +125°C
		IP2524B	–25 to +85°C
		IP3524B	0 to +70°C

ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions [1]	IP1524B IP2524B			IP3524B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	TURN–ON CHARACTERISTICS							
V_{IN} Undervoltage Threshold	V_{IN} Rising	4.3	5.2	6.5	4.3	5.2	6.5	V
Turn–on Hysteresis		0.1	0.3	0.6	0.1	0.3	0.6	mA
Operating Current	V_{IN} = 7 to 40V		7	10		7	10	
	REFERENCE SECTION							
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	V_{IN} = 7 to 40V I_L = 0 to 20mA	4.90		5.10	4.85		5.15	
Line Regulation	V_{IN} = 7 to 40V		1	10		1	15	mV
Load Regulation	I_L = 0 to 20mA		5	15		5	25	
Temperature Stability			40	75		40	75	
Short Circuit Current	V_{REF} = 0	25	70	120	25	70	120	mA
Long Term Stability	T_J = 25°C		1	10		1		mV/khr
	OSCILLATOR SECTION [2]							
Initial Accuracy	T_J = 25°C	41	43	45	39	43	47	kHz
Voltage Stability	V_{IN} = 7 to 40V		0.1	1		0.1	1	%
Temperature Stability			1	2		1	2	
Minimum Frequency	R_T = 150kΩ C_T = 0.1µF		80	140		80	140	Hz
Maximum Frequency	R_T = 2kΩ C_T = 470pF	400	700		400	700		kHz
Clock Amplitude	Output, Pin 3 C_T = 0.01µF	3.0	4.0		3.0	4.0		V
Clock Pulse Width	Output, Pin 3 C_T = 0.01µF	0.4	0.5	1.2	0.4	0.5	1.2	µs
Sawtooth Peak Voltage	C_T = 0.01µF		3.7	4.0		3.7	4.0	V
Sawtooth Valley Voltage	C_T = 0.01µF	0.6	1	1.1	0.6	1	1.1	
Sawtooth Valley T.C.	T_J = 25°C		-1			-1		mV/°C
	ERROR AMP SECTION							
Input Offset Voltage	V_{CM} = 2.3 to V_{REF}		0.1	5		2	10	mV
Input Bias Current	V_{CM} = 2.3 to V_{REF}		1	5		1	10	µA
Input Offset Current	V_{CM} = 2.3 to V_{REF}		0.1	1		0.1	1	

NOTES

1. Test Conditions unless otherwise stated:
   V_{IN} = 20V , I_{REF} = 0.
   T_J = –55 to +125°C for IP1524B
   T_J = –25 to +85°C for IP2524B
   T_J = 0 to +70°C for IP3524B
2. R_T = 2.7KΩ , C_T = 0.01µF unless otherwise stated.

ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

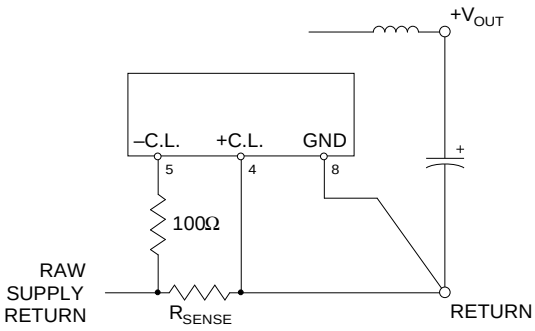
Parameter	Test Conditions [1]	IP1524B IP2524B			IP3524B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	ERROR AMP SECTION (cont.)							
DC Open Loop Gain	ΔV_O = 1 to 3V $R_L \geq 10M\Omega$	60	75		60	75		dB
Common Mode Rejection	V_{CM} = 2.3 to V_{REF}	70	90		70	90		
Supply Voltage Rejection	V_{IN} = 7 to 40V	76	120		76	120		
Output Low Level	I_{SINK} = 100µA		0.2	0.5		0.2	0.5	V
Output High Level	I_{SOURCE} = 100µA	3.8	4.2		3.8	4.2		
Gain Bandwidth Product	T_J = 25°C	1	2		1	2		MHz
	PWM COMPARATOR							
Minimum Duty Cycle	$V_{PIN1} - V_{PIN2} \geq 150mV$			0			0	%
Maximum Duty Cycle	$V_{PIN2} - V_{PIN1} \geq 150mV$	45	49		45	49		
	CURRENT LIMIT AMPLIFIER							
Sense Voltage	V_{CM} = 0 to 17.5V V_{IN} = 7 to 40V	180	200	220	180	200	220	mV
Input Bias Current	V_{CM} = 0 to 17.5V V_{IN} = 7 to 40V		-1	-10		-1	-10	µA
	SHUTDOWN INPUT							
High Input Voltage		2.0			2.0			V
High Input Current	$V_{SHUTDOWN}$ = 5V		0.1	1		0.1	1	mA
Low Input Voltage				0.6			0.6	V
Shutdown Delay	Pin 10 to output T_J = 25°C		50			50		ns
	OUTPUT SECTION (each transistor)							
Collector Leakage Current	V_{CE} = 60V		0.1	20		0.1	20	µA
Collector Saturation Voltage	I_C = 20mA		0.2	0.4		0.2	0.4	V
	I_C = 200mA		1.0	2.2		1.0	2.2	
Emitter Output Voltage	I_E = 50mA	17	19		17	19		V
	I_E = 200mA	16.5	18		16.5	18		
Emitter Voltage Rise Time	R_E = 2kΩ T_J = 25°C		0.2	0.4		0.2		µs
Collector Voltage Fall Time	R_C = 2kΩ T_J = 25°C		0.1	0.2		0.1		

NOTES

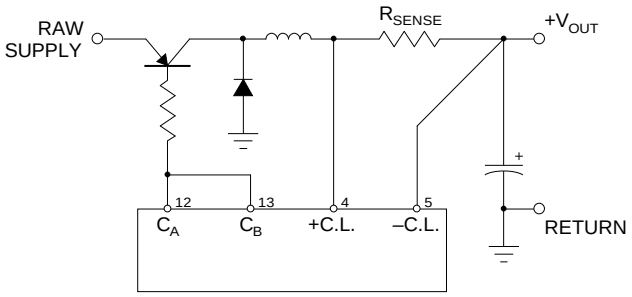
1. Test Conditions unless otherwise stated:
   V_{IN} = 20V , I_{REF} = 0.
   T_J = –55 to +125°C for IP1524B
   T_J = –25 to +85°C for IP2524B
   T_J = 0 to +70°C for IP3524B

APPLICATIONS INFORMATION

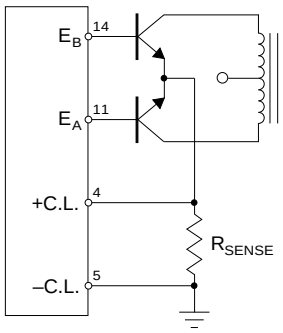
Current Sensing in the Ground Line



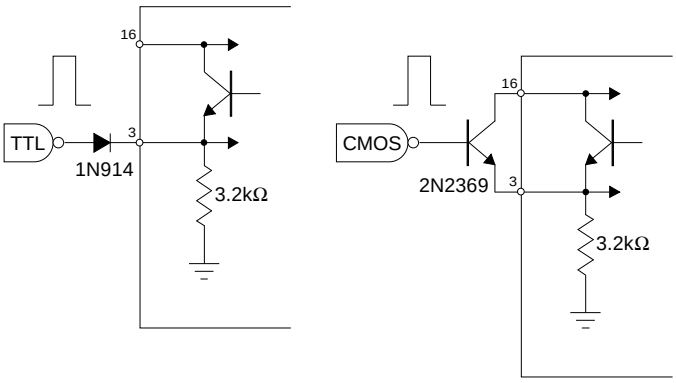
Current Sensing in the Output Line



Sensing Primary Current with an Emitter Resistor



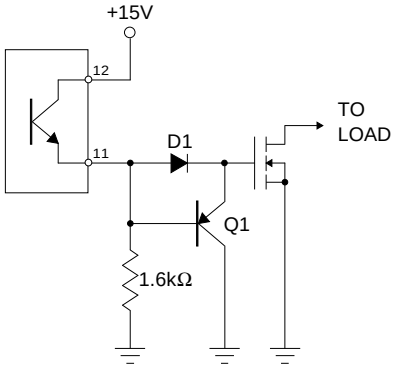
Oscillator Sync to an External Clock



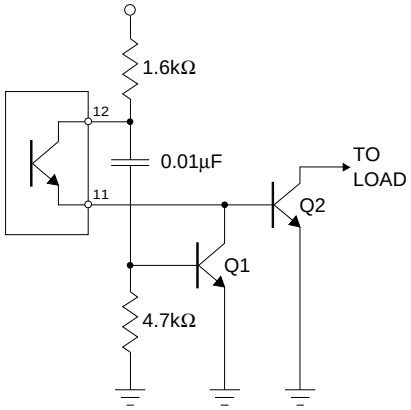
A. TTL Logic

B. 5 Volt CMOS Logic

Driving Power MOSFETs

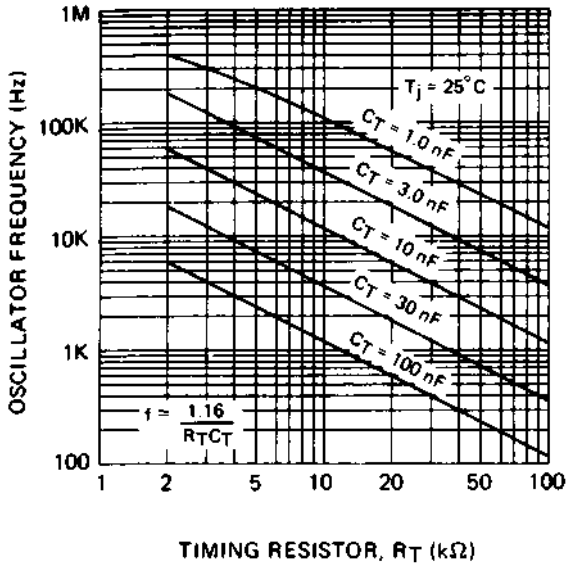


Driving Power Bipolar Transistors

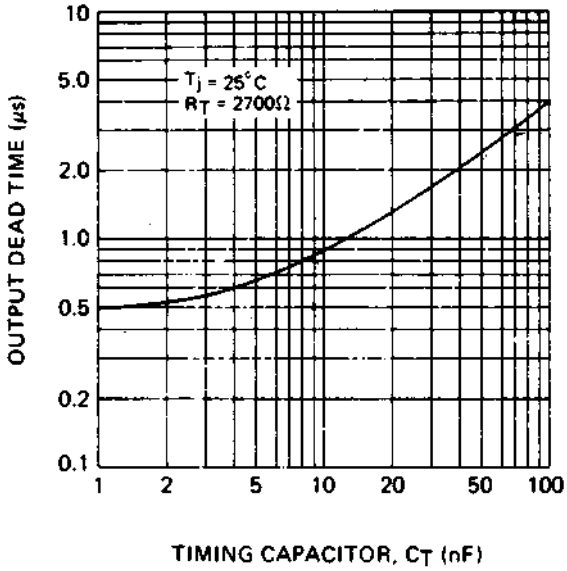


TYPICAL PERFORMANCE CHARACTERISTICS

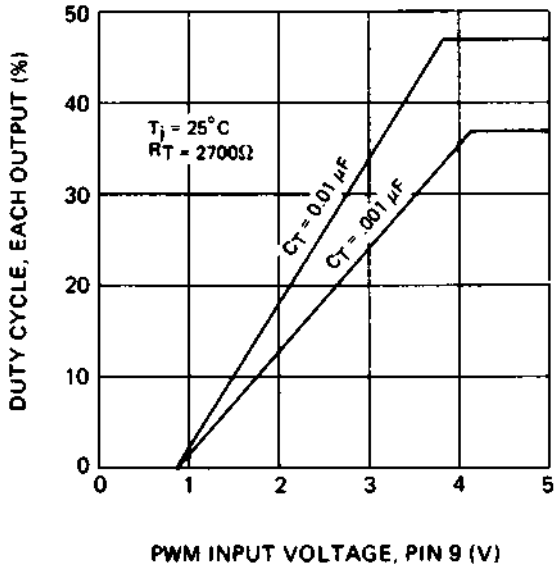
Oscillator Frequency vs. Timing Components



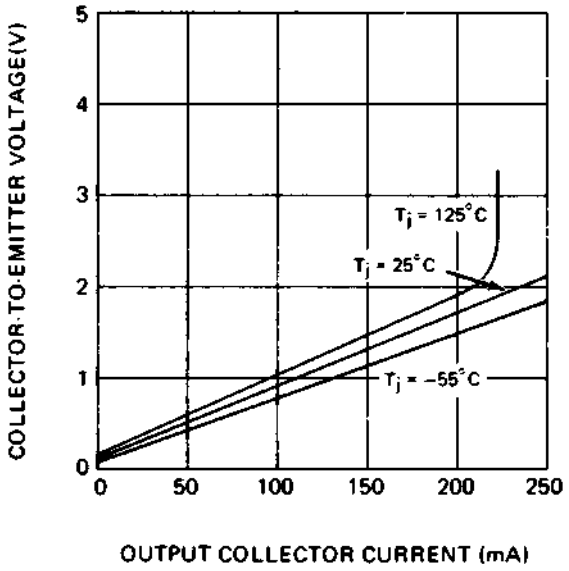
Output Dead Time vs. Timing Capacitance Value



Pulse Width Modulation Transfer Function

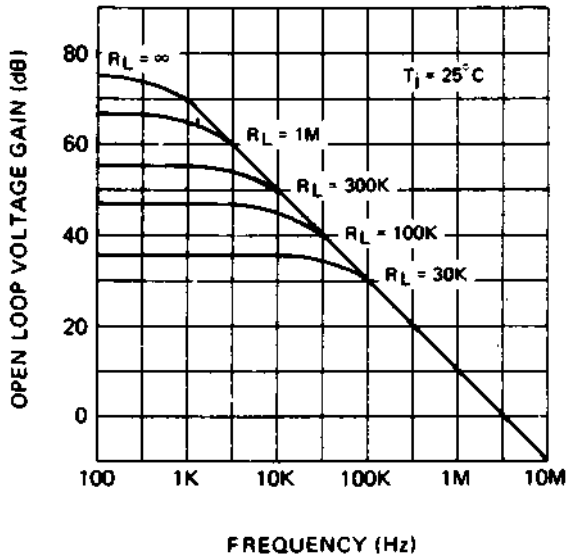


Output Saturation Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Error Amplifier Voltage Gain vs. Frequency



Undervoltage Lockout Characteristics