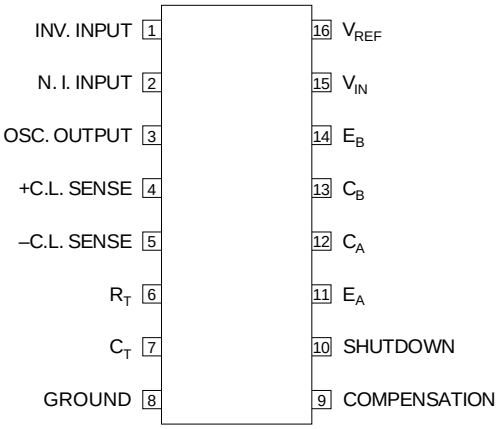
IP1524 SERIES

TOP VIEW



J Package – 16 Pin Ceramic DIP
N Package – 16 Pin Plastic DIP
D Package – 16 Pin Plastic (150) SOIC

REGULATING PULSE WIDTH MODULATORS

FEATURES

- **Guaranteed ±2% reference voltage tolerance**
- **Guaranteed ±6% oscillator tolerance**
- **Fully specified temperature performance**
- **Guaranteed 10mV/1000 hours long term stability**
- **Interchangeable with SG1524 series**

Order Information

Part Number	J–Pack 16 Pin	N–Pack 16 Pin	D–16 16 Pin	Temp. Range
IP1524	✔			-55 to +125°C
IP2524	✔	✔	✔	-25 to +85°C
IP3524	✔	✔	✔	0 to +70°C

Note:
To order, add the package identifier to the part number.
eg. IP1524J
IP3524D–16

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

$+V_{IN}$	Input Voltage		+40V
	Collector Voltage		+40V
	Output Current	(each transistor)	100mA
	Reference Load Current		Internally Limited
	Oscillator Charging Current		5mA
	Shut Down Pin Voltage		+5.5V
	Current Limit Sense Common Mode Range		–1.0 to +1.0V
P_D	Power Dissipation	T_A = 25°C	1W
		Derate @ T_A > 50°C	10mW/°C
P_D	Power Dissipation	T_C = 25°C	2W
		Derate @ T_C > 25°C	16mW/°C
T_J	Operating Junction Temperature		See Ordering Information
T_{STG}	Storage Temperature Range		–65 to +150°C
T_L	Lead Temperature	(soldering, 10 seconds)	+300°C

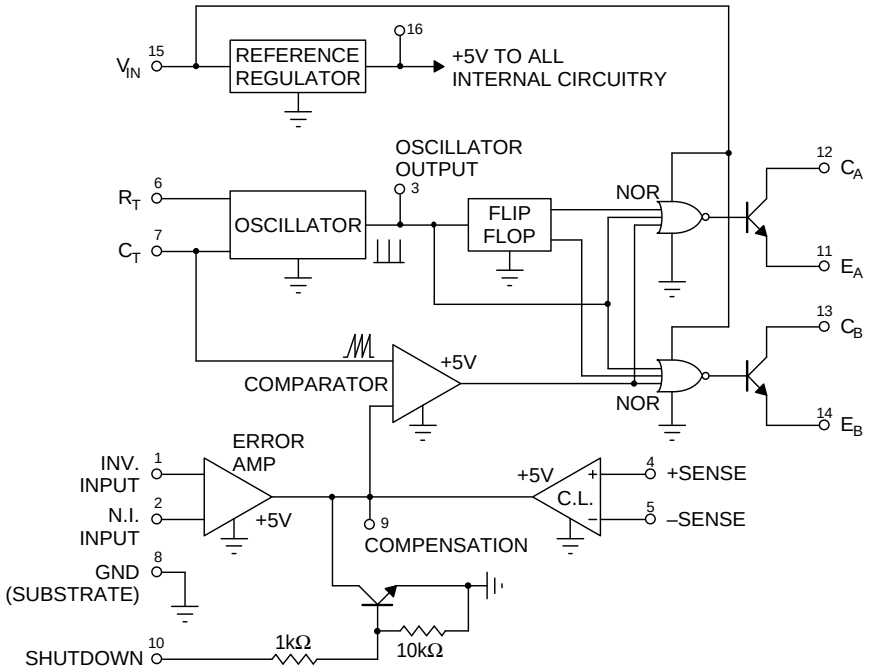
IP1524 SERIES

DESCRIPTION

The IP1524 series of PWM switching regulator control circuits contains all the functions required to implement single-ended or push-pull switching regulators. Included are voltage reference, error amplifer, oscillator, PWM comparator, output drivers, current limiting and shutdown circuitry.

Although functionally indentical to the SG1524 series, SEMELAB has incorporated several improvements to the IP1524 allowing tighter and more complete specification of electrical performance.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{IN}	Input Voltage		+8 to +40V
	Collector Voltage		0 to +40V
	Error Amp Common Mode Range		+1.8 to +3.4V
	Output Current	(each transistor)	0 to 100mA
	Reference Load Current		0 to 20mA
	Oscillator Charging Current		30µA to 2mA
	Oscillator Frequency Range		50Hz to 500kHz
R_T	Oscillator Timing Resistor		1.8kΩ to 100kΩ
C_T	Oscillator Timing Capacitor		1nF to 0.1µF
T_{AMB}	Operating Ambient Temperature Range	IP1524	–55 to +125°C
		IP2524	-25 to +85°C
		IP3524	0 to +70°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Test Conditions [1]	IP1524 IP2524			IP3524			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	REFERENCE SECTION							
Output Voltage	T_J = Over Temp. Range	4.90	5.00	5.10	4.60	5.00	5.40	V
Line Regulation	$+V_{IN}$ = 8 to 40V T_J = Over Temp. Range		1	10		10	30	mV
Load Regulation	I_L = 0 to 20mA T_J = Over Temp. Range		5	20		20	50	
Ripple Rejection	f = 120Hz		80			66		dB
Short Circuit Current	V_{REF} = 0 T_J = Over Temp. Range	25	50	120		100		mA
Temperature Stability	T_J = Over Temp. Range		0.3	1		0.3	1	%
Long Term Stability	T_J = 125°C		1	10		20		mV/khr
	OSCILLATOR SECTION							
Initial Accuracy	R_T = 2.7kΩ C_T = 0.01µF			6		5		%
Voltage Stability	$+V_{IN}$ = 8 to 40V		0.1	1		0.5	1	
Temperature Stability	T_J = Over Temp. Range		1	2			2	
Minimum Frequency	R_T = 100kΩ C_T = 0.1µF T_J = Over Temp. Range		120	240		120		Hz
Maximum Frequency	R_T = 2kΩ C_T = 0.001µF T_J = Over Temp. Range	200	300			300		kHz
Sawtooth Peak Voltage	C_T = 0.01µF		3.6			3.6		V
Sawtooth Valley Voltage	C_T = 0.01µF	0.6	1			1		
Clock Amplitude	Output, Pin 3 C_T = 0.01µF T_J = Over Temp. Range	3.0	4.0			3.5		V
Clock Pulse Width	Output, Pin 3 C_T = 0.01µF	0.3	0.5	1.0		0.5		µs
	ERROR AMP SECTION [2]							
Input Offset Voltage	T_J = Over Temp. Range		0.1	5		2	10	mV
Input Bias Current	T_J = Over Temp. Range		1	2		1	10	µA
Input Offset Current	T_J = Over Temp. Range			0.5			1	
DC Open Loop Gain	T_J = Over Temp. Range	72	80		60	80		dB
Output Low Level	$V_{PIN1} - V_{PIN2} \geq 150mV$			0.5			0.5	V
Output High Level	$V_{PIN2} - V_{PIN2} \geq 150mV$	3.8			3.8			
Common Mode Rejection		70	90		70			dB
Supply Voltage Rejection	$+V_{IN}$ = 8 to 40V	70	100		70			
Gain Bandwidth Product			3			3		MHz

NOTES

1. Test Conditions unless otherwise stated: V_{IN} = 20V , I_{REF} = 0.
2. V_{CM} = +1.8 to +3.4V
3. V_{CM} = -1 to +1V

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Test Conditions [1]	IP1524 IP2524			IP3524			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
	PWM COMPARATOR							
Minimum Duty Cycle	$V_{PIN1} - V_{PIN2} \geq 150mV$ T_J = Over Temp. Range			0			0	%
Maximum Duty Cycle	$V_{PIN2} - V_{PIN1} \geq 150mV$ T_J = Over Temp. Range	45	49		45	49		%
	CURRENT LIMIT AMPLIFIER [3]							
Sense Voltage	V_{CM} = 0	190	200	210	180	200	220	mV
	V_{CM} = 0 T_J = Over Temp. Range	170	200	230		200		
	SHUTDOWN INPUT							
High Input Voltage	$V_{PIN9} \leq 0.6V$ T_J = Over Temp. Range	1.2			1.2			V
High Input Current	$V_{SHUTDOWN}$ = +5V T_J = Over Temp. Range		4	8		4		mA
Low Input Voltage	$V_{PIN9} \geq 3.5V$ T_J = Over Temp. Range			0.3			0.3	V
	OUTPUT SECTION (each transistor)							
Collector – Emitter Voltage	I_C = 50µA T_J = Over Temp. Range	40			40			V
Collector Leakage Current	V_{CE} = 40V T_J = Over Temp. Range		0.1	50		0.1	50	µA
Collector Saturation Voltage	I_C = 50mA T_J = Over Temp. Range		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V T_J = Over Temp. Range	17	18		17	18		V
Emitter Voltage Rise Time	R_E = 2kΩ		0.2	0.4		0.2		µs
Collector Voltage Fall Time	R_C = 2kΩ		0.1	0.2		0.1		
	POWER CONSUMPTION							
Standby Current	V_{IN} = 40V T_J = Over Temp. Range		5	10		5	10	mA

NOTES

1. Test Conditions unless otherwise stated: V_{IN} = 20V , I_{REF} = 0.
2. V_{CM} = +1.8 to +3.4V
3. V_{CM} = -1 to +1V

APPLICATIONS INFORMATION

The IP1524 is a fixed-frequency pulse-width modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T establishes a constant charging current for C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier.

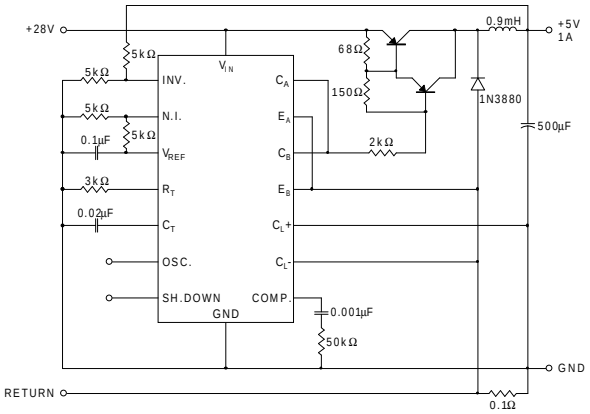
The IP1524 contains an on-board 5V regulator that serves as a reference as well as powering the IP1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output.

The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times.

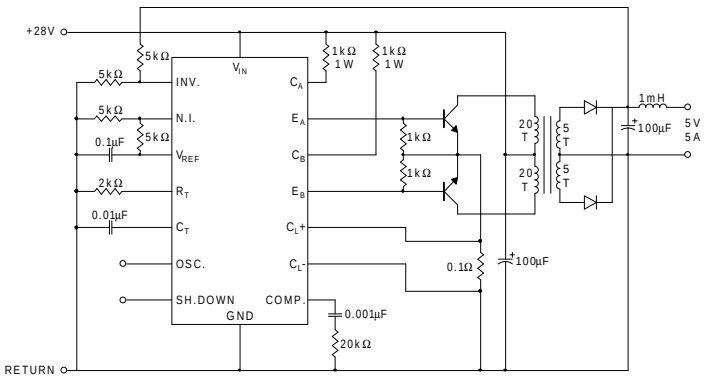
The width of the blanking pulse is controlled by the value of C_T.

The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs.

This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.



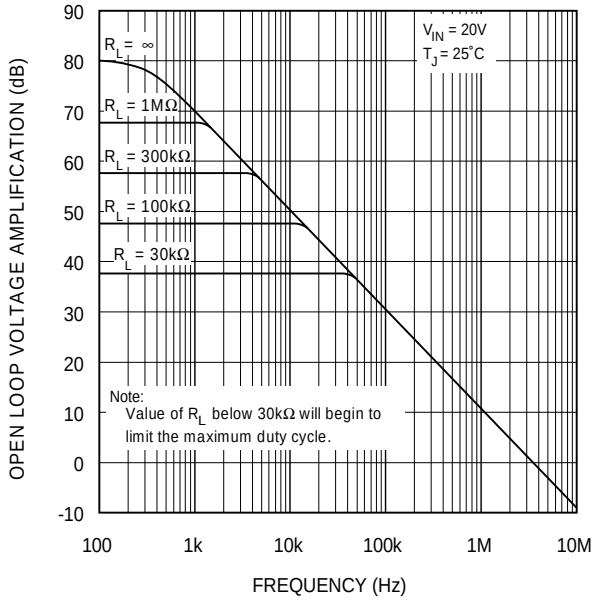
In this conventional single-ended regulator circuit, the two outputs of the IP1524 are connected in parallel for effective 0-90% duty cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.



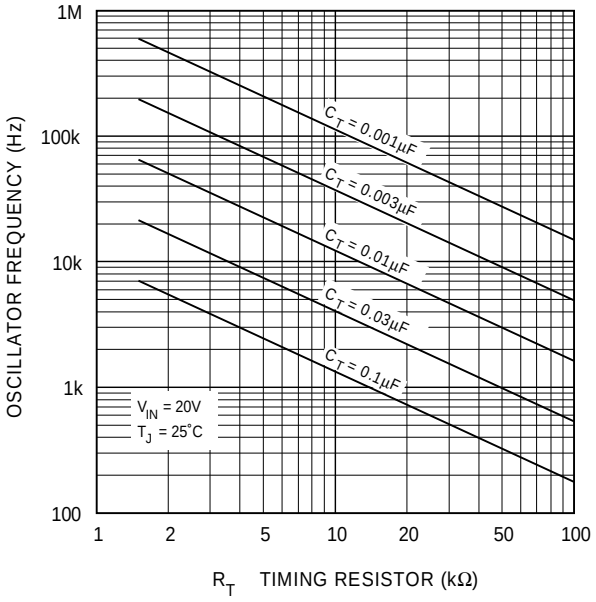
Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the IP1524's internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done in the primary so that the pulse width will be reduced should transformer saturation occur.

TYPICAL PERFORMANCE CHARACTERISTICS

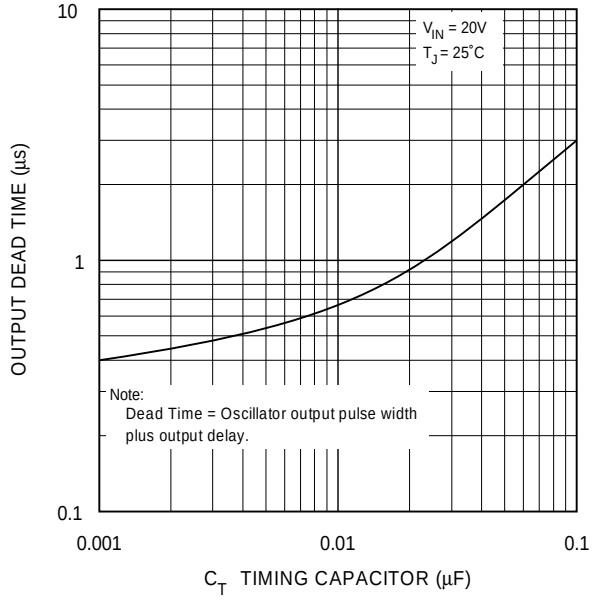
Open-Loop Voltage Amplification of Error Amplifier vs. Frequency



Oscillator Frequency vs. Timing Components



Output Dead Time vs. Timing Capacitance Value



Output Saturation Voltage vs. Load Current