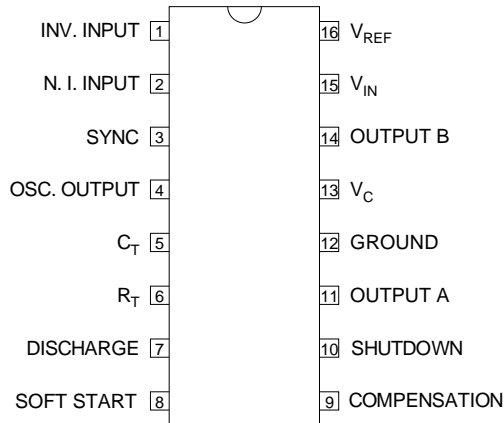


TOP VIEW



J Package – 16 Pin Ceramic DIP
N Package – 16 Pin Plastic DIP
D Package – 16 Pin Plastic (300) SOIC

REGULATING PULSE WIDTH MODULATORS

FEATURES

- Pin Compatible with 1525A Series
- Low Output Crossover Current
- Fixed 100ns Deadtime
- 100Hz to 500kHz Operating Frequencyrange
- 5.1 volt \pm 1% Reference
- Oscillator Sync. Terminal
- Soft Start
- Undervoltage Lockout
- Latching PWM

Order Information

Part Number	J-Pack 16 Pin	N-Pack 16 Pin	D-16 16 Pin	Temp. Range	Note:
IP1P125J	✓			-55 to +125°C	To order, add the package identifier to the part number. eg. IP1P125J
IP3P125D			✓	0 to + 70°C	
IP3P125J	✓			0 to +70°C	
IP3P125N		✓		0 to +70°C	

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

+V _{IN}	Input Voltage		+40V
	Collector Voltage		+40V
	Logic Inputs		-0.3 to +5.5V
	Analogue Inputs		-0.3 to +V _{IN}
	Output Current, Source or Sink		500mA
	Reference Output Load Current		Internally Limited
	Oscillator Charging Current		5mA
P _D	Power Dissipation	T _A = 25°C	1000mW
		Derate @ T _A > 50°C	10mW/°C
P _D	Power Dissipation	T _C = 25°C	2000W
		Derate @ T _C > 25°C	16mW/°C
T _J	Operating Junction Temperature		-55 to +150°C
T _{STG}	Storage Temperature Range		-65 to +150°C
T _L	Lead Temperature	(soldering, 10 seconds)	+300°C

DESCRIPTION

The IP1P125 series of pulse width modulator integrated circuits offers high speed performance optimized for MOSFET drive. Pin compatible with SG1525A, the IP1P125 features low crossover current through the output transistors as well as 95% total usable output pulse width up to 500KHz. High speed latched shutdown is included as well as a precision 5.1 volt reference, error amp, oscillator, latched PWM coparator, totem-pole output drivers, soft-start and undervoltage lockout.

RECOMMENDED OPERATING CONDITIONS

V_{IN}	Input Voltage		+8 to +	
	Collector Voltage		+4.5 to +35V	
	Sink/Source Load Current (Steady State)		0 to 100mA	
	Sink/Source Load Current (Peak)		0 to 400mA	
	Reference Load Current		0 to 20mA	
	Oscillator Frequency Range		100Hz to 500kHz	
R_T	Oscillator Timing Resistor		1.5k Ω to 200k Ω	
C_T	Oscillator Timing Capacitor		470pF to 0.1 μ F	
	Deadtime Resistor Range		0 to 500 Ω	
	Operating Ambient Temperature Range	IP1525A / IP1527A		-55 to +125 $^{\circ}$ C
		IP2525A / IP3527A		-25 to + 85 $^{\circ}$ C
IP3525A / IP3527A			0 to +70 $^{\circ}$ C	

ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1P125			IP3P125			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION								
Output Voltage	$T_J = 25^\circ\text{C}$	5.05	5.10	5.15	5.0	5.1	5.2	V
Line Regulation	$V_{IN} = 8 \text{ to } 35\text{V}$		1	10		1	15	mV
Load Regulation	$I_L = 0 \text{ to } 20\text{mA}$		5	15		5	25	
Temperature Stability note5	Over Operating Range		15	50		15	20	mV
Total Output	$V_{IN} = 8 \text{ to } 35\text{V}, I_L = 0 \text{ to } 20\text{mA}$	5.0		5.2	4.95		5.25	V
Short Circuit Current	$V_{REF} = 0$	25	70	120	25	70	120	mA
Output Noise Voltage note5	$10 \text{ Hz} \leq f \leq 10\text{kHz}$		40	200		40	200	μVrms
Long Term Stability note5			1	10		1	50	$\frac{\text{mV}}{\text{kHr}}$
OSCILLATOR SECTION ²								
Initial Accuracy		37.6	40	42.4	37.6	40	42.4	kHz
Voltage Stability	$V_{IN} = 8 \text{ to } 35\text{V}$		0.1	0.5		0.1	2	
Temperature Stability note5	Over Operating Range		1	4		1	6	%
Minimum Frequency	$R_T = 200\text{k}\Omega \quad C_T = 0.1\mu\text{F}$		80	120		80	120	Hz
Maximum Frequency	$R_T = 2\text{k}\Omega \quad C_T = 470\text{pF} \quad R_D = 0\Omega$		900			900		kHz
Current Mirror	$I_{RT} = 2\text{mA}$	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude	Output, PIN 4, $C_T = 0.1\mu\text{F}$	3.0	4.0		3.0	4.0		V
Clock Width	Output, PIN 4, $C_T = 0.1\mu\text{F}$	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
ERROR AMPLIFIER SECTION ³								
Input Offset Voltage	$V_{cm} = 1.5 \text{ to } 5.2\text{V}$		0.1	5		2	10	mV
Input Bias Current	$V_{cm} = 1.5 \text{ to } 2.5\text{V}$		1	10		1	10	
Input Offset Current	$V_{cm} = 1.5 \text{ to } 5.2\text{V}$		0.1	1		0.1	1	μA
DC Open Loop Gain	$\Delta V_0 = 1 \text{ to } 3\text{V}, R_L \geq 10 \text{ M}\Omega$	60	80		60	80		dB
Gain Bandwidth Product	note5	1	3.5		1	3.5		MHz

ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1P125			IP3P125			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ERROR AMPLIFIER SECTION (cont.) ³								
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6	7.0	3.8	5.6	7.0	
Common Mode Rejection	$V_{CM} = 1.5$ to $5.2V$	60	90		60	90		dB
Supply Voltage Rejection	$V_{IN} = 8$ to $35V$	50	60		50	60		
PWM COMPARATOR								
Minimum Duty Cycle	$V_{PIN1} - V_{PIN2} \geq 150mV$			0			0	%
Maximum Duty Cycle	$V_{PIN2} - V_{PIN1} \geq 150mV$	45	49		45	49		
Input Threshold	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
Input Threshold	Max. Duty Cycle		3.3	3.6		3.3	3.6	
Input Bias Current			50			50		μA
SHUTDOWN SECTION								
Soft Start Current	$V_{SHUTDOWN} = 0V$	25	50	80	25	50	80	μA
Soft Start Low Level	$V_{SHUTDOWN} = 2V$		0.4	0.6		0.4	0.6	V
Shutdown Threshold	To Outputs	0.6	1.3	2.0	0.6	1.3	2.0	
Shutdown Input Current	$V_{SHUTDOWN} = 2.5V$		0.1	1.0		0.1	1.0	mA
Shutdown Delay note5	PIN 10 to Output $T_J = 25^\circ C$		50	300		50	300	ns
OUTPUT DRIVERS (each output) ⁴								
Output Low Level	$I_{SINK} = 20mA$		0.2	0.4		0.2	0.4	V
	$I_{SINK} = 100mA$		1.0	2.5		1.0	2.5	
Output High Level	$I_{SOURCE} = 20mA$	18	19		18	19		V
	$I_{SOURCE} = 100mA$	17	18		17	18		
Collector Leakage Current	$V_C = 35V$			200			200	V
Rise Time	$C_L = 1nF$ $T_J = 25^\circ C$		100	300		100	300	ns
Fall Time	$C_L = 1nF$ $T_J = 25^\circ C$		50	300		50	300	
Dead Time	$C_L = 1nF$ $T_J = 25^\circ C$		100			100		

NOTES

note5

These parameters, although guaranteed over the recommended conditions are not 100% tested in production.