SEME LAB

D2008UK

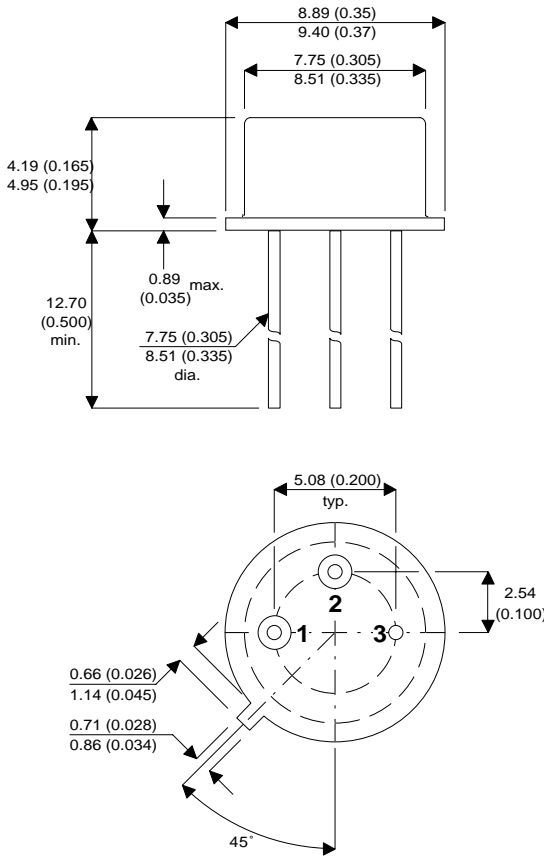## METAL GATE RF SILICON FET

MECHANICAL DATA

TO-39 PACKAGE

PIN1 – DRAIN   PIN2 – GATE   PIN3 – SOURCE

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET
5W – 28V – 400MHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **LOW C_{rss}**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN – 13 dB MINIMUM**

APPLICATIONS

- VHF COMMUNICATIONS from DC to 400MHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P_D	Power Dissipation	29W
BV_{DSS}	Drain – Source Breakdown Voltage	65V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	2A
T_{stg}	Storage Temperature	–65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$	$I_D = 10mA$	65			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 28V$	$V_{GS} = 0$			2	mA
I_{GSS}	Gate Leakage Current	$V_{GS} = 20V$	$V_{DS} = 0$			1	μA
$V_{GS(th)}$	Gate Threshold Voltage*	$I_D = 10mA$	$V_{DS} = V_{GS}$	1		7	V
g_{fs}	Forward Transconductance*	$V_{DS} = 10V$	$I_D = 0.4A$	0.36			S
G_{PS}	Common Source Power Gain	$P_O = 5W$		13			dB
η	Drain Efficiency	$V_{DS} = 28V$	$I_{DQ} = 0.2A$	40			%
VSWR	Load Mismatch Tolerance	f = 400MHz		20:1			—
C_{iss}	Input Capacitance	$V_{DS} = 0$ $V_{GS} = -5V$	f = 1MHz			20	pF
C_{oss}	Output Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$	f = 1MHz			11	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$	f = 1MHz			1	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

THERMAL DATA

$R_{THj-case}$	Thermal Resistance Junction – Case	Max. 6.0°C / W