Ordering number: EN 2057B

Monolithic Linear IC

SANYO No.2057B

LA5316M

Variable Divided Voltage Generator for LCD

Overview

The LA5316M is a variable divided voltage generator IC for multiple drive of LCD matrix.

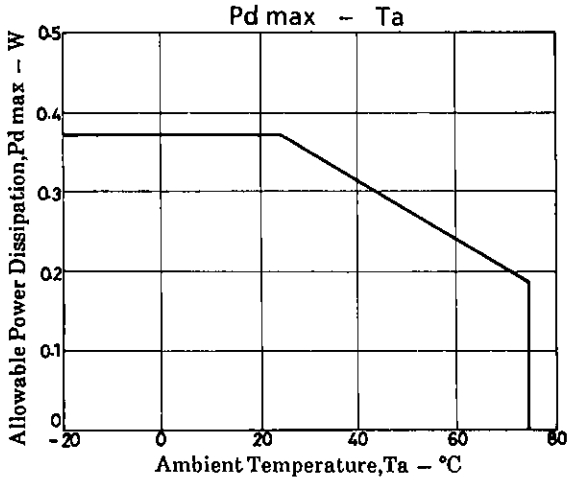
Features

- Power supply for variable bias LCD drive (1/5 to 1/13 bias available by on-chip resistances).
- 5 OP amps to deliver 5 voltage outputs.
- Low current dissipation (1.5mA max).
- Miniflat package.
- On-chip variable voltage regulator for V_{REF}.

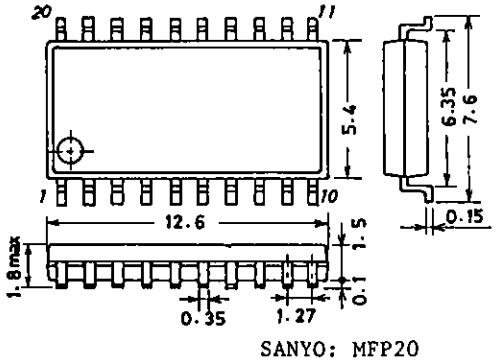
Maximum Ratings at Ta = 25°C				unit
Maximum Supply Voltage	V_{CC} max	GND-V_{CC}	−35 to 0	V
Maximum Output Current	I_{OUT} max	V1,V2,V3,V4,V5	15	mA
Allowable Power Dissipation	Pd max		370	mW
Operating Temperature	**Topr**		−20 to +75	°C
Storage Temperature	Tstg		−30 to +125	°C

Operating Conditions at Ta = 25°C				unit
Supply Voltage	V_{CC} op	GND-V_{CC} : (When V1 > −1V, I_{IN} is needed.) Note 1	−30 to −10	V
Recommended Input Voltage	V_{REF}	GND-V_{REF} : $V_{REF} \geqq V_{CC}$ Note 1	−30 to −6	V
Recommended Input Current	I_{IN}	V_{IN} : V1 > −1V, current source of I_{IN} : 1V or greater relative to GND	0.2 to 3	mA
Recommended Output Current	I_{OUT}1	V1	−0.1 to +5	mA
	I_{OUT}2,3	V2,V3	−5 to +5	mA
	I_{OUT}4,5	V4,V5	−10 to +0.1	mA

Note 1 : Set V_{CC}, V_{REF} so that | V2 | , | V_{CC}-V5 | become 1V or greater.



Package Dimensions 3036B
(unit : mm)



SANYO: MFP20

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Operating Characteristics at Ta = 25°C, V_{CC} = −16V

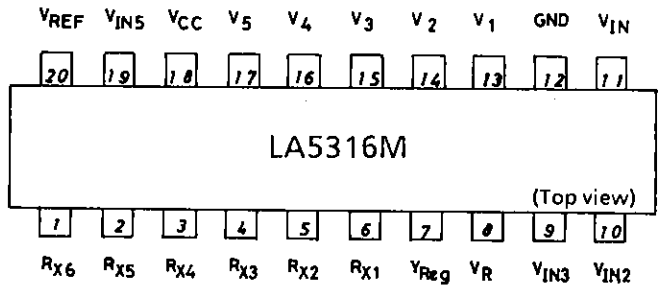
				min	typ	max	unit
Current Dissipation	I_{CC}	V_{IN}, GND-V_{CC}, V_{REF} : V_{CC} = V_{REF} = −16V, V_{IN} = GND, R_X = 5R				1.5	mA
Output Voltage Ratio 1	Ra1	V2/V1		1.96	2.00	2.04	
Output Voltage Ratio 2	Ra2	(V5-V3) / (V5-V4)	Vref = −12V	1.96	2.00	2.04	
Output Voltage Ratio 3	Rb1	V5/V1	V_{CC} = −16V,	8.73	9.00	9.27	
Output Voltage Ratio 4	Rb2	V5/V2	1/9 bias	4.37	4.50	4.63	
Output Voltage Ratio 5	Rb3	V5/(V5-V3)	(R_X = 5R)	4.37	4.50	4.63	
Output Voltage Ratio 6	Rb4	V5/(V5-V4)		8.73	9.00	9.27	
Internal Resistance Ratio 1	4R	V_{IN}3-R_X1			4		
Internal Resistance Ratio 2	5R	V_{IN}3-R_X2	Resistance ratio		5		
Internal Resistance Ratio 3	6R	V_{IN}3-R_X3	referenced to R		6		
Internal Resistance Ratio 4	7R	V_{IN}3-R_X4	across pins ⑤ and ⑥		7		
Internal Resistance Ratio 5	8R	V_{IN}3-R_X5			8		
Internal Resistance Ratio 6	9R	V_{IN}3-R_X6			9		
Resistance	R	R_X1-R_X2 : R value when 0.5V is applied across pins ⑤ and ⑥			20		kΩ
Load Regulation 1	ΔV1	V1 : +100μA < I_{OUT}1 < +5mA				20	mV
Load Regulation 2	ΔV2	V2 : +100μA < I_{OUT}2 < +5mA				20	mV
Load Regulation 3	ΔV3	V3 : +100μA < I_{OUT}3 < +5mA				20	mV
Load Regulation 4	−ΔV2	V2 : −5mA < I_{OUT}2 < −100μA				20	mV
Load Regulation 5	−ΔV3	V3 : −5mA < I_{OUT}3 < −100μA				20	mV
Load Regulation 6	−ΔV4	V4 : −10mA < I_{OUT}4 < −100μA				20	mV
Load Regulation 7	−ΔV5	V5 : −10mA < I_{OUT}5 < −100μA				20	mV
Regulator Voltage	V_{Reg}	GND-V_{Reg} : Pins ⑦ and ⑧ shorted		−6.5	−6.2	−5.9	V
VReg Load Regulation	ΔV_{Reg}	V_{Reg} : −5mA < I_O < +1mA				50	mV

Pin Functions

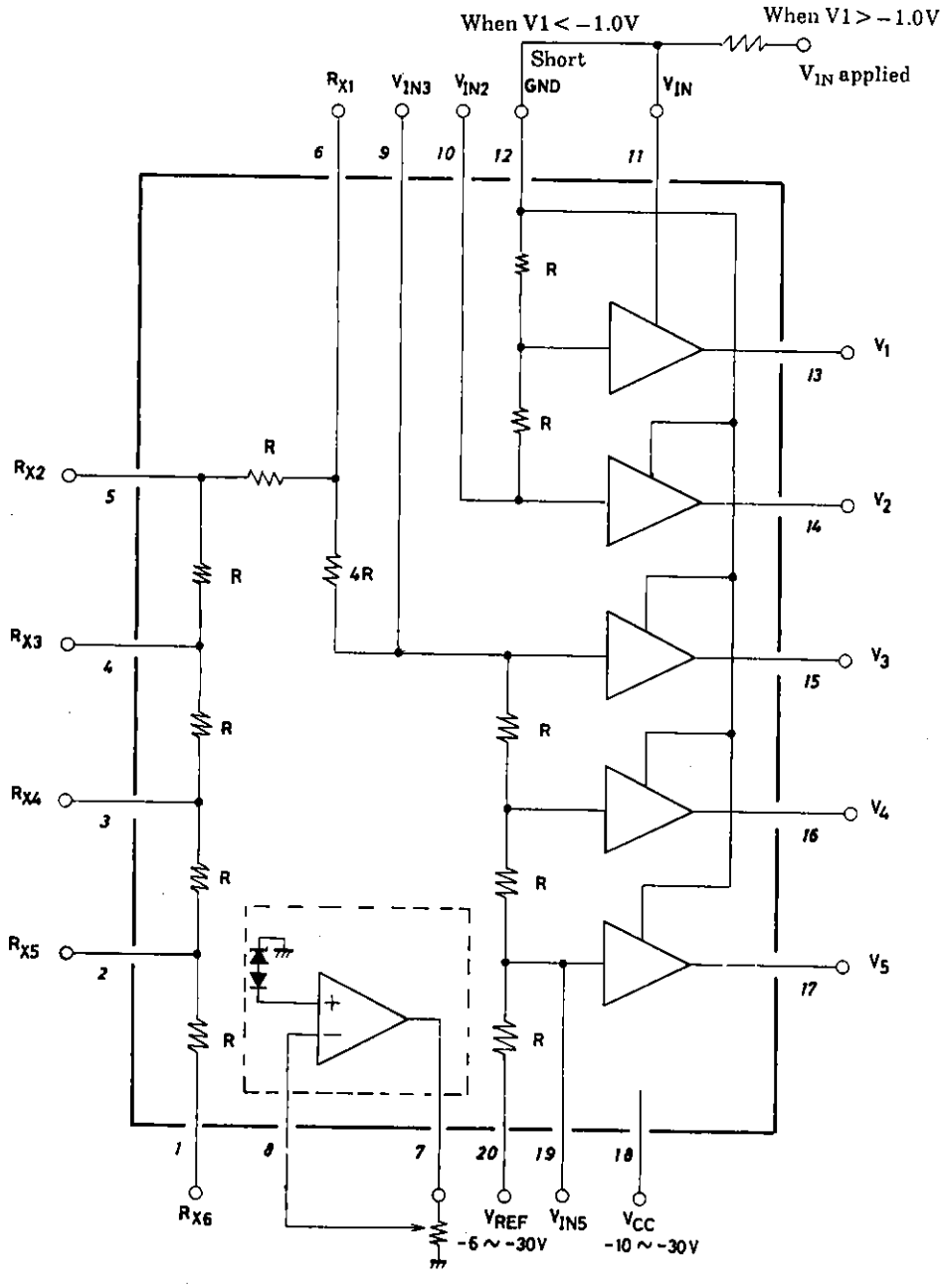
Pin No.	Pin Name	Function	Remarks
1	R_X6	R_X pin	Pin ⑩ shorted R_X = 9R
2	R_X5	R_X pin	Pin ⑩ shorted R_X = 8R
3	R_X4	R_X pin	Pin ⑩ shorted R_X = 7R
4	R_X3	R_X pin	Pin ⑩ shorted R_X = 6R
5	R_X2	R_X pin	Pin ⑩ shorted R_X = 5R
6	R_X1	R_X pin	Pin ⑩ shorted R_X = 4R
7	V_{Reg}	V_{Reg} output	For supplying V_{REF}
8	V_R	V_{Reg} OP amp V_{IN} −	
9	V_{IN}3	V3 input	
10	V_{IN}2	V2 input	
11	V_{IN}	V1 supply (+supply)	When V1 > −1.0V, V_{IN} is applied. When V1 < −1.0V, this pin is shorted to GND.
12	GND	GND	
13	V1	V1 output	
14	V2	V2 output	
15	V3	V3 output	
16	V4	V4 output	
17	V5	V5 output	
18	V_{CC}	V_{CC} supply (−supply)	
19	V_{IN}5	V5 input	
20	V_{REF}	V_{REF} supply (−supply)	

Note) Do not use the NC pin.

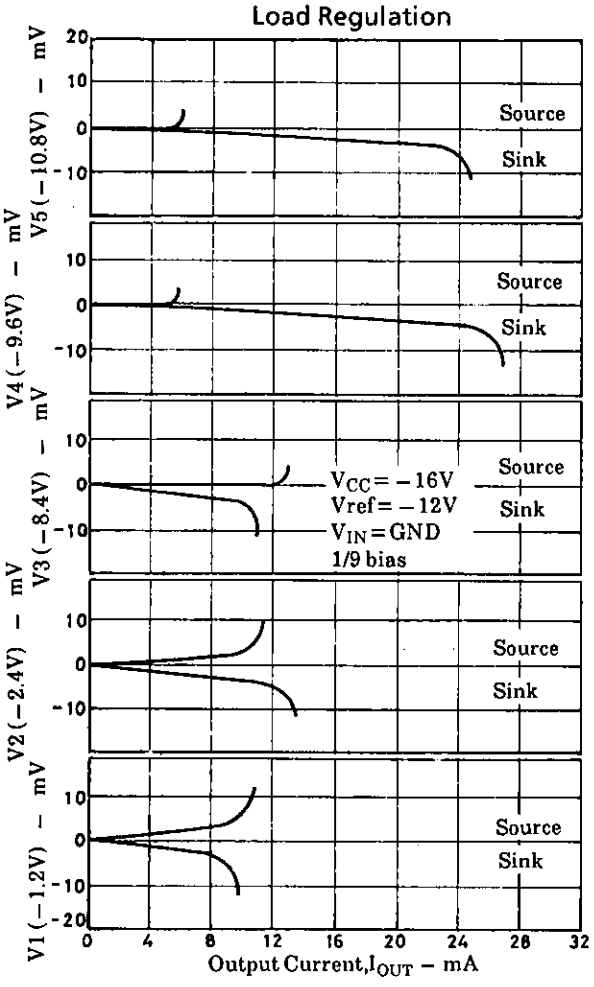
Pin Assignment



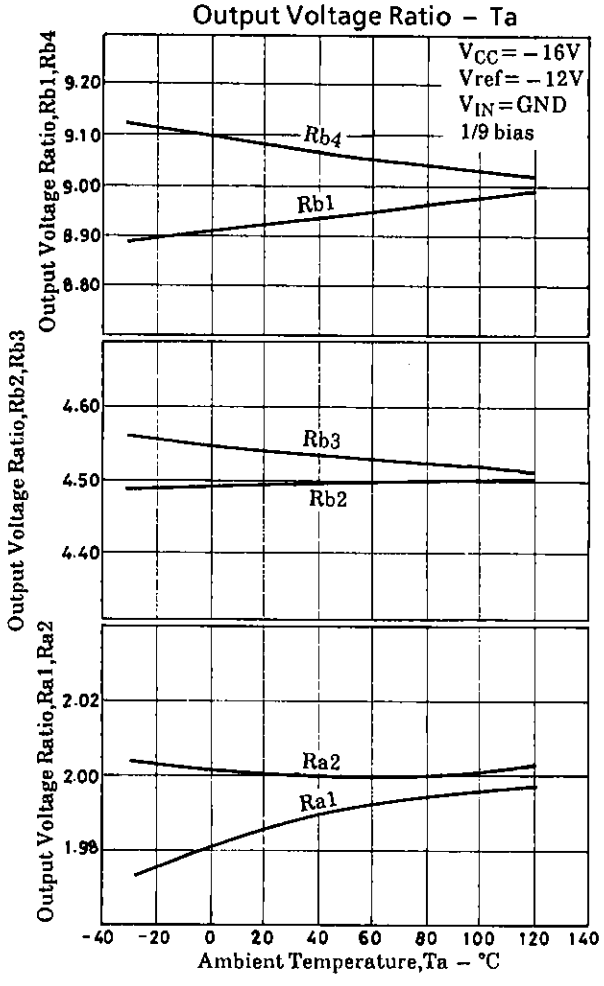
Equivalent Circuit Block Diagram



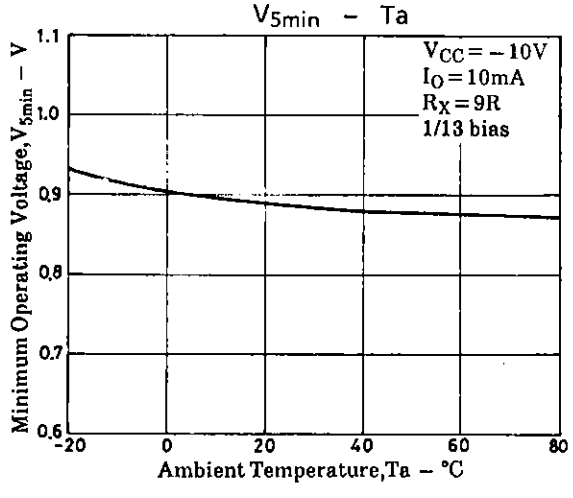
Load Regulation



Output Voltage Ratio − Ta



V_{5min} − Ta



V_{2min} − Ta