

SANYO

No.2801A

LA8610M

Pager Narrow-Band FM-IF Circuit

Overview

The LA8610M is a narrow-band FM-IF circuit for use in radio paging system. It incorporates a number of pager circuit blocks into a single chip, including an IF amplifier and quadrature detector, low-pass filter, wave-shaping circuit, voltage regulator and power amplifier.

The LA8610M features ultra-low power dissipation and low voltage operation down to 1.0V. With a supply voltage of 1.5V, it typically dissipates only 0.7mA when fully active and 5 μ A in battery-save mode.

The LA8610M is available in a 20-pin plastic MFP.

Features

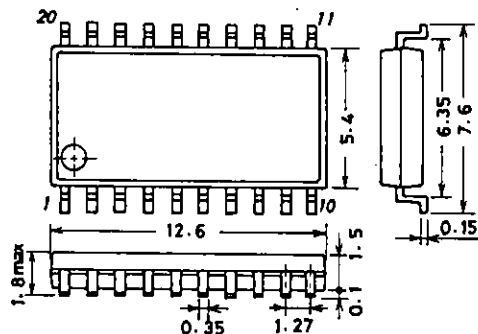
- Low-voltage operation : 1.0 to 5.0V
- Ultra-low power dissipation (0.7mA)
- Built-in voltage regulator (typ 1.07V at 2mA)
- Adjustment-free quadrature detector reduces circuit cost
- FSK signal wave-shaping circuit
- Battery-save mode and on-chip battery check function
- On-chip power amplifier for tone signal

Maximum Ratings at Ta = 25°C

				unit
Maximum Supply Voltage	V _{CC} max	Pins 17,20	6	V
Maximum Flow-in Current	I _{I1} max	Pin 11	100	mA
Allowable Power Dissipation	P _d max		350	mW
Operating Temperature	T _{opr}		-20 to +70	°C
Storage Temperature	T _{stg}		-40 to +125	°C

Operating Conditions at Ta = 25°C

				unit
Recommended Supply Voltage	V _{CC}		1.4	V
Operating Voltage Range	V _{CC op}		1.0 to 5.0	V

Package Dimensions 3036B-IC
(unit: mm)

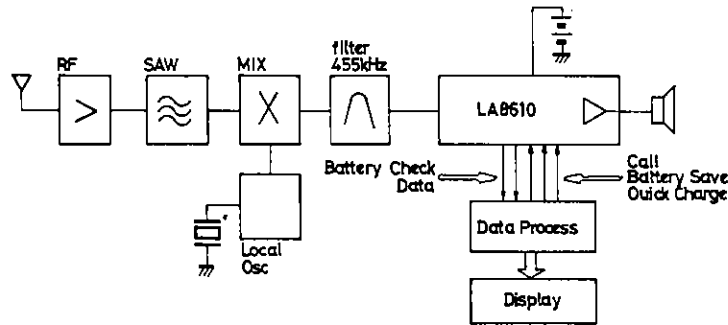
SANYO: MFP20

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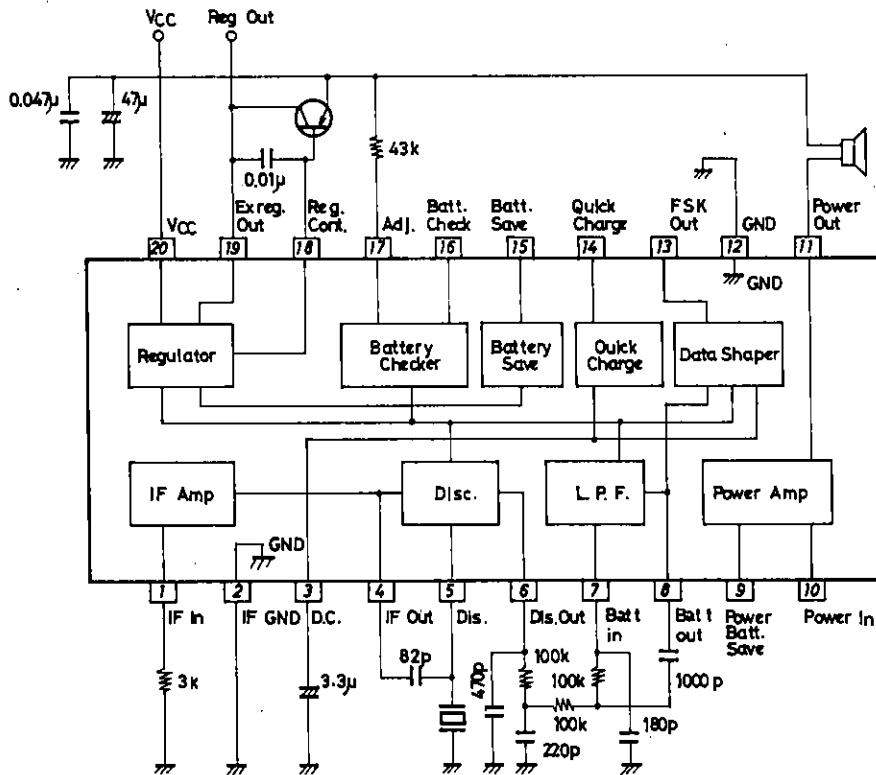
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 1.4\text{V}$, $f_c = 455\text{kHz}$, $f_m = 100\text{Hz}$, $\text{Dev} = \pm 2.5\text{kHz}$, $\text{mod} = 30\%$,
 $V_{in} = (\text{SG open-mode}) - 13\text{dB}$

			min	typ	max	unit
Current Dissipation	$I_{CC} (1)$	No input signal, $V_{15} = 1.4\text{V}$, $V_9 = 1.4\text{V}$	0.7	1.0		mA
Battery-Save Current	$I_{CC} (2)$	No input signal	5.0	10.0		μA
-3dB Limiting Sensitivity	-3dBLS	$V_{IN} = 80\text{dB}\mu$ standard, -3dB input	25	20		$\text{dB}\mu$
Demodulation Output	V_o	$V_{IN} = 80\text{dB}\mu$	30	50		mV
Total Harmonic Distortion	THD	$V_{IN} = 80\text{dB}\mu$	2.0	4.0		%
Signal-to-Noise Ratio	S/N	$V_{IN} = 80\text{dB}\mu$	40	50		dB
AM Rejection Ratio	AMR	$V_{IN} = 80\text{dB}\mu$, AM modulation	30	40		dB
Wave-Shaped Output Level	V_H	$V_{15} = 1.4\text{V}$, $V_3 = 0.8\text{V}$, $V_8 = 0.5\text{V}$	1.0			V
	V_L	$V_{15} = 1.4\text{V}$, $V_3 = 0.8\text{V}$, $V_8 = 1.1\text{V}$			0.15	V
Duty Cycle	Duty			50		%
Battery Check Voltage	V_{Batt}	$R_{17} = 43\text{k}\Omega$	0.93	1.00	1.07	V
Regulated Output Voltage	V_{Reg}	$I_o = 2\text{mA}$	0.97	1.07	1.17	V
Power Output Voltage	P_o	$R_L = 68\text{k}\Omega$, $f = 4.5\text{kHz}$, $P_i = 50\text{mVrms}$	600	700		mV

Typical Paging System



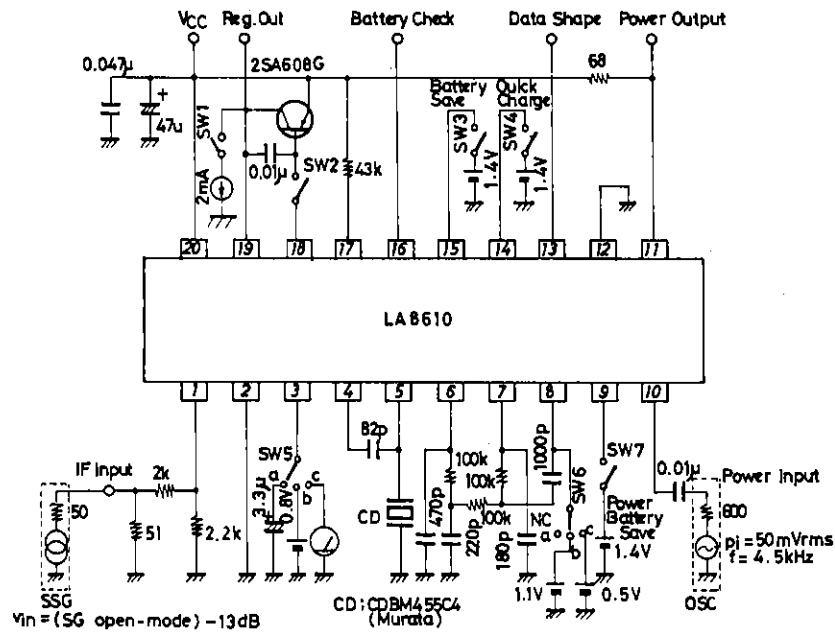
Equivalent Circuit Block Diagram and Peripheral Circuit



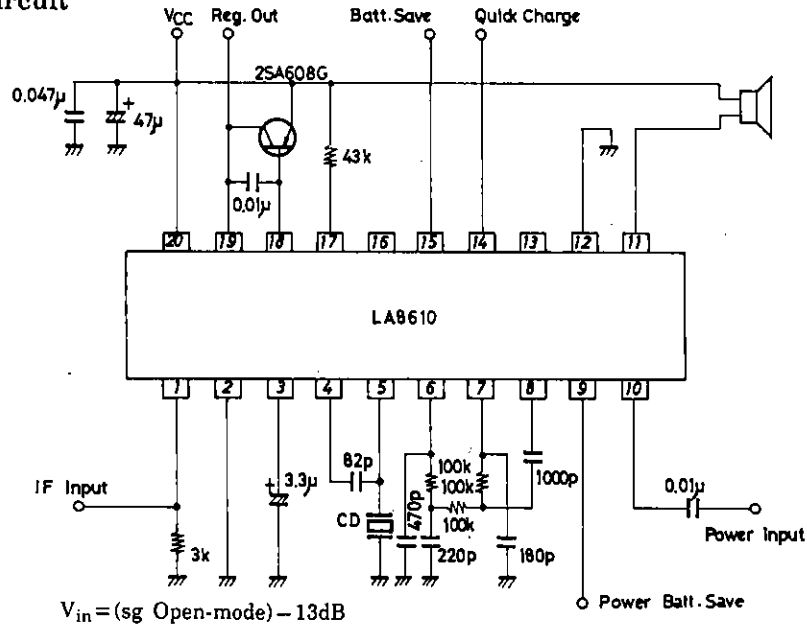
Unit (resistance: Ω , capacitance: F)

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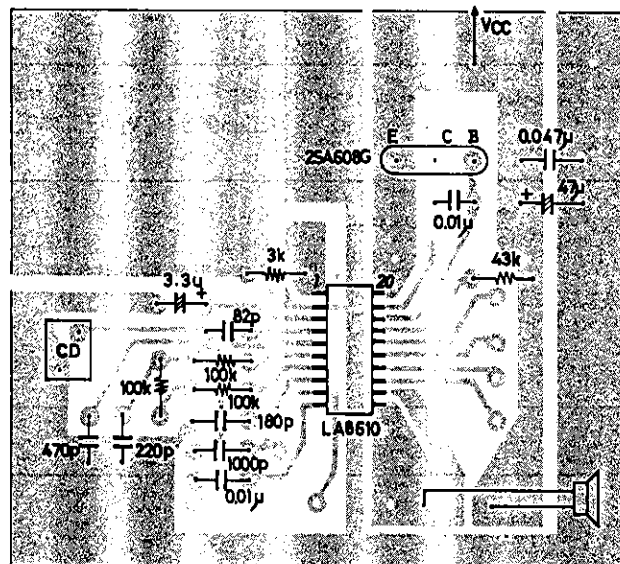
Test Circuit



Sample Application Circuit



Sample Printed Circuit Pattern



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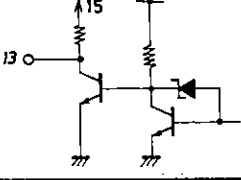
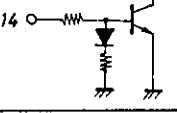
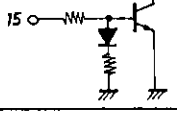
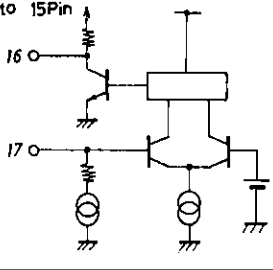
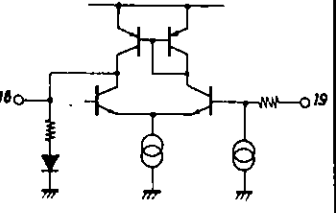
Pin Descriptions

Pin No.	Pin Name	Internal Circuit	Description
1	IF IN		IF amplifier signal input and signal ground
2	IF GND		
3	D.C		Decoupling capacitor
4	IF OUT		IF amplifier output
5	DIS		Quadrature detector input. Connected to pin 4 via a phase shift circuit.
6	DIS OUT		Detected FM signal output
7	Buff IN		Connections for 3rd-order low pass filter using external resistors and capacitors
8	Buff OUT		
9	Power Batt Save		Active-High power amplifier enable input (High = $V_{CC} \pm 0.6V$)
10	Power IN		Power amplifier input and output
11	Power OUT		
12	GND		Ground

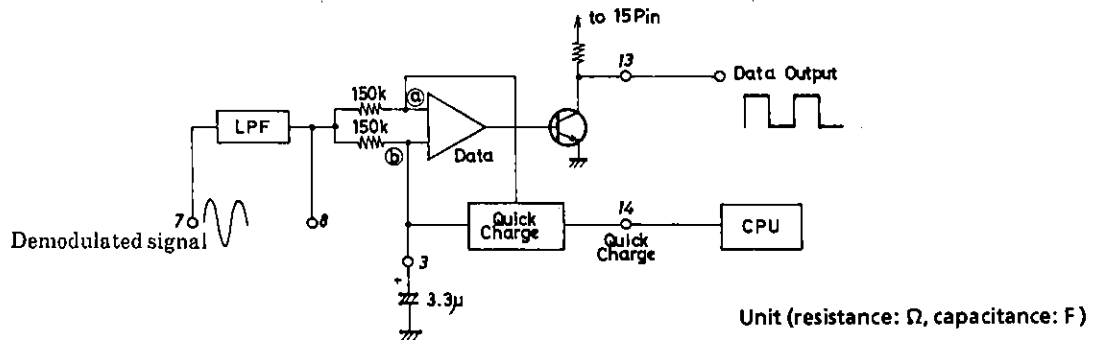
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Pin No.	Pin Name	Internal Circuit	Description
13	FSK OUT		Shaped signal derived from the signal input on pin 8
14	Quick Charge		Active-High quick-charge circuit control input (High = $V_{CC} \pm 0.6V$)
15	Batt Save		Battery-save control pin. Circuit operation is stopped when this pin is held Low. Save : $I_{CC0} = 5\mu A$ typ.
16	Batt Check		Battery check and check threshold adjustment pins. The voltage on pin 16 is output 'High' when the supply voltage drops below the value set by the internal and external resistances on pin 17.
17	ADJ		
18	REG CONT		Voltage regulator connections. Requires an external PNP transistor with base to pin 18, collector to pin 19 and emitter to V_{CC} . Output voltage on pin 19 is typically 1.07V.
19	EX-REG OUT		
20	V_{CC}		Positive power supply pin. Operating supply range is 1.0 to 5V.

● Quick-Charge Circuit

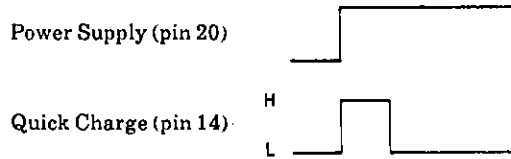


The quick-charge circuit compensates a duty of the output signal on pin 13 when power is turned on or the LA8610M is switched from battery-save mode to the active state.

Pin 14 should be High when power is switched on or the device put into the active state. The quick charge circuit then sources current into the capacitor on pin 3 to equalize the voltages at points a and b in the circuit above. If quick charge is not used, the capacitor on pin 3 is charged at a rate determined by the time constant of the capacitor (3.3µF) and internal resistor (150kΩ).

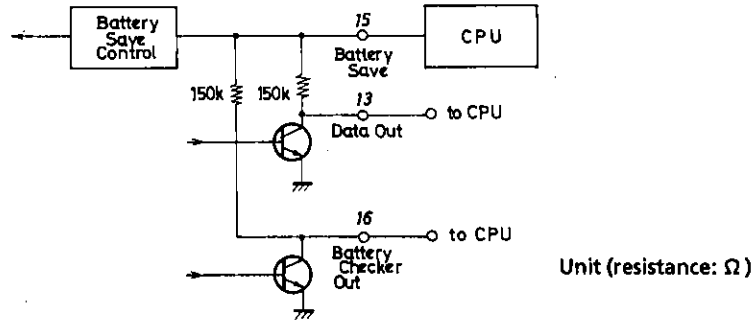
Pin 14 should be made Low or Open after quick-charge is completed, as shown by the waveform below.

Timing

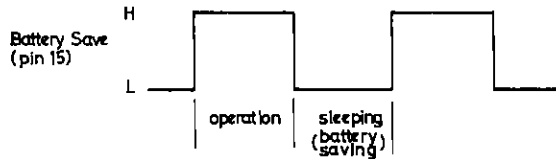


Note also that the phase of the wave-shaped output on pin 13 advances as the capacitor's value decreases. The recommended value of the capacitor is 3.3 μ F.

• Battery Save and Battery Check



Timing



The battery-save function extends battery life for intermittent device operation. The LA8610M is operational when pin 15, the battery-save control pin, is High ($V_{CC} \pm 0.6V$). When pin 15 is Low, the internal circuits are disabled to reduce power consumption.

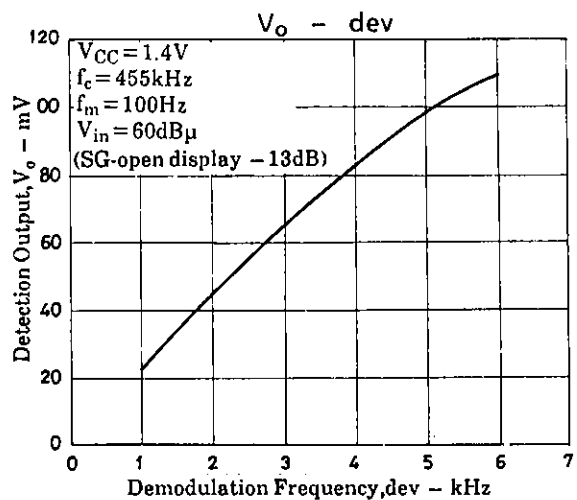
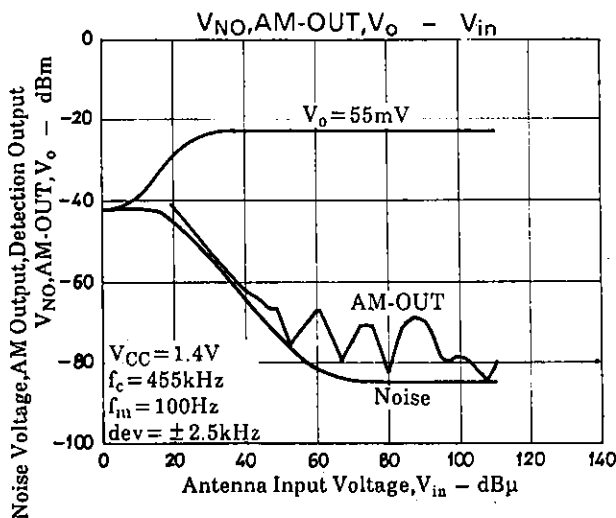
When the power supply voltage drops below the threshold set by the internal and external resistances on pin 17, the voltage present on pin 15 is output on pin 16. Hence, pin 16 will go High when the LA8610M is active and the battery voltage drops below the threshold. It is normally Low.

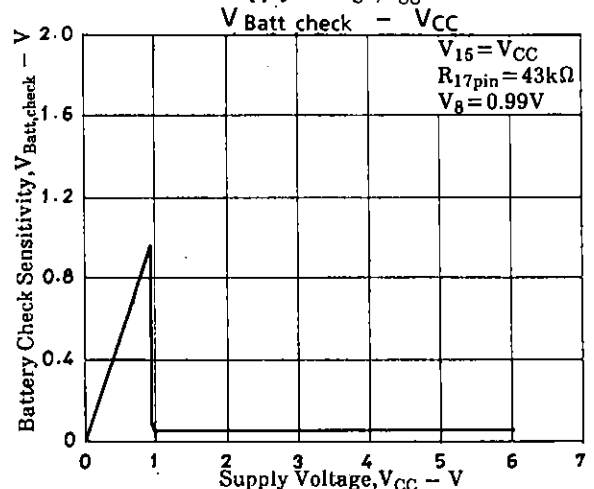
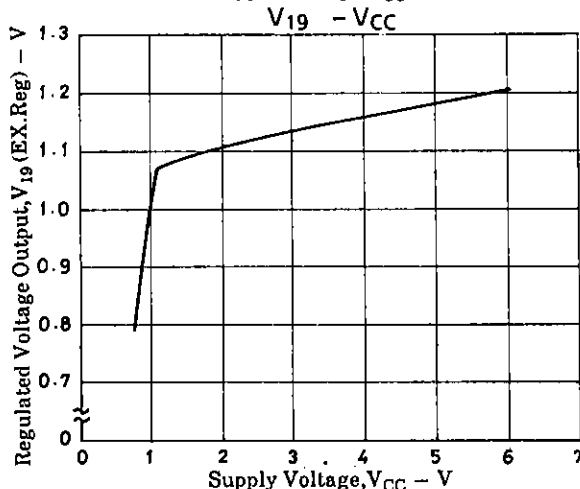
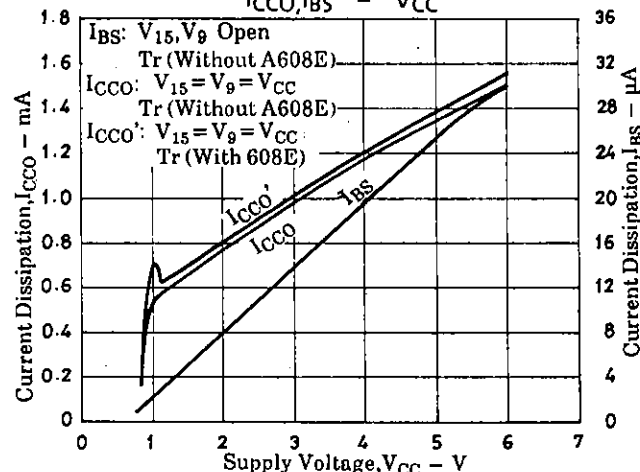
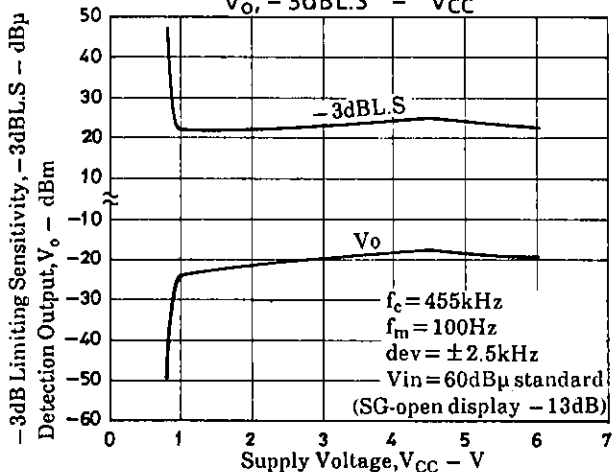
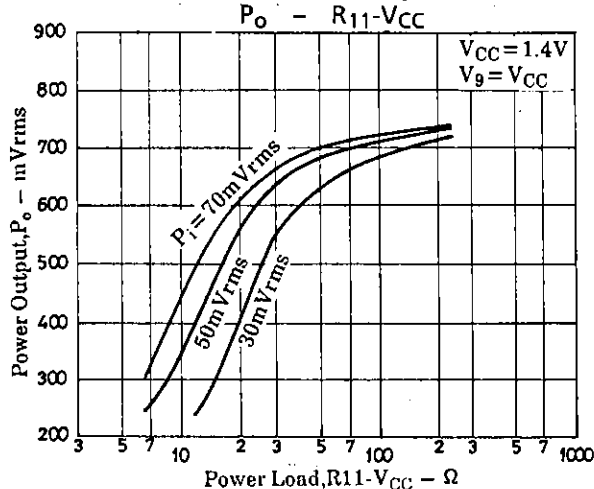
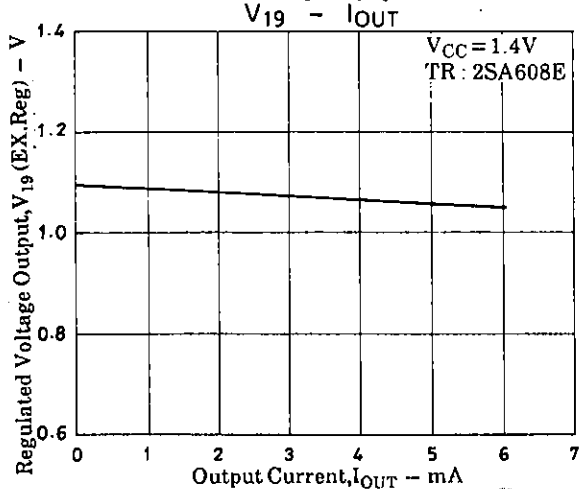
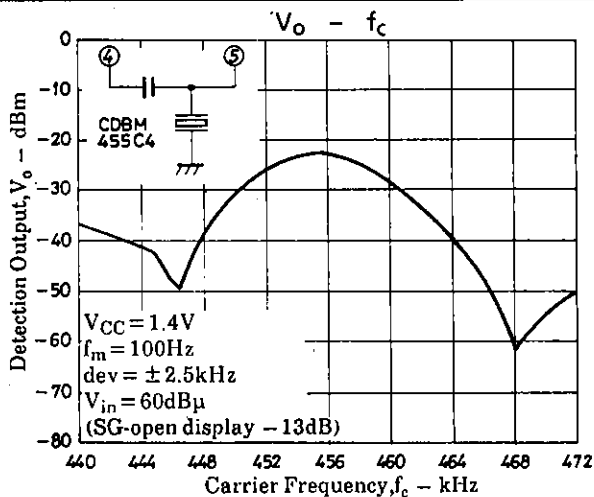
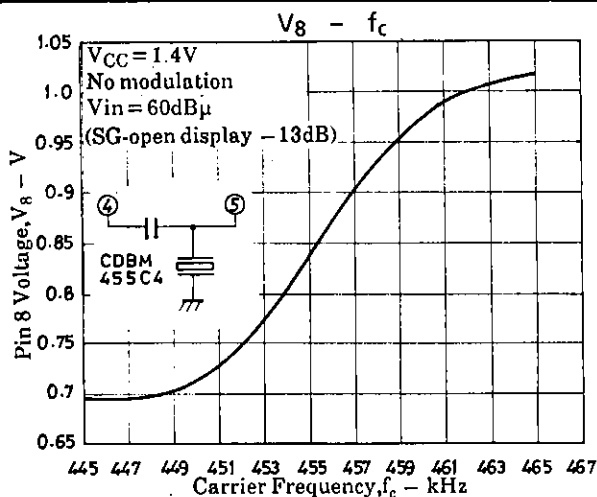
• Voltage Regulator

The voltage regulator requires an external PNP transistor, with base to pin 18, collector to pin 19 and emitter to V_{CC} . A regulated output of typically 1.07V is available on the PNP collector.

• Control Voltage Range

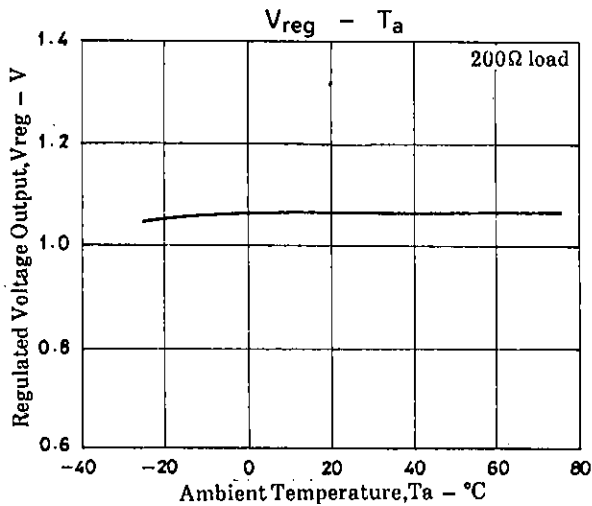
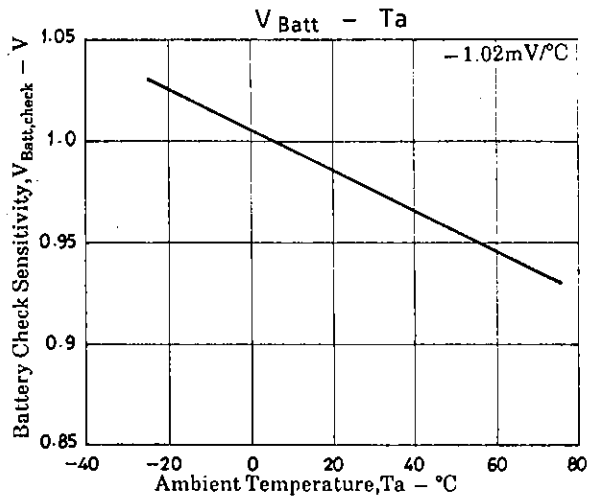
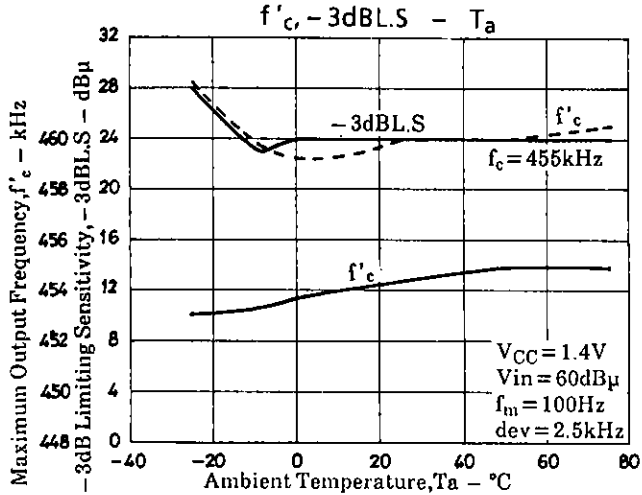
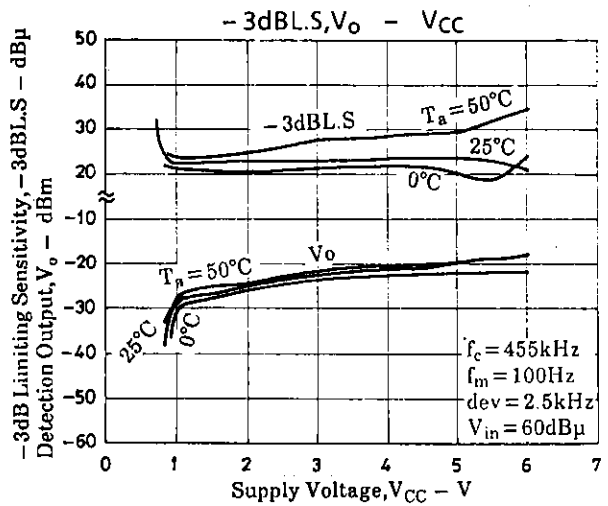
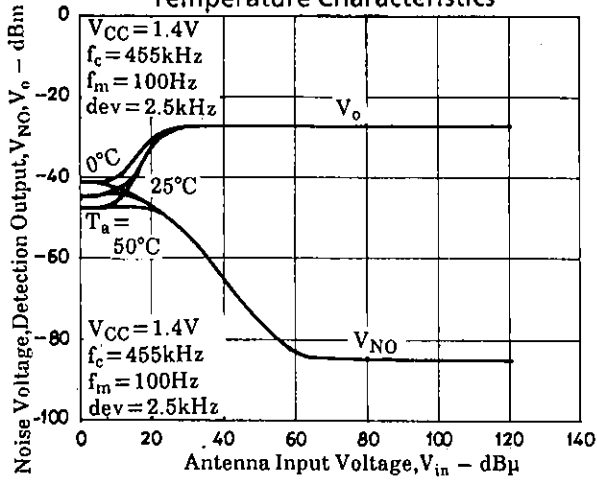
The value of the High-level control voltage applied to pins 9, 14 and 15 should be within the range $V_{CC} \pm 0.6V$. Voltages outside this range may cause abnormal device operation.





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Temperature Characteristics



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