

SANYO

No. 4456

LB1881V**Three-Phase Brushless Motor Driver****Overview**

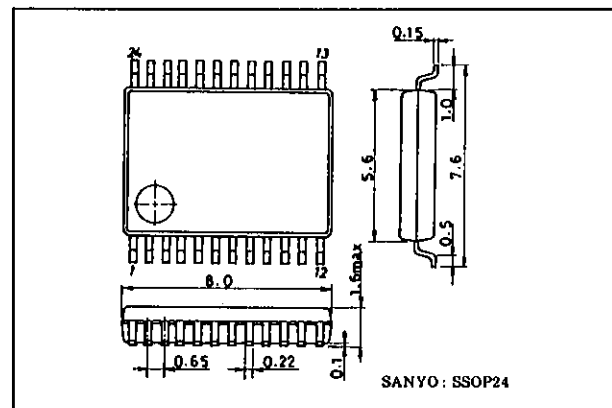
The LB1881V is a three-phase brushless motor driver IC designed for use as a camcorder capstan or drum motor driver, or as a digital audio tape player/recorder motor driver.

Features

- 120° voltage linear system
- Appropriate for portable applications, since the LB1881M reduces system power requirements by using motor voltage control for speed control.
- Built-in torque ripple compensation circuit
- Small external capacitances due to the adoption of a soft switching technique (chip capacitor).
- Built-in thermal shutdown circuit
- Built-in FG amplifier

Package Dimensions

unit: mm

3175A-SSOP24**Specifications****Absolute Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V _{CC1} max		7	V
	V _{CC2} max		12	V
	V _S max		V _{CC2}	V
Output applied voltage	V _O max		V _S + 2	V
Input applied voltage	V _I max	All input pins	V _{CC1}	V
Output current	I _O max		1.0	A
Allowable power dissipation	P _d max		0.5	W
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V _{CC1}	V _{CC1} ≤ V _{CC2}	4.0 to 6.0	V
	V _{CC2}		4 to 10	V
	V _S		Up to V _{CC2}	V

Electrical Characteristics at Ta = 25°C, V_{CC1} = 5 V, V_{CC2} = 7 V, V_S = 3 V

Parameter	Symbol	Condition	Rating			Unit	Note
			min	typ	max		
Supply current	I _{CC1}	V _{BR} = 5 V		3.0	5.0	mA	
	I _{CC2}	V _{BR} = 5 V		6.5	10.0	mA	
	I _S	V _{BR} = 5 V, R _L = ∞			5.0	mA	
Output quiescent current	I _{CCOQ}	V _{STBY} = 0 V			100	μA	
	I _{SOQ}	V _{STBY} = 0 V, R _L = ∞			150	μA	
Output saturation voltage	V _{O(sat)}	I _{OUT} = 0.6 A, sink + source			1.7	V	
Output TRS withstand voltage	V _{O(sus)}	I _{OUT} = 20 mA	12			V	1
Output quiescent voltage	V _{OQ}	V _{BR} = 5 V	1.45	1.55	1.65	V	
Hall amplifier input offset voltage	V _{HOFFSET}		-5		+5	mV	1
Hall amplifier common mode input voltage range	V _{HCOM}		1.4		2.8	V	
Hall I/O voltage gain	GV _{HO}	Range = 8.2 kΩ	34.0	37.0	40.0	dB	
Brake pin high level voltage	V _{BRH}		2.0			V	
Brake pin low level voltage	V _{BRL}				0.8	V	
Brake pin input current	I _{BRIN}				120	μA	
Brake pin leakage current	I _{BRLEAK}				-30	μA	
FRC pin high level voltage	V _{FRCH}		2.8			V	
FRC pin low level voltage	V _{FRCL}				1.2	V	
FRC pin input current	I _{FRGIN}				100	μA	
FRC pin leakage current	I _{FRCLEAK}				-30	μA	
Upper side residual voltage	V _{XH}	I _{OUT} = 100 mA, V _{CC2} = 6 V, V _S = 2 V	0.285		0.455	V	
Lower side residual voltage	V _{XL}	I _{OUT} = 100 mA, V _{CC2} = 6 V, V _S = 2 V	0.350		0.440	V	
Residual voltage inflection point	V _{SΔVX}	I _{OUT} = 100 mA, V _{CC2} = 6 V		0.9		V	1
Overlap level	OL	V _{CC2} = 6 V, V _S = 3 V, R _L = 100 Ω (Y)	60	70	80	%	
Overlap vertical difference	ΔOL	V _{CC2} = 6 V, V _S = 3 V, R _L = 100 Ω (Y)	-10	0	+10	%	
Standby on voltage	V _{STBYL}		-0.2		+0.8	V	2
Standby off voltage	V _{STBYH}		2		5	V	
Standby pin bias current	I _{STBYIN}				100	μA	
Thermal protection circuit operating temperature	T _{TSD}		150	180	210	°C	1
Thermal protection circuit hysteresis	ΔT _{TSD}			15		°C	1
[FG amp]							
FG amplifier input offset voltage	V _{FGOFFSET}		-8		+8	mV	
Open loop voltage gain	GV _{FG}	f = 10 kHz		43		dB	
Source output saturation voltage	V _{FGOU}	I _O = -2 mA	3.7			V	
Sink output saturation voltage	V _{FGOD}	I _O = 2 mA			1.3	V	
Common mode signal exclusion ratio	GHR			80		dB	1
FG amplifier common mode input voltage range	V _{FGCH}		0		3.5	V	
Phase margin	φ _M			20		deg	1
Schmitt amplifier threshold voltage	V _{FGSH}	V _{FGIN} * = 2.5 V, when V _{FGOUT2} goes from high to low	2.45	2.50	2.55	V	
Schmitt amplifier hysteresis width	V _{FGSHIS}	V _{FGIN} * = 2.5 V	20	40	60	mV	

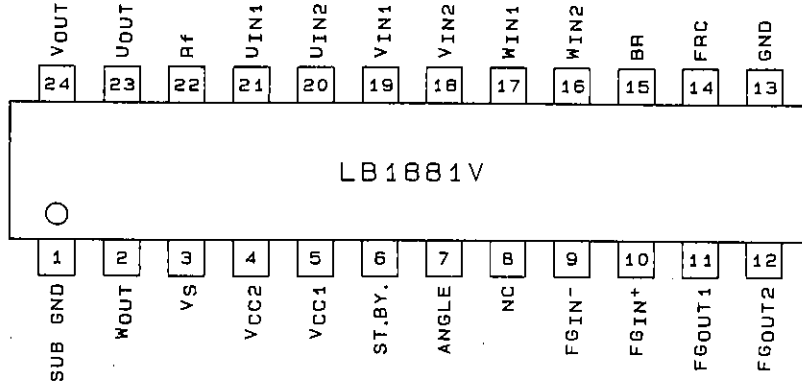
Note: 1. These are target settings, and are not measured. The overlap ratings are taken as test ratings without change.

2. When the standby pin is open the IC will be in the standby state.

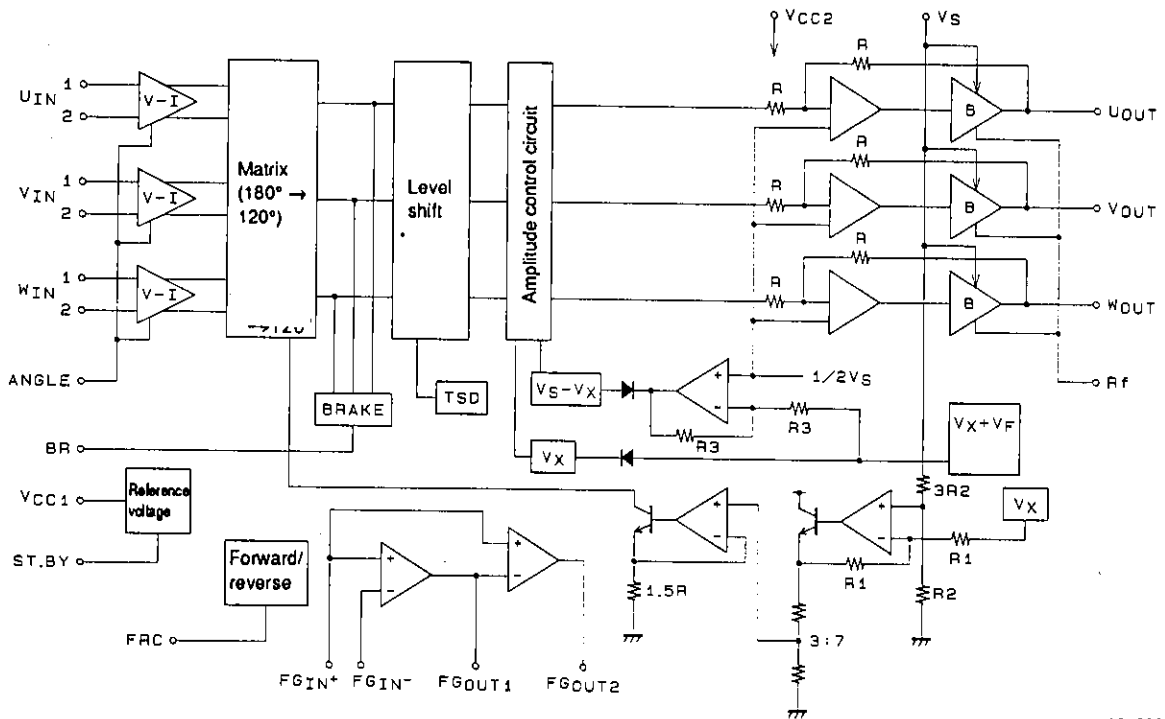
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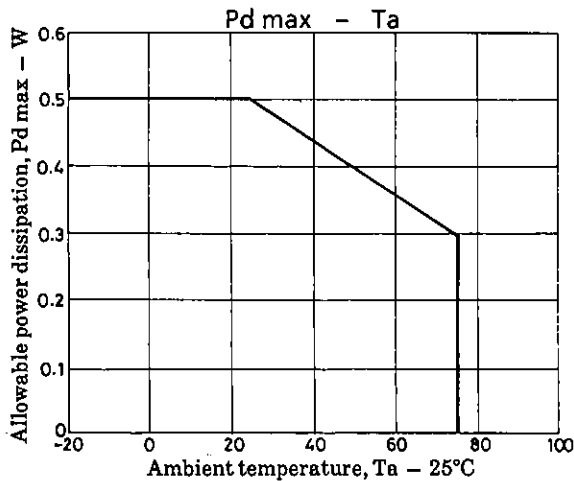
Pin Assignment (top view)



Block Diagram



AG1389



Pin Functions

Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
3	V_S	$< V_{CC2}$		Power supply input that determines the output amplitude. It must be set to a voltage lower than V_{CC2} .
4	V_{CC2}	4 to 10 V		Power supply for power amplifier systems other than motor drive transistors. Power supply pin that provides voltage for blocks other than control blocks supplied by V_{CC1} .
5	V_{CC1}	4 to 6 V		Power supply that provides voltage for the Hall amplifier, the forward/reverse circuit, the FG amplifier, and the thermal shutdown circuit.
6	ST. BY	(H): 2.0 V max (L): 0.8 V min (When V_{CC1} is 5 V)	<p>A01401</p>	All circuits can be made inoperative either by connecting this pin to GND, or by leaving it open. In that state the supply current will be approximately 0 μ A. Hold at 2 V or higher during normal operation.
7	ANGLE		<p>A01402</p>	Connect a resistor between this pin and GND. Changing the value of this resistor will change the Hall input-output gain (motor waveform slope).
9 10	FG_{IN}^- FG_{IN}^+	0 V min 3.5 V max (When V_{CC1} is 5 V)	<p>A01403</p>	FG signal input pin
11	FG_{OUT1}		<p>A01404</p>	FG amplifier output pin

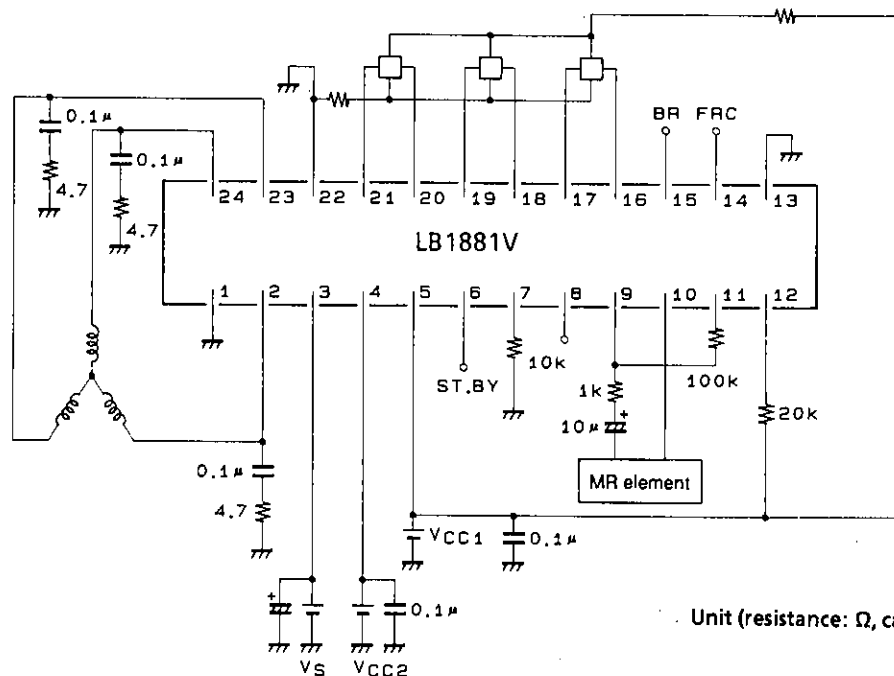
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Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
12	FG OUT2			FG Schmitt amplifier output pin
14	FRC	(H): 2.8 V min (L): 1.2 V max (When V_{CC1} is 5 V)		Pin for setting the motor to forward or reverse rotation Low level: Forward rotation (under 1.2 V: when V_{CC1} is 5 V) High level: Reverse rotation (over 2.8 V: when V_{CC1} is 5 V)
15	BR	(H): 2.0 V min (L): 0.8 V max		Motor brake pin Low level: Motor drive (under 0.8 V) High level: Motor brake (over 2.0 V)
16 17 18 19 20 21	W_{IN2} W_{IN1} V_{IN2} V_{IN1} U_{IN2} U_{IN1}	1.4 V min 2.8 V max (When V_{CC1} is 5 V)		W phase Hall element input pins. Logic high is defined to be states where $W_{IN1} > W_{IN2}$. V phase Hall element input pins. Logic high is defined to be states where $V_{IN1} > V_{IN2}$. U phase Hall element input pins. Logic high is defined to be states where $U_{IN1} > U_{IN2}$.
22	R_f			Output transistor GND
23 24 2	U_{OUT} V_{OUT} W_{OUT}			Output pin
1 13	SUBGND GND			GND for all circuits other than output transistors.

Application Circuit Example



A01410

Logic Value Table

	Source	Sink	Input			Forward/reverse control F/RC
			U	V	W	
1	W phase → V phase		H	H	L	L
	V phase → W phase		H	H	L	H
2	W phase → U phase		H	L	L	L
	U phase → W phase		H	L	L	H
3	V phase → W phase		L	L	H	L
	W phase → V phase		L	L	H	H
4	U phase → V phase		L	H	L	L
	V phase → U phase		L	H	L	H
5	V phase → U phase		H	L	H	L
	U phase → V phase		H	L	H	H
6	U phase → W phase		L	H	H	L
	W phase → U phase		L	H	H	H

Inputs:

High: For each phase, the input 1 potential is at least 0.2 V higher than the input 2 potential.

Low: For each phase, the input 1 potential is at least 0.2 V lower than the input 2 potential.

Forward/reverse control:

High: 2.8 V to V_{CC1}

Low: 0 to 1.2 V