Ordering number: EN 3438A

CMOS LSI

SANYO No. 3438A

# LC65404A

(A/D Converter, FLT drivers, PWM Output, and On-chip 4Kbyte ROM)

## 4-bit Single Chip Microcomputer for Control Applications

The LC65404A is a 52-pin CMOS 4-bit single chip microcomputer. It consists of a high-speed core CPU with the minimum cycle time = 0.92μF, 8-bit AD converter with 8 input channels, 4Kbyte ROM and a 1Kbit RAM (256 x 4 bits).

The LC65404A has a total of 41 input/output (I/O) port pins; 29 for high withstand outputs (Drivers for fluorescent display tubes and LEDs), and 12 for input/output (including the alternative pins to interrupt inputs and serial input).

In addition, this single-chip microcomputer has a two-channel timer. This timer circuit block can be used as a general-purpose timer, watchdog timer, time base timer, PWM type DA converter, melody tone generator and the like within application products. It is designed based on various standby operation modes. As a result, the LC65404A microcomputer can be embedded into many kinds of home appliances as, for example, display control and timer control in audio visual products.

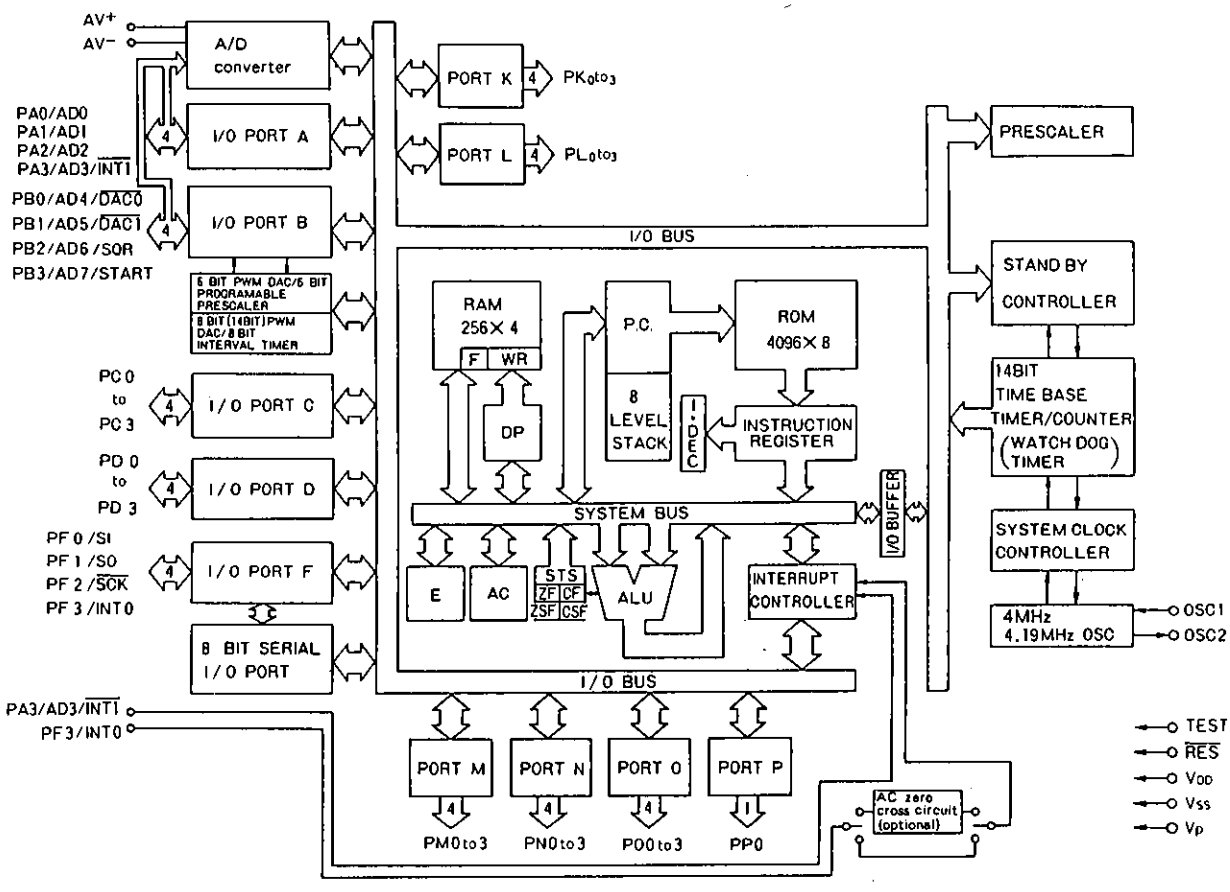
There is another microcomputer with almost all the LC65404A functions but oscillation circuit design and ambient operating temperature range. Its chip name is LC65204A. This single chip device has a subclock function and its operating temperature range is from minus 30 °C (-30) to plus 70 °C (+70). For detailed information, refer to its catalog. Note that the LC65404A should be used with the X1 pin connected to the $V_{DD}$ and the X2 pin left open.

**Features:**

- Seventy-seven instructions
- On-chip storage capacity; 4Kbyte ROM and 1Kbit (256 x 4 bits) RAM
- Minimum instruction cycle time: 0.92μs (4.33MHz at $V_{DD}$ = 4.5V or greater)
  1.84μs (2.17MHz at $V_{DD}$ = 4.0V or greater)
- Reduced power dissipation mode through system clock selection by software
  - Main system clock = 4.19MHz : 0.95μs, 1.9μs and 30.6μs
- Operating temperature: Ta = -30 °C to +85 °C
- Working register/Flag function
  - (16 flags + 8 working registers ) x 4 banks
- Stacks : 8 levels
- I/O ports : 41 (Total)
  - High-voltage withstand output ports : 21
  - High-voltage withstand input/output ports : 8
  - Medium-voltage withstand input/output ports : 3
  - Input/output ports : 9
- AD converter (sequential comparison type)
  - 8-bit Accuracy x 8 channels
- Timer : 2 channels
  - Timer 1 (interval timer) : Also used as the PWM DAC and applicable to a divider at melody tone generation.
  - Time base timer for clock generation : 14-level divider on-chipped
- PWM DAC output : Also used as timer 1.
  - 6-bit PWM DAC + 8-bit PWM DAC or 14-bit PWM DAC
- Serial input/output interface (LSB first)
  - 8-bit input/output
- AC zero cross detection circuit
  - The AC zero cross detection circuit is allowed to be internally connected to the PF3/INT0 pin through option data specification.

- Interrupt function: 5 interrupt sources and 4 vector addresses
  - External interrupt sources: 2
  - Timer interrupt sources: 2
  - Serial input/output interrupt source: 1
- On-chip oscillation stabilization period wait function: Effective at the reset.
- Oscillation circuit: 1 type
  - Main clock: 4.19MHz Crystal oscillation or 4.0MHz Ceramic oscillation
- Standby function: two modes; HALT mode and HOLD mode
- Supply voltage: 3.0V to 6.0V
- Package: DIP-52S
- Evaluation Tools: LC65999 (evaluation chip) + EVA800/850-TB651XX/2XX/3XX/4XX
  LC65PG20X/40X (piggyback)

**System Block Diagram**



**Development Support**

The development support tools for the LC65404A are as follows:

(1) User's Manual
[LC65204A/404A User's Manual]

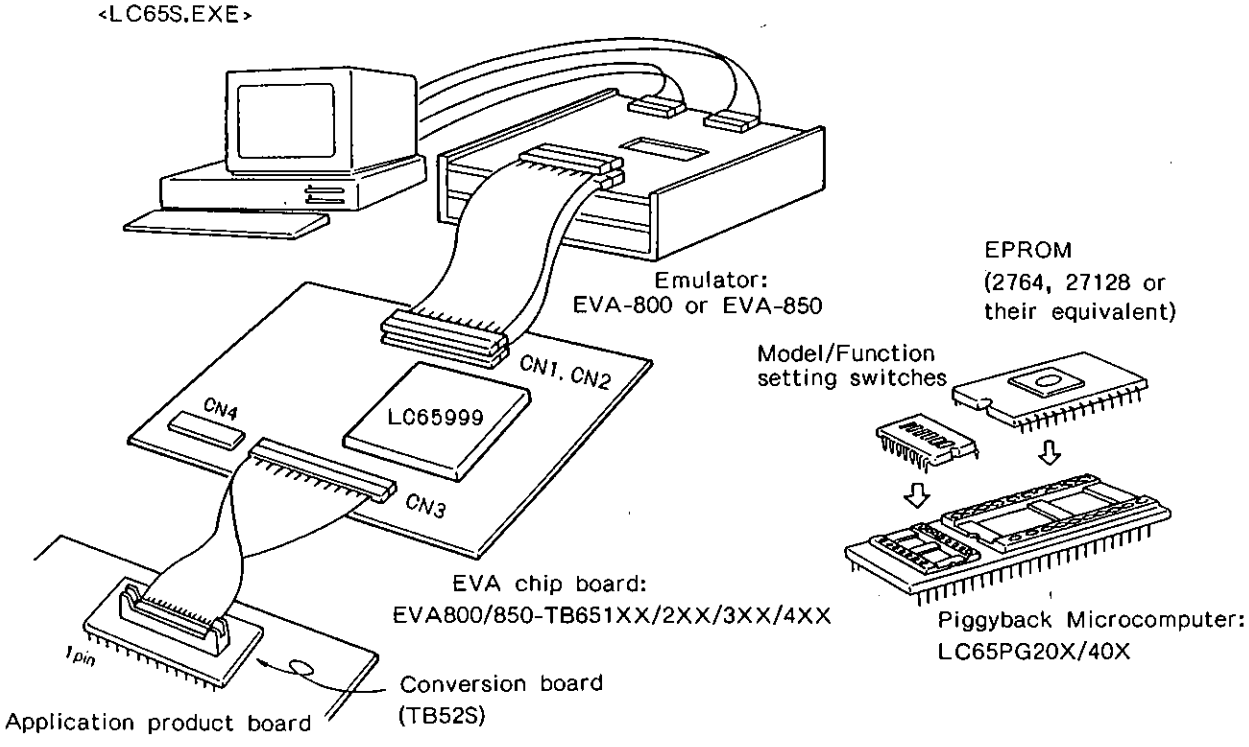
(2) Development Tool Manual
[EVA800/850-LC651XX/2XX/3XX/4XX Development Tool Manual]

(3) Development Tools

3-1. Program development tools
- i. MS-DOS Host Computer System and Cross Assembler (note 1)
- ii. Cross Assembler --- MS-DOS-based Cross Assembler : LC65S.EXE

3-2. Program evaluation tools
- i. Evaluation Chip: LC65999
- ii. Piggyback Microcomputer : LC65PG20X/40X
- iii. Emulator : EVA-800 main unit and EVA chip board, or EVA-850 main unit and EVA chip board (note 2)

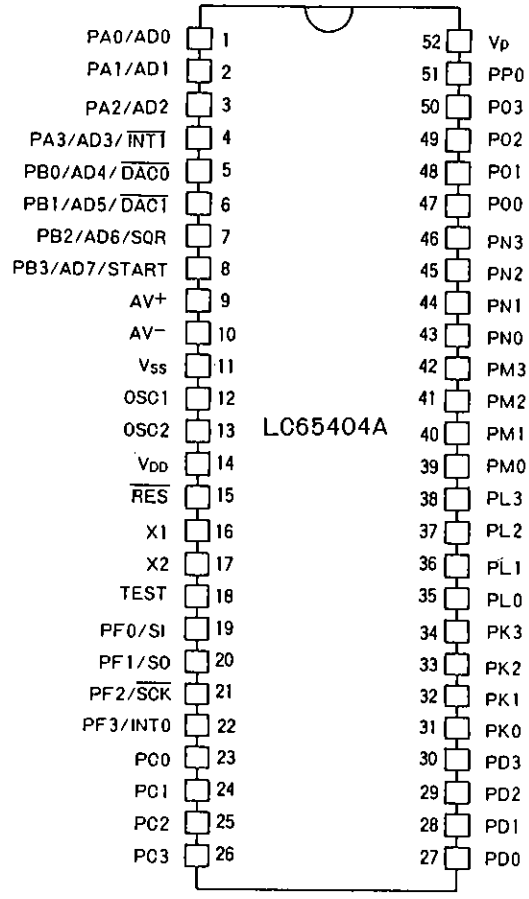
**Outline of the Development Support System**




(Note 1) MS-DOS: A trademark of Microsoft Corporation.

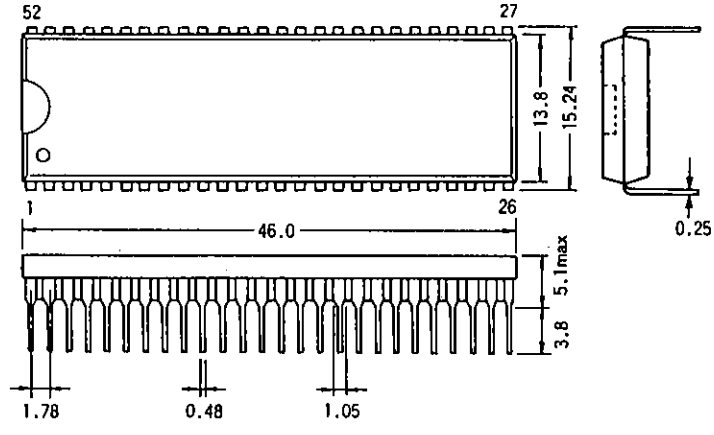
(Note 2) The EVA-800 and EVA-850 are general names given to emulators. They are qualified with suffixes (A, B, ...) because the emulators are updated very often. So use the latest version of the emulators by checking the suffixes carefully prior to program debug.

**LC65404A Pin Assignment**




## Package Dimensions : 3128

(unit: mm)




SANYO : DIP52S

**Pin Description**

| Pin Name | No.Of Pins | I/O | Functional Description | Output Driver | Option | Reset Status | Unused Pin Handling |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1 | — | Power supply pin | — | — | — | — |
| $V_{SS}$ | 1 | — | | | | | |
| TEST | 1 | I | LSI test pin. This pin should be connected to the Vss pin during operation and has an internal pull-down resistor. | — | — | — | Always connected to the $V_{SS}$ pin. |
| $\overline{RES}$ | 1 | I | System reset input. This pin has an internal pull-up resistor. | — | — | — | — |
| $AV^+$ | 1 | — | Reference voltage input pin for A/D conversion | — | — | — | Always connected to the $V_{SS}$ pin. |
| $AV^-$ | 1 | — | | | | | |
| OSC1 | 1 | I | Oscillation circuit component pins for system main clock generation. If external clock input is used, leave the OSC2 pin open and connect the external clock generator to the OSC1 pin. Feed-back resistor is internally provided. | — | — | — | — |
| OSC2 | 1 | O | | | | | |
| X1 | 1 | I | Unusable. Always leave the X2 pin Open and connect the X1 pin to the $V_{DD}$. | — | — | — | X1: connected to the VDD pin. X2: left OPEN. |
| X2 | 1 | O | | | | | |
| Vp | 1 | — | Load power for FLT output internal pull-down resistor | — | — | — | Connected to the $V_{DD}$ pin. |
| PA0 to 3 | 4 | I/O | Input/output port pins PA0 to PA3<br>- Port function<br>4-bit data input (IP instruction)<br>4-bit data output (OP instruction)<br>1-bit input decide operation (BP/BNP instruction)<br>1-bit output set and reset operations (SPB and RPB instructions)<br>- Low-level threshold input<br>- All these four port pins can be used for two or more purposes:<br>PA0/AD0:<br>Also used as AD converter input pin AD0<br>PA1/AD1:<br>Also used as AD converter input pin AD1<br>PA2/AD2:<br>Also used as AD converter input pin AD2<br>PA3/AD3/$\overline{INT1}$:<br>Also used as AD converter input pin AD3 and as external interrupt signal input pin $\overline{INT1}$ | Normal-voltage withstand Medium-level current type | Each port pin can be set to output type (1) or (2):<br>(1) Open Drain (OD) output<br>(2) Pull-up resistor output | Output transistor OFF (H-level output) | Should be set to the open drain output type and then connected to the $V_{SS}$ pin. |
| PB0 to 3 | 4 | I/O | Input/output port pins PB0 to PB3<br>- These port pins have the same function as port pins PA0 to PA3.<br>- Low-level threshold input<br>- All these four port pins can be used for two or more purposes:<br>PB0/AD4/$\overline{DAC0}$:<br>Also used as AD converter input pin AD4 and 6-bit PWM output pin $\overline{DAC0}$<br>PB1/AD5/$\overline{DAC1}$:<br>Also used as AD converter input pin AD5 and 8-/14-bit PWM output pin $\overline{DAC1}$<br>PB2/AD6/SQR:<br>Also used as AD converter input pin AD6 and square waveform signal output pin SQR.<br>PB3/AD7/START:<br>Also used as AD converter input pin AD7 and standby control input pin START | Same as PA0 to PA3 | Same as PA0 to PA3 | Same as PA0 to PA3 | Same as PA0 to PA3. |

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| Pin Name | No.Of Pins | I/O | Functional Description | Output Driver | Option | Reset Status | Unused Pin Handling |
|---|---|---|---|---|---|---|---|
| PC0to3 | 4 | I/O | Input/output port pins PC0 to PC3<br>- Same as port pins PA0 to PA3 in function.<br>- High-level threshold input<br>- The output level of these four port pins can be set to 'H' or 'L' by option data at the same time.<br>- FLT segment drive output | VDD-45V High-voltage withstand Medium current type | The output type of each port pin can be set to either (1) or (2) by option data.<br>(1) Open Drain (OD) output<br>(2) Pull-down resistor output<br>Output level specification option: The output level of all the four port pins can be simultaneously set to 'H' or 'L' at the reset by option data. | The output level at the reset can be set to 'H' or 'L' by option data. | Set the pin(s) to the open drain output type by option data and then connect it (or them) to the Vss pin through the resistance of some kohms. In addition, be sure to set the port output level at the reset to 'L'. |
| PD0to3 | 4 | I/O | Input/output port pins PD0 to PD3<br>- Same as port pins PA0 to PA3 in function and characteristic. | Same as port pins PC0 to PC3 | Same as port pins PC0 to PC3 | Same as port pins PC0 to PC3 | Same as port pins PC0 to PC3 |
| PF0to3 | 4 | I/O | Input/output port pins PF0 to PF3<br>- Same as port pins PA0 to PA3 in function.<br>- Schmitt input<br>- All these four port pins can be used for two purposes:<br>PF0/SI:<br>Also used as 8-bit serial input pin SI.<br>PF1/SO:<br>Also used as 8-bit serial output pin SO.<br>PF2/$\overline{SCK}$ :<br>Also used as 8-bit serial clock pin $\overline{SCK}$<br>PF3/INT0:<br>Also used as external interrupt request input INT0. The AC zero cross detection circuit can be internally added to this pin by option data (AC zero cross interrupt function available). | PF0 to PF2 Open Drain (OD) output type: Withstand voltage +15V Pull-up output type: Normal-voltage withstand PF3 Normal-voltage withstand Medium current type | (1) Output type option: Same as port pins PA0 to PA3.<br>(2) The AC zero cross detection circuit can be internally added to the INT0 pin by option data. | Same as port pins PA0 to PA3 | Set the pin(s) to the open drain output type by option data and then connect it (or them) to the Vss pin. |
| PK0to3 | 4 | O | Output port pins PK0 to PK3<br>- Port functions<br>4-bit data output (OP Instruction)<br>1-bit set and reset operation (SPB and RPB instructions)<br>1-bit decide operation (BP and BNP instructions)<br>- FLT segment drive output | Same as port pins PC0 to PC3 | The output type of each port pin can be set to either (1) or (2).<br>(1) Open Drain (OD) output<br>(2) Pull-down resistor output | Output transistor OFF ('L' level output) | Set the pin(s) to the open drain output type by option data and then connect it (or them) to the VDD pin |
| PL0to3 | 4 | O | Output port pins PL0 to PL3<br>- Same as port pins PK0 to PK3 in function.<br>- FLT digit drive output | VDD-45V High-voltage withstand Large current type | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 |
| PM0to3 | 4 | O | Output port pins PM0 to PM3.<br>- Same as port pins PL0 to PL3 in function and characteristic | Same as port pins PL0 to PL3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 |
| PN0to3 | 4 | O | Output port pins PN0 to PN3.<br>- Same as port pins PL0 to PL3 in function and characteristic | Same as port pins PL0 to PL3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 |
| PO0to3 | 4 | O | Output port pins PO0 to PO3.<br>- Same as port pins PL0 to PL3 in function and characteristic | Same as port pins PL0 to PL3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 |
| PP0 | 1 | O | Output port pin PP0<br>- Same as port pins PL0 to PL3 except for 1-bit configuration. | Same as port pins PL0 to PL3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 | Same as port pins PK0 to PK3 |

User Option types

1) Oscillation circuit options

The main clock oscillation circuit and the sub clock oscillation circuit can be selected from the following optional circuits:

| Option name | Optional oscillation circuit |
|---|---|
| Main clock oscillation circuit | Two-pin CF oscillation circuit |
| | Two-pin X'tal (crystal) oscillation circuit |
| | External clock input |
| Sub clock oscillation circuit | Unused |

2) Output level option

This option is provided to set the output level of input/output ports C and D to either 'H' or 'L' at the reset. This sets the output level of the four pins at the same time.

| Option name | Conditions |
|---|---|
| 1. 'H' level output at the reset | Simultaneous 4-bit setting (input/output ports C and D) |
| 2. 'L' level output at the reset | Simultaneous 4-bit setting (input/output ports C and D) |

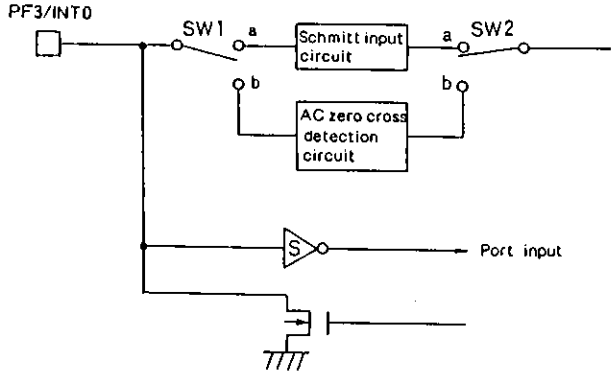
3. Watchdog reset option

The watchdog reset option is used to select the watchdog reset function. Note that the watchdog reset function utilizes the time base timer.

| Option name | Conditions |
|---|---|
| 1. Watchdog reset function select | An additional program routine is required in order for the time base interrupt request flag to be reset at a certain interval. This prevents the watchdog reset circuit from being activated in cases but a program upset. |
| 2. Watchdog reset function non-select | —— |

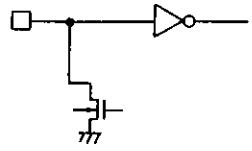
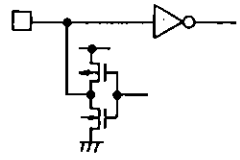
4) AC zero cross detection input circuit option

The AC zero cross detection input circuit option is used to permit the INT0 pin to internally have an AC zero cross detection circuit or Schmitt input circuit.

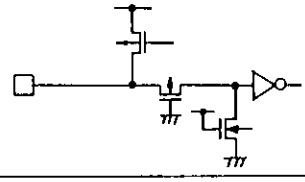
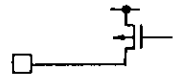
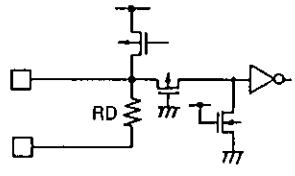
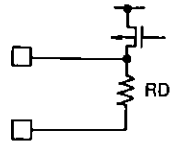



| SW / Option name | SW1 | SW2 |
|---|---|---|
| INT0 input | a | a |
| AC zero cross input | b | b |

5) Normal-voltage withstand/Medium-voltage withstand port output type option
This user option is used to allow the output circuit type of each normal-voltage withstand and medium-voltage input/output port pin to be set to either the open drain output or the pull-up resistor output (bit-by-bit setting only).

| Option name | Circuit type | Applied ports |
|---|---|---|
| Open Drain (OD) output |  | Ports A, B and F |
| Pull-up resistor output |  | Ports A, B and F |

6) High-voltage withstand port output type option
This user option is used to allow the output circuit type of each high-voltage input/output and high-voltage output port pin to either the open drain output or the pull-down resistor output (bit-by-bit setting only).

| Option name | Circuit type | Applied ports |
|---|---|---|
| Open Drain (OD) output |  | Ports C and D |
| |  | Ports K, L, M, N, O and P |
| Pull-down resistor output |  | Ports C and D |
| |  | Ports K, L, M, N, O and P |

## Major LC65404A Characteristics

1. Absolute Maximum Ratings at Ta = 25 °C, Vss = 0V

| Parameter | Symbol | Applied Pins and Remarks | Conditions | $V_{DD}$(V) | Limits | Unit |
|---|---|---|---|---|---|---|
| Maximum Supply Voltage | $V_{DD}$ max | $V_{DD}$ | | | −0.3 to +7.0 | V |
| Input Voltage | $V_I$(1) | OSC1 | At self-oscillation | | Up to the voltage produced | |
| | $V_I$(2) | TEST, $\overline{RES}$, OSC1 | OSC1: at external clock input | | −0.3 to $V_{DD}$+0.3 | |
| | $V_I$(3) | AV+ | | | −0.3 to $V_{DD}$+0.3 | |
| | $V_I$(4) | AV− | | | −0.3 to $V_{DD}$+0.3 | |
| | $V_I$(5) | Vp | | | $V_{DD}$−45 to $V_{DD}$+0.3 | |
| Output Voltage | $V_O$(1) | OSC2 | At self-oscillation | | Up to the voltage produced | |
| | $V_O$(2) | Ports K, L, M, N, O and port pin P0 | | | $V_{DD}$−45 to $V_{DD}$+0.3 | |
| Input/output Voltage | $V_{IO}$(1) | Port pins F2 to F0 | At open drain output | | −0.3 to +15 | |
| | $V_{IO}$(2) | Port pins F2 to F0 | At pull-up resistor output | | −0.3 to $V_{DD}$+0.3 | |
| | $V_{IO}$(3) | Ports C and D | | | $V_{DD}$−45 to $V_{DD}$+0.3 | |
| | $V_{IO}$(4) | Ports A and B port pin F3 | | | −0.3 to $V_{DD}$+0.3 | |
| Peak Output Current | $I_{OP}$(1) | Ports A, B, and F | | | −2 to +10 | mA |
| | $I_{OP}$(2) | Ports L, M, N, O and port pin P0 | | | −30 to 0 | |
| | $I_{OP}$(3) | Ports C, D and K | | | −10 to 0 | |
| Average Output Current | $I_{OA}$(1) | Ports A, B, and F | Average value per pin for 100ms | | −2 to +10 | |
| | $I_{OA}$(2) | Ports L, M, N, O and port pin P0 | | | −30 to 0 | |
| | $I_{OA}$(3) | Ports C, D, and K | | | −10 to 0 | |
| | $\Sigma I_{OA}$(1) | Ports A and B | Total current value of all pins for 100ms | | −16 to +80 | |
| | $\Sigma I_{OA}$(2) | Port F | | | −8 to +40 | |
| | $\Sigma I_{OA}$(3) | Ports L, M, N, O and port pin P0 | | | −50 to 0 | |
| | $\Sigma I_{OA}$(4) | Ports C, D and K | | | −50 to 0 | |
| Maximum Power Dissipation | Pd max | DIP52S | Ta=−30 to +85°C | | 580 | mW |
| Ambient Operating Temperature | Topr | | | | −30 to +85 | °C |
| Ambient Storage Temperature | Tstg | | | | −55 to +125 | |

2. Allowable Operating Range at Ta = -30 °C to +85 °C, Vss = 0V

| Parameter | Symbol | Applied Pins and Remarks | Conditions | $V_{DD}$(V) | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Operating Power Supply Voltage (including a standby mode) | $V_{DD}$(1) | $V_{DD}$ | 0.92μs ≦ Tcyc < 36μs | | 4.5 | | 6.0 | V |
| | $V_{DD}$(2) | $V_{DD}$ | 1.84μs ≦ Tcyc < 36μs | | 4.0 | | 6.0 | |
| | $V_{DD}$(3) | $V_{DD}$ | 29.4μs ≦ Tcyc < 36μs | | 3.0 | | 6.0 | |
| Memory backed-up Power Supply Voltage | $V_{ST}$ | $V_{DD}$ | Full standby mode (HOLD mode) | | 1.8 | | 6.0 | V |

To be continued on the next page.

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Allowable Operating Range at Ta = -30 °C to +85 °C, Vss = 0V

| Parameter | | Symbol | Applied Pins and Remarks | Conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$(V) | Min | Typ | Max | |
| Input 'H'-level Voltage | | $V_{IH}$(1) | OD type port pins F2 to F0 | Output Nch (N-channel) Tr.(translstor)OFF | 3.0to6.0 | 0.80$V_{DD}$ | | 13.5 | V |
| | | $V_{IH}$(2) | PU type port pins F2 to F0 | Output Nch Tr. OFF | 3.0to6.0 | 0.80$V_{DD}$ | | $V_{DD}$ | |
| | | $V_{IH}$(3) | Ports A and B | Output Nch Tr. OFF | 3.0to6.0 | 1.9 | | $V_{DD}$ | |
| | | $V_{IH}$(4) | Ports C and D | Output Nch Tr. OFF | 4.5to6.0 | 0.80$V_{DD}$ | | $V_{DD}$ | |
| | | | | | 3.0to6.0 | 0.85$V_{DD}$ | | $V_{DD}$ | |
| | | $V_{IH}$(5) | OSC1, START, PF3/ INT0, $\overline{INT1}$ (Note 1) | See Fig. 3 (applies to OSC1 only). Output Nch Tr. OFF (applies to other pins than OSC1). | 3.0to6.0 | 0.80$V_{DD}$ | | $V_{DD}$ | |
| | | $V_{IH}$(6) | $\overline{RES}$ | | 1.8to6.0 | 0.80$V_{DD}$ | | $V_{DD}$ | |
| Input 'L'-level Voltage | | $V_{IL}$(1) | Port pins F2 to F0 | Output Nch Tr. OFF | 3.0to6.0 | Vss | | 0.20$V_{DD}$ | V |
| | | $V_{IL}$(2) | Ports A and B | Output Nch Tr. OFF | 4.5to6.0 | Vss | | 0.5 | |
| | | | | | 3.0to6.0 | Vss | | 0.35 | |
| | | $V_{IL}$(3) | Ports C and D | Output Nch Tr. OFF | 3.0to6.0 | Vss | | 0.40$V_{DD}$ | |
| | | $V_{IL}$(4) | TEST | | 4.5to6.0 | Vss | | 0.30$V_{DD}$ | |
| | | | | | 3.0to6.0 | Vss | | 0.25$V_{DD}$ | |
| | | $V_{IL}$(5) | OSC1, $\overline{RES}$, PF3/ INT0, $\overline{INT1}$ (Note 1) | See Fig. 3 (applies to OSC1 only). Output Nch Tr. OFF (applies to other pins than OSC1). | 3.0to6.0 | Vss | | 0.20$V_{DD}$ | |
| | | $V_{IL}$(6) | START | | 1.8to6.0 | Vss | | 0.20$V_{DD}$ | |
| Instruction Cycle Time | | Tcyc | | (Note 2) | (Note 2) | 0.92 | | 36 | μs |
| Main Clock External Input Conditions | Frequency | Fxosc | OSC1 | (Note 2) | 3.0to6.0 | 3.6 | | 4.33 | MHz |
| | Pulse Width | Twoscch Twosccl | | See Fig. 3 | 4.5to6.0 | 70 | | | ns |
| | | | | | 3.0to6.0 | 140 | | | |
| | Rise and Fall Times | Toscr Toscf | | See Fig. 3 | 3.0to6.0 | | | 30 | ns |

(Note 1) This does not apply to the case where the AC zero cross detection circuit has been internally added to the INT0 pin by the user option data.

(Note 2) Frequencies are closely related to power supply voltages and instruction cycle times. So they should be studied in connection with supply voltages and cycle times.

3. Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

| Parameter | Symbol | Applied Pins and Remarks | Conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$(V) | Min | Typ | Max | |
| Input 'H'-level Current | $I_{IH}$(1) | OD type port pins F2 to F0 | Output Nch (N channel) Tr. (transistor) OFF (including Nch Tr. OFF leakage current). Vin=+13.5V | 3.0to6.0 | | | +5.0 | μA |
| | $I_{IH}$(2) | OD type ports A and B, and OD type port pin F3 (including multi-functional port pins INT0, $\overline{INT1}$ and START) (Note 1) | Output Nch (N channel) Tr. (transistor) OFF (including Nch Tr. OFF leakage current). Vin=$V_{DD}$ | 3.0to6.0 | | | +1.0 | |
| | $I_{IH}$(3) | $\overline{RES}$ | Vin=$V_{DD}$ | 3.0to6.0 | | | +1.0 | |
| | $I_{IH}$(4) | OSC1 | Vin=$V_{DD}$ | 3.0to6.0 | | | +10 | |
| | $I_{IH}$(5) | OD type ports C and D | Output Pch Tr OFF. Vin = $V_{DD}$ | 3.0to6.0 | | +30 | +100 | |
| Input 'L'-level Current | $I_{IL}$(1) | OD type ports A, B and F (including multi-functional port pins INT0, $\overline{INT1}$ and START) (Note 1) | Output Nch Tr. OFF. Vin = Vss | 3.0to6.0 | −1.0 | | | μA |
| | $I_{IL}$(2) | PU type ports A, B and F (including multi-functional port pins INT0, $\overline{INT1}$ and START) (Note 1) | Output Nch Tr. OFF. Vin = Vss | 3.0to6.0 | −1.0 | −0.5 | | mA |
| | $I_{IL}$(3) | $\overline{RES}$ | Vin=Vss | 3.0to6.0 | −60 | −25 | | μA |
| | $I_{IL}$(4) | OSC1 | Vin=Vss | 3.0to6.0 | −10 | | | |
| | $I_{IL}$(5) | OD type ports C and D | Output Pch (P channel) Tr. (transistor) OFF (including Pch Tr. OFF leakage current). Vout = $V_{DD}$ - 40V | 3.0to6.0 | −30 | | | |
| Output 'H'-level Voltage | $V_{OH}$(1) | PU type ports A, B and F | $I_{OH}$=−50μA | 4.5to6.0 | $V_{DD}$−1.2 | | | V |
| | $V_{OH}$(2) | PU type ports A, B and F | $I_{OH}$=−10μA | 3.0to6.0 | $V_{DD}$−0.5 | | | |
| | $V_{OH}$(3) | Ports L, M, N and O, and port pin P0 | $I_{OH}$=−20mA | 4.5to6.0 | $V_{DD}$−2.1 | | | |
| | $V_{OH}$(4) | Ports L, M, N and O, and port pin P0 | $I_{OH}$=−1.0mA $I_{OH}$s of other ports < -1mA | 3.0to6.0 | $V_{DD}$−1.0 | | | |
| | $V_{OH}$(5) | Ports C, D and K | $I_{OH}$=−5 mA | 4.5to6.0 | $V_{DD}$−1.8 | | | |
| | $V_{OH}$(6) | Ports C, D and K | $I_{OH}$=−1.0mA $I_{OH}$s of other ports < -1mA | 3.0to6.0 | $V_{DD}$−1.0 | | | |
| Output 'L'-level Voltage | $V_{OL}$(1) | Ports A, B and F | $I_{OL}$=5 mA | 4.5to6.0 | | | 1.5 | V |
| | $V_{OL}$(2) | Ports A, B and F | $I_{OL}$=1.0mA $I_{OL}$s of other ports < 1mA | 3.0to6.0 | | | 0.5 | |

To be continued on the next page.

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Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

| Parameter | | | Symbol | Applied Pins and Remarks | Conditions | VDD(V) | Limits Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output 'L'-level Current (the current produced by pull-down resistors) | | | IOL | PD type ports C, D, K, L, M, N and O, and PD type port pin P0 | Output Pch (P channel) Tr. (transistor) OFF Vout=3.0V Vp=−35V | 5.0 | 190 | 362 | 844 | μA |
| Output OFF Leakage Current | | | Ioff(1) | OD type ports K, L, M, N and O, and OD type port pin P0 | Output Pch (P channel) Tr. (transistor) OFF Vout=VDD | 3.0to6.0 | | | 30 | μA |
| | | | Ioff(2) | OD type ports K, L, M, N and O, and OD type port pin P0 | Output Pch (P channel) Tr. (transistor) OFF Vout=VDD−40V | 3.0to6.0 | −30 | | | |
| Pull-up MOS Tr. Resistance | | | Rtru | PU type ports A, B and F | Output Nch (N channel) Tr. (transistor) OFF VIN=0V | 5.0 | 8 | 12 | 30 | kΩ |
| Pull-up resistor | | | Ru | $\overline{RES}$ | VIN=0V | 5.0 | 100 | | 400 | kΩ |
| Pull-down resistor | | | Rd | PD type ports C, D, K, L, M, N and O, and PD type port pin P0 | Output Pch (P channel) Tr. (transistor) OFF Vout=3.0V Vp=−35V | 5.0 | 45 | 105 | 200 | kΩ |
| Hysteresis Voltage | | | VHYS | Port F and port pins INT0, $\overline{INT1}$ $\overline{RES}$ and START (Note 1) | | 3.0to6.0 | | 0.1VDD | | V |
| Serial Clock | Input Clock Cycle | | TCKCY(1) | $\overline{SCK}$ | See Figure 5. | 4.0to6.0 | 0.8 | | | μs |
| | Output Clock Cycle | | TCKCY(2) | $\overline{SCK}$ | See Figure 5. | 4.0to6.0 | 2.0× TCYC | | | |
| | Input Clock 'L'-level Pulse Width (Note 5) | | TCKL(1) | $\overline{SCK}$ | See Figure 5. | 4.0to6.0 | 0.3 | | | |
| | Output Clock 'L'- level Pulse Width | | TCKL(2) | $\overline{SCK}$ | See Figure 5. | 4.0to6.0 | TCYC | | | |
| | Input Clock 'H'-level Pulse Width (Note 5) | | TCKH(1) | $\overline{SCK}$ | See Figure 5. | 4.0to6.0 | 0.3 | | | |
| | Output Clock 'H'-level Pulse Width | | TCKH(2) | $\overline{SCK}$ | See Figure 5. | 4.0to6.0 | TCYC | | | |
| Serial Input | Data Setup Time | | TICK | SI | With reference to the rising edge of the $\overline{SCK}$ signal See Fig. 5. | 4.0to6.0 | 0.2 | | | |
| | Data Hold Time | | TCKI | SI | | 4.0to6.0 | 0.2 | | | |
| Serial Output | Output Delay Time | | TCKO | SO | With reference to the falling edge of the SCK signal. External resistance: 1 kohm. External capacitance: 50pF. See Fig. 5. | 4.0to6.0 | | | 0.5 | |
| Main Clock Self-oscillation Conditions | Crystal Oscillation | Oscillation Frequency | foscx | OSC1 OSC2 (Note 3) | See Fig. 1. (Note 2) | 3.0to6.0 | | 4.19 | | MHz |
| | | Oscillation Stabilizing Period | tMXS | | See Fig. 2 | | | | 20 | ms |
| | Ceramic Oscillation | Oscillation Frequency | fOSCCF | | See Fig. 1. (Note 2) | | 3.92 | 4.0 | 4.08 | MHz |
| | | Oscillation Stabilizing Period | tMCFS | | See Fig. 3 | | | | 10 | ms |

(Note 3) For oscillation constants, refer to Tables 1.

To be continued on the next page.

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Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

| | Parameter | Symbol | Applied Pins and Remarks | Conditions | VDD(V) | Limits Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| AC Zero Cross Detection Input Characteristics | Input Frequency | FZIN | Apply to the case where the AC zero cross detection circuit has been internally added to the PF3/INT0 pin by the user option data. | ① At open drain output ② At self-bias ON ③ See Fig.7. | 4.5to6.0 | 40 | | 1000 | Hz |
| | Input Voltage | VZIN | | ①, ②, ③ Coupling capacitance = 1uF | | 1.0 | | 2.4 | Vp-p |
| | Detection Error | VZA | | ①, ②, ③ 60Hz sinewave signal input | | | | ±100 | mV |
| | Input Current | IIHZ | | ①, ②, ③ VIN=VDD | | | | +40 | μA |
| | | IILZ | | ①, ②, ③ VIN=VSS | | −40 | | | |
| | Threshold Voltage | Vt*ACM | | ①, ②, ③ | | 0.3VDD | | 0.7VDD | V |
| | 'L'-level Input Threshold Voltage | Vt*ACL | | ①, ②, ③ | | | VT*ACM −0.2 | | |
| Comparator Characteristics (with AD converter in comparator mode) | Comparison Accuracy | VCECON | AD0toAD7 | AV+=VDD AV−=VSS | 5.0 ±10% | | ±1 | ±2 | LSB |
| | Threshold Voltage | VTHCON | | | | AV− | | AV+ | V |
| | Input Voltage | VINCON | | | | AV− | | AV+ | |
| | Reference Input Voltage | AV+ | AV+ | | | AV− | | VDD | |
| | | AV− | AV− | | | VSS | | AV+ | |
| | Conversion Time | TCC | | Comparator speed 1/1. At 12 x TCYC. | | 11 (TCYC= 0.92μs) | | 96 (TCYC= 8μs) | μs |
| | | | | Comparator speed 1/2. At 23 x TCYC. | | 21 (TCYC= 0.92μs) | | 92 (TCYC= 4μs) | |
| AD Conversion Characteristics (AD converter in A/D mode) | Resolution | | | | 5.0 ±10% | | 8 | | Bit |
| | Absolute Accuracy | | | AV+=VDD AV−=VSS | | | ±1 | ±2 | LSB |
| | Zero Scale Error | EZS | | | | | | ±1 | |
| | Full Scale Error | EFS | | | | | | ±1 | |
| | Conversion Time | TCAD | | AD speed 1/1. At 26 x TCYC | | 24 (TCYC= 0.92μs) | | 208 (TCYC= 8μs) | μs |
| | | | | AD speed 1/2. At 51 x TCYC. | | 47 (TCYC= 0.92μs) | | 204 (TCYC= 4μs) | |
| | Reference Input Voltage | AV+ | AV+ | | | AV− | | VDD | V |
| | | AV− | AV− | | | VSS | | AV+ | |
| | Reference Input Current Range | IRIF | AV+, AV− | AV+=VDD AV−=VSS | | 75 | 150 | 300 | μA |
| | Analog Input Voltage Range | VAIN | AD0toAD7 | | | AV− | | AV+ | V |
| | Analog Port Input Current | IAIN | Port pins AD0 to AD7 (with the output circuit of the input/output multi-functional port pins set to OD type) | Including output OFF leakage current. VAIN=VDD | | | | 1 | μA |
| | | | | VAIN=VSS | | −1 | | | |

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Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

| Parameter | Symbol | Applied Pins and Remarks | Conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD(V) | Min | Typ | Max | |
| Dissipated Current in Normal Operation Mode (Note 4) | IDDOP(1) | VDD | 4.19MHz x 1/1: High-speed operation mode (TCYC = 0.95 µs). | 4.5to6.0 | | 3 | 6 | mA |
| | IDDOP(2) | VDD | 4.19MHz x 1/2: High-speed operation mode (TCYC = 1.9 µs). | 4.0to6.0 | | 2 | 4 | |
| | IDDOP(3) | VDD | 4.19MHz x 1/32: Low-speed operation mode (TCYC = 30.5 µs). | 3.0 | | 0.3 | 1 | |
| Dissipated Current in Standby Operation Mode (Note 4) | IDDST(1) | VDD | 4.19MHz main clock oscillation (HALT mode) | 6.0 | | 0.8 | 1.5 | mA |
| | IDDST(2) | VDD | | 3.0 | | 200 | 500 | µA |
| Dissipated current in Full standby operation mode (Note 4) | IDDST(3) | VDD | Full standby mode (HOLD mode) | 1.8 | | | 1 | |
| | IDDST(4) | VDD | Full standby mode (HOLD mode) | 6.0 | | | 10 | |

(Note 4) The 'dissipated current' does not include the current flowing into the I/O port transistors, pull-up/pull-down resistors.

(Note 5) When the internal clock is used, although according to the specifications TCKL(2) and TCKH(2)(=TCYC) are output from the $\overline{SCK}$ pin with the minimum clock width, there are cases where their clock widths become shorter than TCYC due to the value of the pull-up resistor. However, it is necessary to select a value for the pull-up resistor so that even at the minimum, these clock widths exceed the 0.3 µs stipulated for TCKL(1) and TCKH(1).

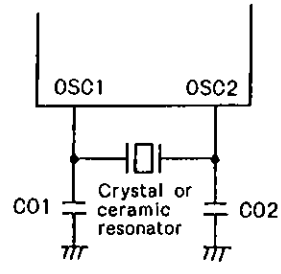



Fig. 1 Main clock oscillation circuit

Table 1. Guaranteed constants for Main clock oscillation

| Oscillation type | Supplier | Oscillator | CO1 | CO2 | |
|---|---|---|---|---|---|
| 4.194304MHz crystal osc | Kinseki | HC-49/U CL=13.2pF | 15pF | 15pF | |
| | Nippon Denpa | AT-51 CL=16pF | 22pF | 22pF | |
| 4.0MHz ceramic resonator osc | Murata | CSA4.00MG | 33pF | 33pF | |
| | | CST4.00MGW | Not required | Not required | *1 |
| | Kyocera | KBR-4.0MS | 33pF | 33pF | |
| | | KBR-4.0MES | Not required | Not required | *1 |

CO1 and CO2 tolerance: Within ±10% (including wire capacitance)
CL: Internal load capacitance of a crystal oscillator
*1: Three-pin (C internally provided) ceramic resonator

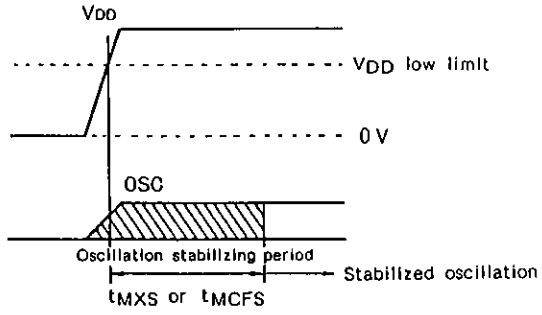



Fig. 2. Main clock oscillation stabilizing period

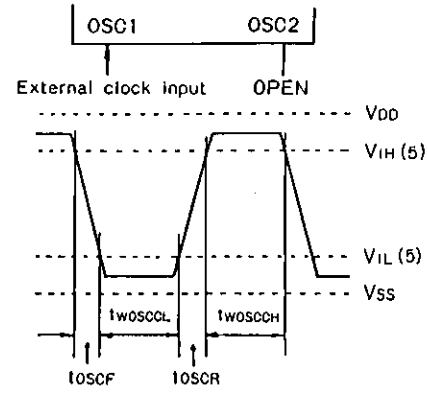
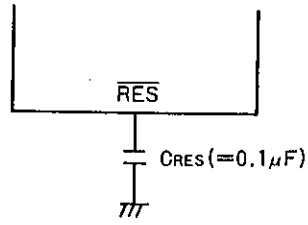


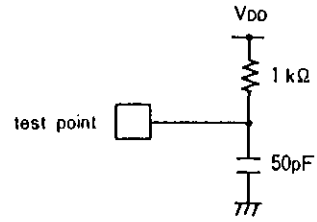

Fig.3. Input waveform of input clock (for main clock)




(Note)
If power stabilizing time is zero, the reset time will be 10ms to 100ms with the $C_{RES}$ = 0.1μF.

If the power stabilizing period is rather long, the $C_{RES}$ value should be set properly so that the reset time period can be longer than the main clock oscillation stabilizing period.

Fig. 4. Reset Circuit




Serial output load

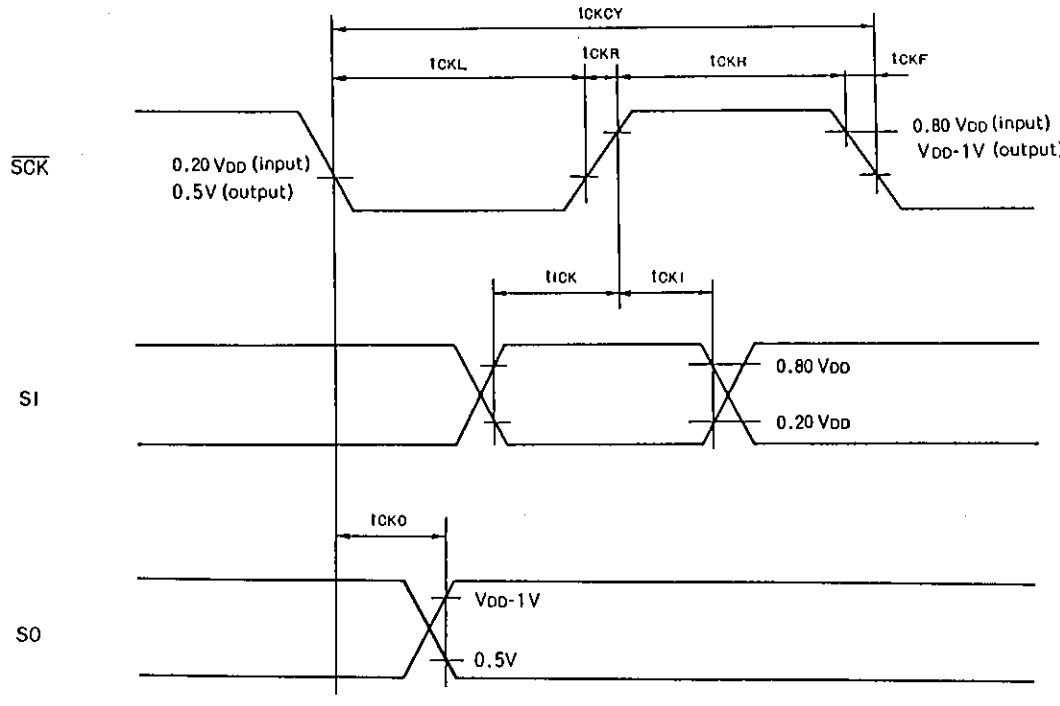
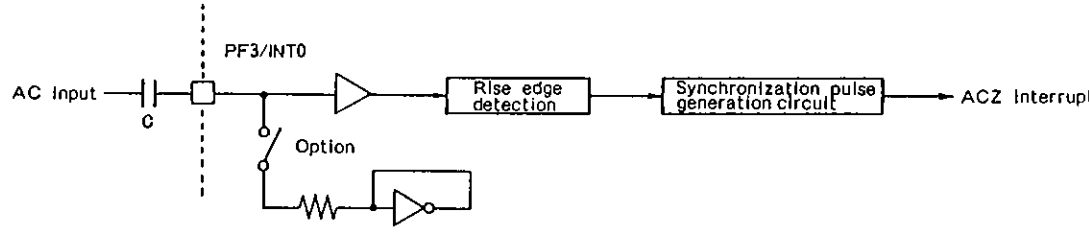
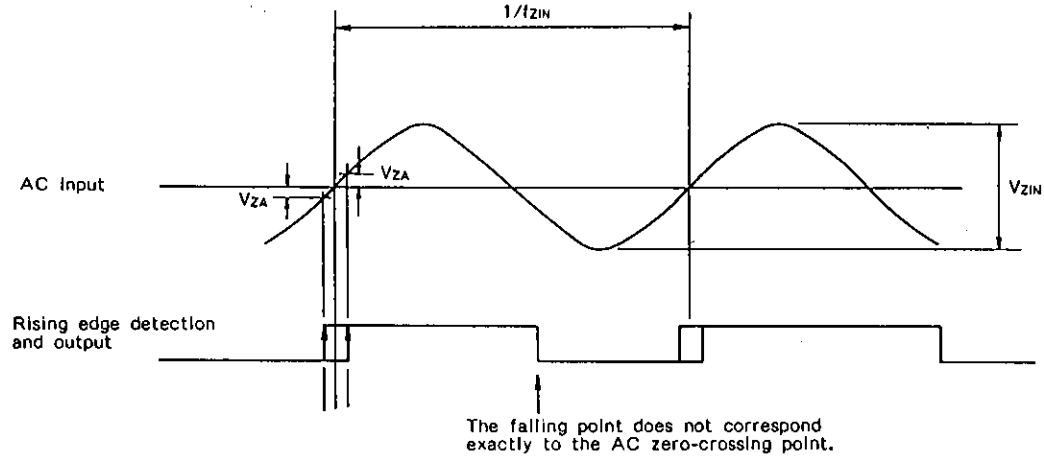



Fig. 5 Serial clock timing




<AC zero cross detection>




<AC zero cross timing>

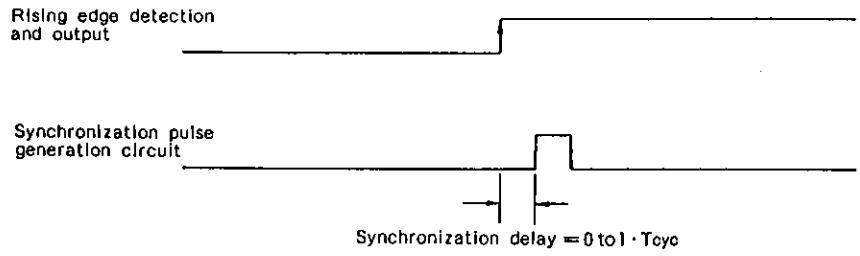



Fig. 6 AC zero cross detection

## LC65404A Instruciton Set (by Function)

Convention

| | | | |
|---|---|---|---|
| AC | : ACcumulator | PC | : Program Counter |
| ACt | : ACcumulator bit t | STACK | : STACK register |
| CF | : Carry Flag | bAt, bHa, | |
| CTL | : ConTroL register | bLa | : Working register |
| MSTEN | : MaSTerinterrupt ENable flag | ZF | : Zero Flag |
| DP | : Data Pointer | ( ) [ ] | : Indicates the content. |
| E | : E register | ← | : Transfer operation and its direction |
| bFn | : Flag bit n | + | : Addition |
| M | : Memory | - | : Subtraction |
| M (DP) | : Memory address specified by DP | ∧ | : And |
| P ($DP_L$) | : Input/output port specified by DPL | ∨ | : Or |
| GP (DP) | : Pseudo port specified by DP | ∀ | : Exclusive Or |

| Instruction group Type | Mnemonic | | Operation Code $D_7D_6D_5D_4$ | Operation Code $D_3D_2D_1D_0$ | Bytes | Cycles | Operations | Operating Description | Affected STS flag(s) | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| Accumulator Manipulation Instructions | CLA | Clear AC | 1 1 0 0 | 0 0 0 0 | 1 | 1 | AC ← 0 | Resets AC to 0. | ZF | * 1 |
| | CLC | Clear CF | 1 1 1 0 | 0 0 0 1 | 1 | 1 | CF ← 0 | Resets CF to 0. | CF | |
| | STC | Set CF | 1 1 1 1 | 0 0 0 1 | 1 | 1 | CF ← 1 | Sets CF to 1. | CF | |
| | CMA | Complement AC | 1 1 1 0 | 1 0 1 1 | 1 | 1 | AC ← $\overline{(AC)}$ | Inverts all AC bits. | ZF | |
| | INC | Increment AC | 0 0 0 0 | 1 1 1 0 | 1 | 1 | AC ← (AC) + 1 | Increments AC by 1. | ZF CF | |
| | DEC | Decrement AC | 0 0 0 0 | 1 1 1 1 | 1 | 1 | AC ← (AC) − 1 | Decrements AC by 1. | ZF CF | |
| | RAL | Rotate AC left through CF | 0 0 0 0 | 0 0 0 1 | 1 | 1 | $AC_0$ ← (CF), $AC_{n+1}$ ← $(AC_n)$, CF ← $(AC_3)$ | Rotates AC left through CF. | ZF CF | |
| | TAE | Transfer AC to E | 0 0 0 0 | 0 0 1 1 | 1 | 1 | E ← (AC) | Transfers AC to E. | | |
| | XAE | Exchange AC with E | 0 0 0 0 | 1 1 0 1 | 1 | 1 | (AC) ⇄ (E) | Exchange the contents of AC and E. | | |
| Memory Manipulation Instructions | INM | Increment M | 0 0 1 0 | 1 1 1 0 | 1 | 1 | M(DP) ← (M(DP)) + 1 | Increments M(DP) by 1. | ZF CF | |
| | DEM | Decrement M | 0 0 1 0 | 1 1 1 1 | 1 | 1 | M(DP) ← (M(DP)) − 1 | Decrements M(DP) by 1. | ZF CF | |
| | SMB bit | Set M data bit | 0 0 0 0 | 1 0 $B_1B_0$ | 1 | 1 | M(DP, $B_1B_0$) ← 1 | Sets the M(DP) bit specified by $B_1B_0$. | | |
| | RMB bit | Reset M data bit | 0 0 1 0 | 1 0 $B_1B_0$ | 1 | 1 | M(DP, $B_1B_0$) ← 0 | Resets the M(DP) bit specified by $B_1B_0$. | ZF | |
| Operation and Compare Instructions | AD | Add M to AC | 0 1 1 0 | 0 0 0 0 | 1 | 1 | AC ← (AC) + (M(DP)) | Adds AC and M(DP) in binary and sets its sum in AC. | ZF CF | |
| | ADC | Add M to AC with CF | 0 0 1 0 | 0 0 0 0 | 1 | 1 | AC ← (AC) + (M(DP)) + (CF) | Adds AC and M(DP) with CF in binary and sets its sum in AC. | ZF CF | |
| | DAA | Decimal adjust AC in addition | 1 1 1 0 | 0 1 1 0 | 1 | 1 | AC ← (AC) + 6 | Adds 6 to AC. | ZF | |
| | DAS | Decimal adjust AC in subtraction | 1 1 1 0 | 1 0 1 0 | 1 | 1 | AC ← (AC) + 10 | Adds 10 to AC. | ZF | |
| | EXL | Exclusive or M to AC | 1 1 1 1 | 0 1 0 1 | 1 | 1 | AC ← (AC) ∀ (M(DP)) | Logically exclusive-Ors AC and M(DP) and sets its logical exclusive sum in AC. | ZF | |
| | AND | And M to AC | 1 1 1 0 | 0 1 1 1 | 1 | 1 | AC ← (AC) ∧ (M(DP)) | Logically Ands AC and M(DP) and sets its logical product in AC. | ZF | |
| | OR | Or M to AC | 1 1 1 0 | 0 1 0 1 | 1 | 1 | AC ← (AC) ∨ (M(DP)) | Logically Ors AC and M(DP) and sets its logical sum in AC. | ZF | |
| | CM | Compare AC with M | 1 1 1 1 | 1 0 1 1 | 1 | 1 | $\overline{(M(DP))}$ + (AC) + 1 | Compares AC with M(DP), and sets or resets CF and ZF according to the result. (Comparison result / CF / ZF: (M(DP)) > (AC) 0 0; (M(DP)) = (AC) 1 1; (M(DP)) < (AC) 1 0) | ZF CF | |
| | CI data | Compare AC with immediate data | 0 0 1 0<br>0 1 0 0 | 1 1 0 0<br>$I_3I_2I_1I_0$ | 2 | 2 | $\overline{I_3I_2I_1I_0}$ + (AC) + 1 | Compares AC with immediate data $I_3I_2I_1I_0$, and sets or resets CF and ZF according to the result. (Comparison result / CF / ZF: $I_3I_2I_1I_0$ > (AC) 0 0; $I_3I_2I_1I_0$ = (AC) 1 1; $I_3I_2I_1I_0$ < (AC) 1 0) | ZF CF | |
| | CLI data | Compare $DP_L$ with immediate data | 0 0 1 0<br>0 1 0 1 | 1 1 0 0<br>$I_3I_2I_1I_0$ | 2 | 2 | ($DP_L$) ∀ $I_3I_2I_1I_0$ | Compares $DP_L$ with immediate data $I_3I_2I_1I_0$. | ZF | |
| Load and Store Instructions | LI data | Load AC with immediate data | 1 1 0 0 | $I_3I_2I_1I_0$ | 1 | 1 | AC ← $I_3I_2I_1I_0$ | Load immediate data $I_3I_2I_1I_0$ into AC. | ZF | * 1 |
| | S | Store AC to M | 0 0 0 0 | 0 0 1 0 | 1 | 1 | M(DP) ← (AC) | Store AC to M(DP). | | |
| | L | Load AC from M | 0 0 1 0 | 0 0 0 1 | 1 | 1 | AC ← (M(DP)) | Load M(DP) into AC. | ZF | |
| | XM data | Exchange AC with M then modify $DP_H$ with immediate data | 1 0 1 0 | 0 $M_2M_1M_0$ | 1 | 2 | (AC) ⇄ (M(DP))<br>$DP_H$ ← ($DP_H$) ∀ 0 $M_2M_1M_0$ | Exchanges the contents of AC and M(DP), then logically exclusive-Ors ($DP_H$) and immediate data 0$M_2M_1M_0$ and finally replaces $DP_H$ with the logical exclusive sum. | ZF | Whether or not ZF is affected depends on the result of exclusive-Oring between ($DP_H$) and 0$M_2M_1M_0$. |
| | X | Exchange AC with M | 1 0 1 0 | 0 0 0 0 | 1 | 2 | (AC) ⇄ (M(DP)) | Exchanges the contents of AC and M(DP). | ZF | Whether or not ZF is affected depends on the DPH content at the time when the instruction is executed. |
| | XI | Exchange AC with M then increment $DP_L$ | 1 1 1 1 | 1 1 1 0 | 1 | 2 | (AC) ⇄ (M(DP))<br>$DP_L$ ← ($DP_L$) + 1 | Exchanges the contents of AC and M(DP) and then increments $DP_L$ by 1. | ZF | Whether or not ZF is affected depends on the $DP_L$ increment. |
| | XD | Exchange AC with M then decrement $DP_L$ | 1 1 1 1 | 1 1 1 1 | 1 | 2 | (AC) ⇄ (M(DP))<br>$DP_L$ ← ($DP_L$) − 1 | Exchanges the contents of AC and M(DP) and then decrements $DP_L$ by 1. | ZF | Whether or not ZF is affected depends on the $DP_L$ decrement. |
| | RTBL | Read table data from program ROM | 0 1 1 0 | 0 0 1 1 | 1 | 2 | AC, E ← ROM (PCh, E, AC) | Replaces the PC low-order 8 bits with E and AC, and then loads the contents of the ROM address specified by the new PC contents into AC and E. | | |

| Instruction group type | Mnemonic | | Operation Code $D_7D_6D_5D_4$ | Operation Code $D_3D_2D_1D_0$ | Bytes | Cycles | Operations | Operating Description | Affected STS flag(s) | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| Data Pointer Manipulation Instructions | LDZ data | Load $DP_H$ with Zero and $DP_L$ with immediate data respectively | 1 0 0 0 | $I_3$ $I_2$ $I_1$ $I_0$ | 1 | 1 | $DP_H \leftarrow 0$<br>$DP_L \leftarrow I_3 I_2 I_1 I_0$ | Loads zero and immediate data $I_3I_2I_1I_0$ into $DP_H$ and $DP_L$, respectively. | | |
| | LHI data | Load $DP_H$ with immediate data | 0 1 0 0 | $I_3$ $I_2$ $I_1$ $I_0$ | 1 | 1 | $DP_H \leftarrow I_3 I_2 I_1 I_0$ | Loads immediate data $I_3I_2I_1I_0$ into $DP_H$. | | |
| | IND | Increment $DP_L$ | 1 1 1 0 | 1 1 1 0 | 1 | 1 | $DP_L \leftarrow (DP_L)+1$ | Increments $DP_L$ content by 1. | ZF | |
| | DED | Decrement $DP_L$ | 1 1 1 0 | 1 1 1 1 | 1 | 1 | $DP_L \leftarrow (DP_L)-1$ | Decrements $DP_L$ content by 1. | ZF | |
| | TAL | Transfer AC to $DP_L$ | 1 1 1 1 | 0 1 1 1 | 1 | 1 | $DP_L \leftarrow (AC)$ | Transfers AC content to $DP_L$. | | |
| | TLA | Transfer $DP_L$ to AC | 1 1 1 0 | 1 0 0 1 | 1 | 1 | $AC \leftarrow (DP_L)$ | Transfers $DP_L$ content to AC. | ZF | |
| | XAH | Exchange AC with $DP_H$ | 0 0 1 0 | 0 0 1 1 | 1 | 1 | $(AC) \rightleftarrows (DP_H)$ | Exchanges the contents of AC and $DP_H$. | | |
| Working Register Manipulation Instructions | XAt<br>XA0<br>XA1<br>XA2<br>XA3 | Exchange AC with working register bAt | | $t_1$ $t_0$ | | | | Exchanges the contents of AC and a specified working register in register bank b (already selected). Note that bits $t_1$ and $t_0$ are used to specify working registers bA0, bA1, bA2 and bA3. | | |
| | | | 1 1 1 0 | 0 0 0 0 | 1 | 1 | $(AC) \rightleftarrows (bA0)$ | | | |
| | | | 1 1 1 0 | 0 1 0 0 | 1 | 1 | $(AC) \rightleftarrows (bA1)$ | | | |
| | | | 1 1 1 0 | 1 0 0 0 | 1 | 1 | $(AC) \rightleftarrows (bA2)$ | | | |
| | | | 1 1 1 0 | 1 1 0 0 | 1 | 1 | $(AC) \rightleftarrows (bA3)$ | | | |
| | XHa<br>XH0<br>XH1 | Exchange $DP_H$ with working register bHa | | a | | | | Exchanges the contents of DPH and a specified working register in register bank b (already selected). Note that bit a is used to specify working registers bH0 and bH1. | | |
| | | | 1 1 1 1 | 1 0 0 0 | 1 | 1 | $(DP_H) \rightleftarrows (bH0)$ | | | |
| | | | 1 1 1 1 | 1 1 0 0 | 1 | 1 | $(DP_H) \rightleftarrows (bH1)$ | | | |
| | XLa<br>XL0<br>XL1 | Exchange $DP_L$ with working register bLa | | a | | | | Exchanges the contents of $DP_L$ and a specified working register in register bank b (already selected). Note that bit a is used to specify working registers bL0 and bL1. | | |
| | | | 1 1 1 1 | 0 0 0 0 | 1 | 1 | $(DP_L) \rightleftarrows (bL0)$ | | | |
| | | | 1 1 1 1 | 0 1 0 0 | 1 | 1 | $(DP_L) \rightleftarrows (bL1)$ | | | |
| | SRBA | Set Register Bank Address | 1 1 1 1 | 0 0 1 0 | 1 | 1 | RBF ← I110 of SB | Sets the bank value given by the SB instruction in the register bank flag. | | |
| Flag Manipulation Instructions | SFB flag | Set flag bit | 0 1 0 1 | $B_3$ $B_2$ $B_1$ $B_0$ | 1 | 1 | bFn←1 | Sets a specified flag in register bank b (already selected). Note that immediate data $B_3B_2B_1B_0$ is used to specify the flags. | | |
| | RFB flag | Reset flag bit | 0 0 0 1 | $B_3$ $B_2$ $B_1$ $B_0$ | 1 | 1 | bFn←0 | Resets a specified flag in register bank b (already selected). Note that immediate data $B_3B_2B_1B_0$ is used to specify the flags. | ZF | Flags are divided into 16 groups: 0F3 to 0F0, 0F4 to 0F7, 3F11, 3F12 to 3F15. Whether ZF is set or reset depends on the content of the 4-bit group to which a specified flag belongs. |
| Jump and Subroutine Instructions | JMP addr | Jump in the current bank | 0 1 1 0<br>$P_7$ $P_6$ $P_5$ $P_4$ | 1 $P_{10}$ $P_9$ $P_8$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | PC ← PC11 or (inverted PC11)<br>$P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$ | Makes program jump to the address specified by PC11 (or inverted PC11) and immediate data $P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$. | | If executed immediately after the BANK instruction, the current bank value will be changed (bit PC11 is inverted). |
| | JPEA | Jump in the current page modified by E and AC | 1 1 1 1 | 1 0 1 0 | 1 | 1 | $PC_{7\text{to}0} \leftarrow (E, AC)$ | Replaces lower- order 8 bits of PC with E and AC and then jumps to the address specified by the new PC content. | | |
| | CZP addr | Call subroutine in the zero page | 1 0 1 1 | $P_3$ $P_2$ $P_1$ $P_0$ | 1 | 1 | STACK←(PC)+1<br>$PC_{11\text{to}6}, PC_{1\text{to}0} \leftarrow 0$<br>$PC_{5\text{to}2} \leftarrow P_3P_2P_1P_0$ | Calls a subroutine in page 0 of bank 0. | | |
| | CAL addr | Call subroutine in the zero bank | 1 0 1 0<br>$P_7$ $P_6$ $P_5$ $P_4$ | 1 $P_{10}$ $P_9$ $P_8$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | STACK←(PC)+2<br>$PC_{11\text{to}0} \leftarrow 00\,P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$ | Calls a subroutine in bank 0. | | |
| | RT | Return from subroutine | 0 1 1 0 | 0 0 1 0 | 1 | 1 | PC ← (STACK) | Returns to main routine from a subroutine. | | |
| | RTI | Return from interrupt routine | 0 0 1 0 | 0 0 1 0 | 1 | 1 | PC ← (STACK)<br>CF ZF ← CSF, ZSF | Returns to main routine from an interrupt servicing routine. | ZF CF | |
| | BANK | Change bank | 1 1 1 1 | 1 1 0 1 | 1 | 1 | $PC_{11} \leftarrow \overline{(PC_{11})}$<br>GP(DP) | Specifies new ROM banks or pseudo ports. | | |
| | SB | Set bank | 0 1 1 0 | 0 1 $I_1$ $I_0$ | 1 | 1 | RBF←$I_1I_0$ | Specifies working register and flag banks. | | |
| Branch Instructions | BAt addr | Branch on AC bit | 0 1 1 1<br>$P_7$ $P_6$ $P_5$ $P_4$ | 0 0 $t_1$ $t_0$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | $PC_{7\text{to}0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$<br>if ACt = 1 | Makes program branch to a specified address in the same page if a specified AC bit is set to 1. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses and another immediate data $t_1t_0$ used to specify AC bits. | | The mnemonic will change from BA0 to BA3 depending on the value of immediate data $t_1t_0$. |
| | BNAt addr | Branch on no AC bit | 0 0 1 1<br>$P_7$ $P_6$ $P_5$ $P_4$ | 0 0 $t_1$ $t_0$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | $PC_{7\text{to}0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$<br>if ACt = 0 | Makes program branch to a specified address in the same page if a specified AC bit is reset to 0. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses and another immediate data $t_1t_0$ used to specify the desired bit. | | The mnemonic will change from BNA0 to BNA3 depending on the value of immediate data $t_1t_0$. |
| | BMt addr | Branch on M bit | 0 1 1 1<br>$P_7$ $P_6$ $P_5$ $P_4$ | 0 1 $t_1$ $t_0$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | $PC_{7\text{to}0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$<br>if (M(DP.$t_1t_0$)) = 1 | Makes program branch to a specified address in the same page if a specified M(DP) bit is set to 1. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses and another immediate data $t_1t_0$ used to specify the desired bit. | | The mnemonic will change from BM0 to BM3 depending on the value of immediate data $t_1t_0$. |
| | BNMt addr | Branch on no M bit | 0 0 1 1<br>$P_7$ $P_6$ $P_5$ $P_4$ | 0 1 $t_1$ $t_0$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | $PC_{7\text{to}0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$<br>if (M(DP.$t_1t_0$)) = 0 | Makes program branch to a specified address in the same page if a specified M(DP) bit is reset to 0. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses and another immediate data $t_1t_0$ used to specify the desired bit. | | The mnemonic will change from BNM0 to BNM3 depending on the value of immediate data $t_1t_0$. |
| | BPt addr | Branch on Port bit | 0 1 1 1<br>$P_7$ $P_6$ $P_5$ $P_4$ | 1 0 $t_1$ $t_0$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | $PC_{7\text{to}0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$<br>if (P($DP_L$.$t_1t_0$)) = 1<br>or (GP(DP.$t_1t_0$)) = 1 | Makes program branch to a specified address in the same page if a specified port P($DP_L$) or pseudo port GP(DP) bit is set to 1. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses and another immediate data $t_1t_0$ used to specify the desired bit. | | The mnemonic will change from BP0 to BP3 depending on the value of immediate data $t_1t_0$. |
| | BNPt addr | Branch on no Port bit | 0 0 1 1<br>$P_7$ $P_6$ $P_5$ $P_4$ | 1 0 $t_1$ $t_0$<br>$P_3$ $P_2$ $P_1$ $P_0$ | 2 | 2 | $PC_{7\text{to}0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$<br>if (P($DP_L$.$t_1t_0$)) = 0<br>or (GP(DP.$t_1t_0$)) = 0 | Makes program branch to a specified address in the same page if a specified port P($DP_L$) or pseudo port GP(DP) bit is reset to 0. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses and another immediate data $t_1t_0$ used to specify the desired bit. | | The mnemonic will change from BNP0 to BNP3 depending on the value of immediate data $t_1t_0$. |

| Instruction group type | Mnemonic | | Operation Code | | Bytes | Cycles | Operations | Operating Description | Affected STS flag(s) | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $D_7D_6D_5D_4$ | $D_3D_2D_1D_0$ | | | | | | |
| Branch Instructions | BC addr | Branch on CF | 0 0 1 1 $P_7P_6P_5P_4$ | 1 1 1 0 $P_3P_2P_1P_0$ | 2 | 2 | $PC_{7to0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ If CF = 1 | Makes program branch to a specified address in the same page if CF is set. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses. | | |
| | BNC addr | Branch on no CF | 0 0 1 1 $P_7P_6P_5P_4$ | 1 1 1 1 $P_3P_2P_1P_0$ | 2 | 2 | $PC_{7to0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ If CF = 0 | Makes program branch to a specified address in the same page if CF is reset. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses. | | |
| | BZ addr | Branch on ZF | 0 1 1 1 $P_7P_6P_5P_4$ | 1 1 1 0 $P_3P_2P_1P_0$ | 2 | 2 | $PC_{7to0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ If ZF = 1 | Makes program branch to a specified address in the same page if ZF is set. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses. | | |
| | BNZ addr | Branch on no ZF | 0 0 1 1 $P_7P_6P_5P_4$ | 1 1 1 0 $P_3P_2P_1P_0$ | 2 | 2 | $PC_{7to0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ If ZF = 0 | Makes program branch to a specified address in the same page if ZF is reset. Note that immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ is used to specify addresses. | | |
| | BFn addr | Branch on flag bit | 1 1 0 1 $P_7P_6P_5P_4$ | $n_3n_2n_1n_0$ $P_3P_2P_1P_0$ | 2 | 2 | $PC_{7to0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ If bFn = 1 | Makes program branch to a specified address in the same page if a specified flag bit (one of the 16 flag bits) in register bank b (already selected) is set. Note that immediate data $n_3n_2n_1n_0$ is used to specify the desired flag bit and another immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ used to specify the desired address. | | The mnemonic changes from BF0 to BF15 according to the values of n. |
| | BNZ addr | Branch on no flag bit | 1 0 0 1 $P_7P_6P_5P_4$ | $n_3n_2n_1n_0$ $P_3P_2P_1P_0$ | 2 | 2 | $PC_{7to0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ If bFn = 0 | Makes program branch to a specified address in the same page if a specified flag bit (one of the 16 flag bits) in register bank b (already selected) is reset. Note that immediate data $n_3n_2n_1n_0$ is used to specify the desired flag bit and another immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ used to specify the desired address. | | The mnemonic changes from BNF0 to BNF15 according to the values of n. |
| Input/output Instructions | IP | Input port to AC | 0 0 0 0 | 1 1 0 0 | 1 | 1 | AC ← (P(DPL)) or (GP(DP)) | Inputs data to AC from the port P(DPL) or pseudo port GP (DP). | ZF | |
| | OP | Output AC to port | 0 1 1 0 | 0 0 0 1 | 1 | 1 | P(DPL) or GP(DP) ← (AC) | Outputs data to the port P(DPL) or pseudo port GP(DP) from AC. | | |
| | SPB bit | Set port bit | 0 0 0 0 | 0 1 $B_1B_0$ | 1 | 2 | $P(DP_L.B_1B_0) \leftarrow 1$ or GP(DP, $B_1B_0$) | Sets a specified bit of the port P(DPL) or pseudo port GP (DP). Note that immediate data B1B0 is used to specify the desired port bit. | | If executed, the content of the E register will be destroyed. |
| | RPB bit | Reset port bit | 0 0 1 0 | 0 1 $B_1B_0$ | 1 | 2 | $P(DP_L.B_1B_0) \leftarrow 0$ or GP(DP, $B_1B_0$) | Resets a specified bit of the port P(DPL) or pseudo port GP (DP). Note that immediate data $B_1B_0$ is used to specify the desired port bit. | ZF | If executed, the content of the E register will be destroyed. |
| Other Instructions | SCTL bit | Set control register bit | 0 0 1 0 1 0 0 0 | 1 1 0 0 $B_3B_2B_1B_0$ | 2 | 2 | CTL, $B_3B_2B_1B_0 \leftarrow 1$ or MSTEN ← 1 | Sets a specified bit of the control register (individual interrupt enable flag) or the master interrupt enable flag. Note that immediate data $B_3B_2B_1B_0$ is used to specify the desired bit. | | * 2 |
| | RCTL bit | Reset control register bit | 0 0 1 0 1 0 0 1 | 1 1 0 0 $B_3B_2B_1B_0$ | 2 | 2 | CTL, $B_3B_2B_1B_0 \leftarrow 0$ or MSTEN ← 0 | Resets a specified bit of the control register (individual interrupt enable flag) or the master interrupt enable flag. Note that immediate data $B_3B_2B_1B_0$ is used to specify the desired bit. | ZF | * 2 |
| | HALT | Halt | 1 1 1 1 | 0 1 1 0 | 1 | 1 | Halt, Hold | Places the chip in the standby mode. | | |
| | NOP | No operation | 0 0 0 0 | 0 0 0 0 | 1 | 1 | No operation | The CPU runs idle for one machine cycle. | | |

*1: If two or more LI or CLA instructions are executed continuously, only the first instruction will be executed normally. However, the instructions following the first will be handled as the NOP instructions.

*2: B3B2B1B0 = 0000B to 1000B

## On the LC65404A user mask option code specification

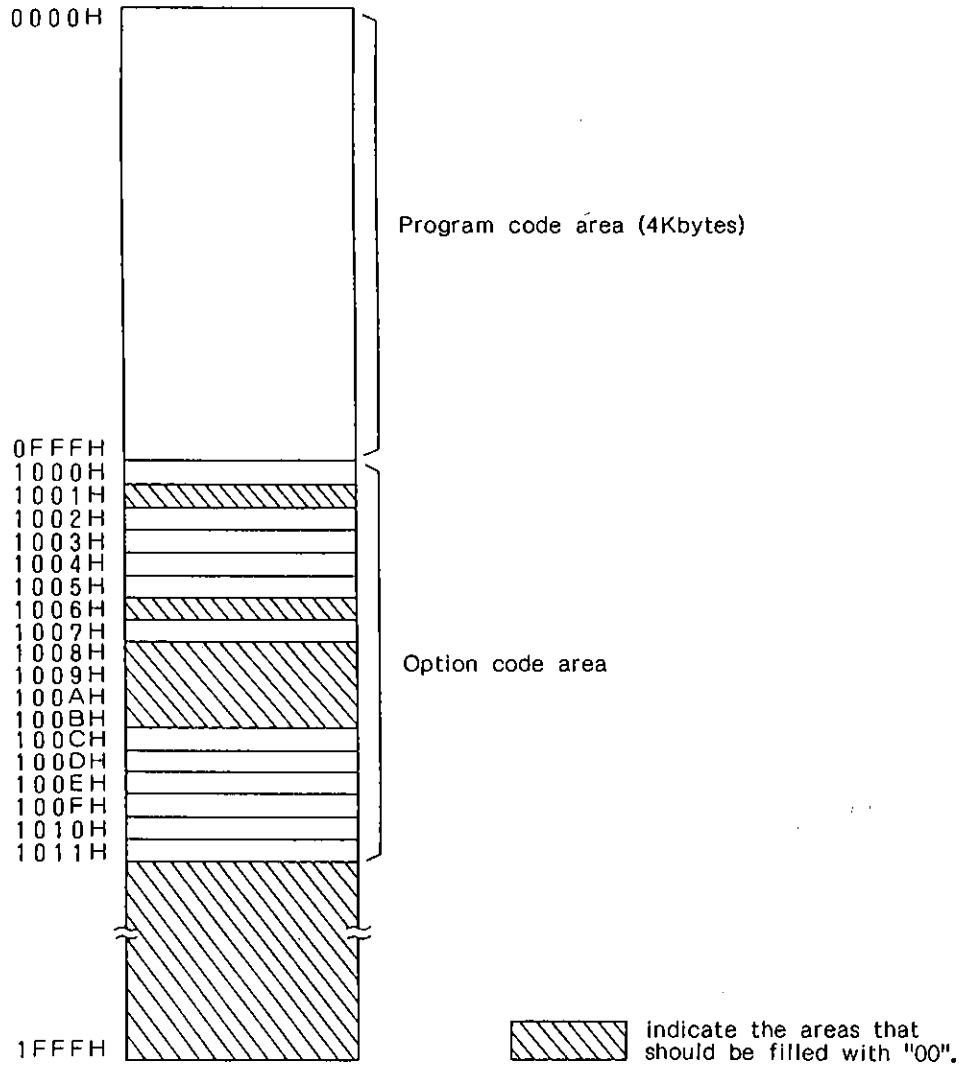
Overview

The user mask option data for the LC65404A should be stored to an EPROM as well as program code and then sent to Sanyo.

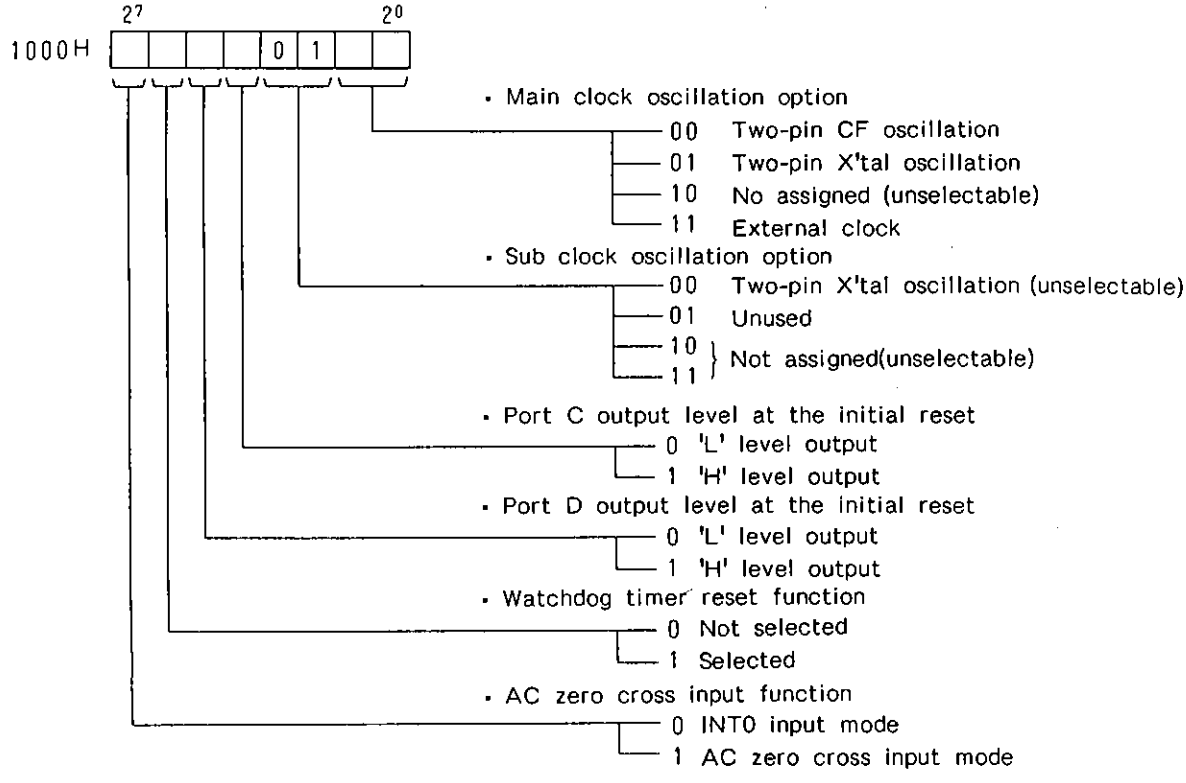
With the Sanyo cross assembler for the LC65404A, the user is allowed to specify option codes in the conversation mode and the user option data can be set in an EPROM properly with ease.

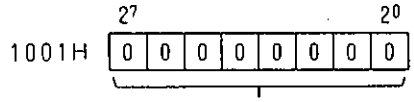
If the Sanyo cross assembler is not used, the option code should be specified in the following manner (this corresponds to the format of the cross assembler):

EPROM address map

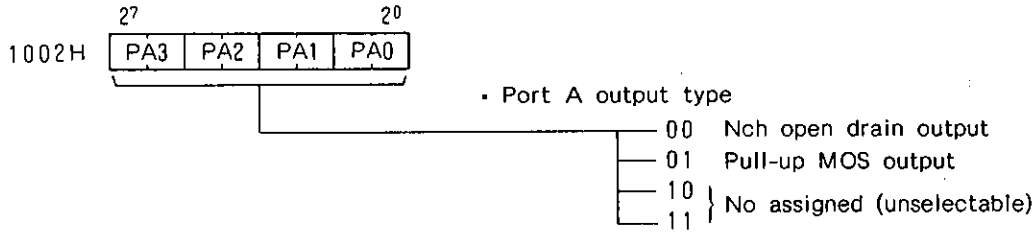


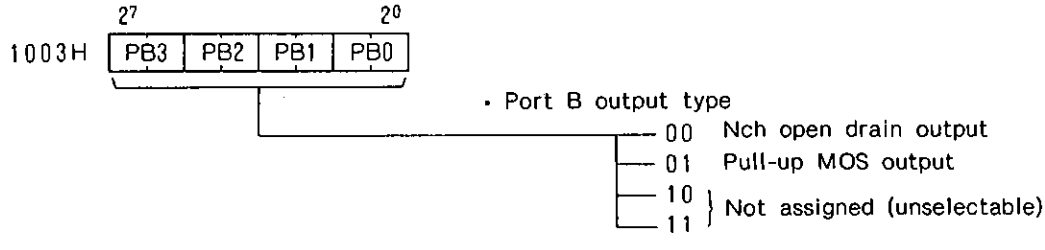
Contents of User option codes




These bits should always be set to '0'.

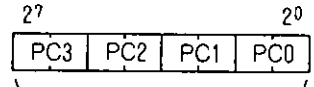



To be continued on the next page.

Continued from the preceding page.

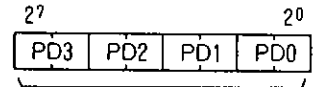
1004H




• Port C output type

- 00 Pch open drain output
- 01 Not assigned (unselectable)
- 10 Pull-down resistor output
- 11 Not assigned (unselectable)

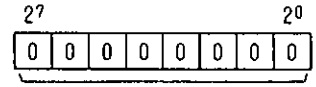
1005H




• Port D output type

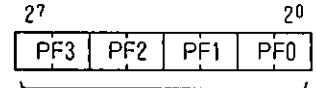
- 00 Pch open drain output
- 01 Not assigned (unselectable)
- 10 Pull-down resistor output
- 11 Not assigned (unselectable)

1006H




These bits should always be set to '0'.

1007H

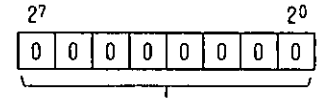



• Port F output type

- 00 Nch open drain output
- 01 Pull-up MOS output
- 10, 11 Not assigned (unselectable)

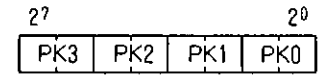
(Note) Be sure to set the output type of the PF3 port pin to OD if the AC zero cross input mode has been selected with the AC zero cross input option.

1008H to 100BH




These bits should always be set to '0'.

100CH

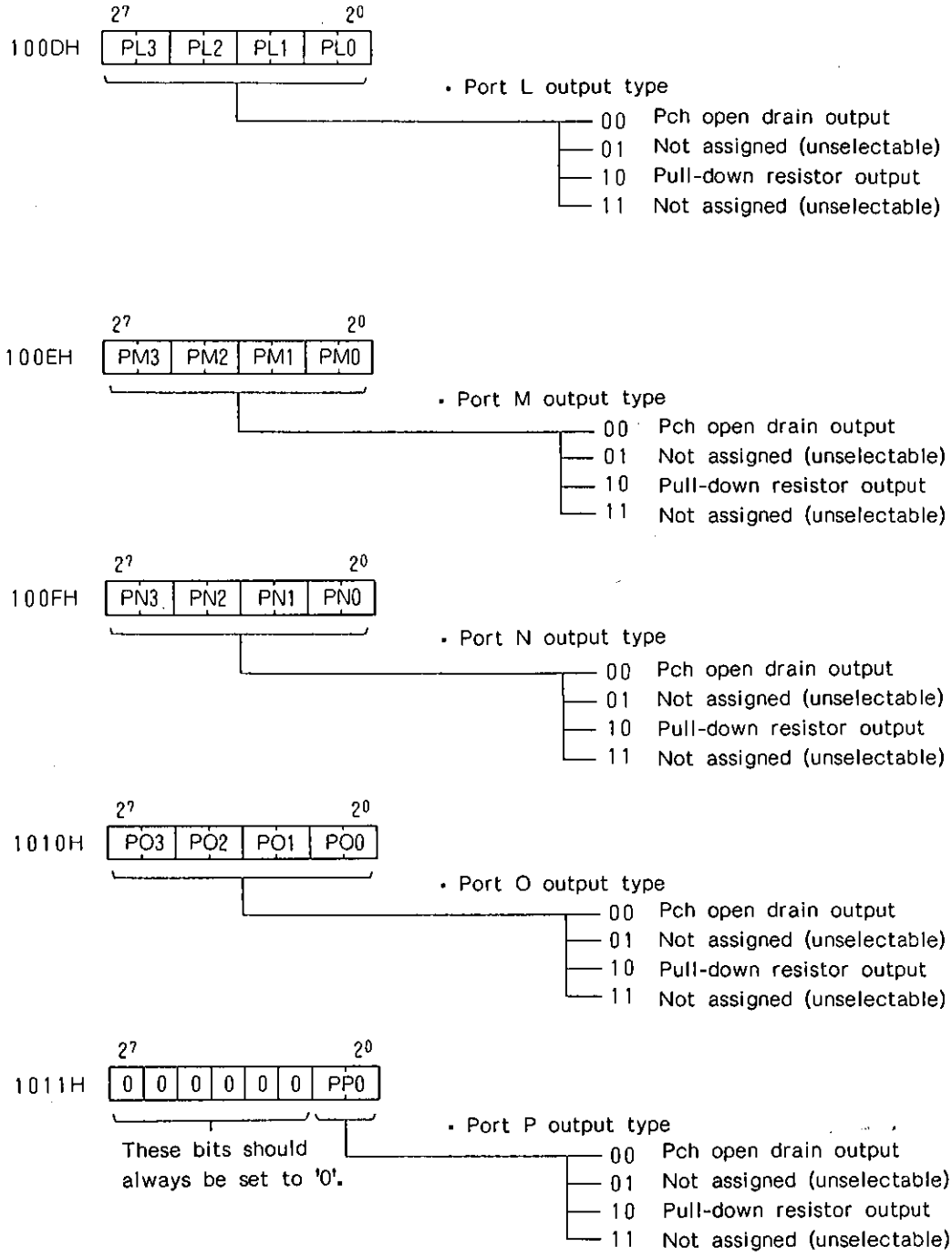



• Port K output type

- 00 Pch open drain output
- 01 Not assigned (unselectable)
- 10 Pull-down resistor output
- 11 Not assigned (unselectable)

To be continued on the next page.

Continued from the preceding page.



## Programming Considerations

- The user application programs for the LC65404A should be developed with the following considerations in mind.

<table>
<tr><th colspan="2">Item</th><th>Functions</th><th>Consideration</th></tr>
<tr><td rowspan="3">System Clock Function</td><td>System clock mode</td><td>The LC65404A allows the user to select the desired system clock source from the following three by software.<br>① Main clock 1/1 mode ($T_{CYC}$= 0.95 µs)<br>② Main clock 1/2 mode ($T_{CYC}$ = 1.90 µs)<br>③ Main clock 1/32 mode ($T_{CYC}$ = 30.6 µs)<br><br>(Note) Main clock = 4.19MHz</td><td>• The main clock oscillation is always required at the system start-up.</td></tr>
<tr><td>System clock switching</td><td>The desired system clock mode can be selected by writing data to the clock mode flag (CMF: 2 bits) of the system clock control register as shown below:<br><table><tr><th>CMF</th><th>System clock mode</th></tr><tr><td>0</td><td>Main clock 1/32 mode (at the reset)</td></tr><tr><td>1</td><td>Main clock 1/1 mode</td></tr><tr><td>2</td><td>Main clock 1/2 mode</td></tr><tr><td>3</td><td>Unusable</td></tr></table></td><td>• When the current system clock mode needs to be changed, the user should confirm that the main clock oscillation has become stabilized or that the MCSTP flag has been set to '0' in the external clock input mode.<br>• The current system clock mode will be switched to the desired mode in 64 cycles (64/fMOSC. Max.) after the CMF flag is set properly. If the user wants the LC65404A to enter a standby mode after the system clock switching, the above switching time period should be kept in mind. That is, the user should execute the HALT instruction after the switching time elapses.</td></tr>
<tr><td>Main clock control (oscillation stop/start)</td><td>The main clock oscillation should be started by setting the MCSTP flag of the system clock control register to "0" (at the reset).</td><td>• Be sure not to set the MCSTP to '1'. If it is set to '1', the main clock oscillation will stop. As a result, the microcomputer will operate abnormally.</td></tr>
<tr><td rowspan="2">Standby Function</td><td>HALT mode start/release</td><td><Start><br>The HALT mode will be started if the HALT instruction is executed with the SLPF flag of the standby control register set to '0'. Note that the instruction will be processed as the NOP instruction if one of the following conditions is satisfied.<br><br><Release><br>(1) Reset<br>(2) The PB3/START pin is set to 'H' with the WG2 = 1.<br>(3) The interrupt release signal becomes active with the WG3 = 1.<br>(4) Time base overflow</td><td>• If the HALT mode needs to be released based on the PB3/START pin level ('H') or the interrupt release signal, the WG2 or WG3 flag must be set prior to the execution of the HALT instruction.</td></tr>
<tr><td>HOLD mode start/release</td><td><Start><br>The HOLD mode will be started if the HALT instruction is executed with the SLPF = 1.<br><br><Release><br>(1) Reset<br>(2) The PB3/START pin is set to 'H' with the WG1 = 1.</td><td>• Execute one NOP instruction before issuing the HALT instruction to place the microcomputer in the HOLD mode.<br>• If the HOLD mode needs to be released based on the PB3/START pin level, it should be confirmed that the WG1 flag is set and the active oscillation clock (either main clock x 1/128 ) is used as the time base source clock prior to the execution of the HALT instruction.</td></tr>
</table>

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| Item | | Functions | Consideration |
|---|---|---|---|
| Watchdog reset (only in case when the optional watchdog function has been selected) | | The watchdog reset function uses the time base timer to allow program upset and watchdog reset. | • The routine must be included in the user application program in order to reset the TBF flag within a certain fixed time (maximum time base timer overflow cycle). In this case, be sure not to overlap the time base interrupt request signal timing with the TBF flag reset timing.<br>• The active oscillation clock should be used as the time base clock source.<br>• If the time base interrupt request flag (TBF) is set to '1' prior to the HALT mode activation, the HALT mode will be released due to the time base overflow signal and at the same time the watchdog reset signal becomes active. In order to prevent the watchdog reset at the HALT mode release, ① reset the TBF immediately before executing the HALT instruction or ② set the time base interrupt enable flag (TBEN) and the HALT release enable flag (WG3: release due to the interrupt) before executing the HALT instruction. |
| Interrupt function | Interrupt Enable flag (control register: 5 bits) | • Five flags are provided to control the five interrupt sources on one-to-one basis. To enable a certain interrupt request, its corresponding interrupt enable flag must be set. (For this purpose, the SCTL0 to SCTL7 instructions can be used. Note that multiple flag bits cannot be accessed at the same time.)<br>• All the interrupt enable flags are reset at the system reset. | • No flag is reset after interrupt processing terminates. In resetting a certain flag, issue the RCTL instruction to that flag.<br>• All the flags are reset at the HOLD mode start. Set the desired flag after the HOLD mode is released. |
| | Interrupt request flag | • Five interrupt request flags are provided to the five interrupt sources on an one-to-one basis. These flags are assigned to a pseudo port. To reset the flag bits, data is loaded to the AC (ACcumulator) by the 'BANK + IP' instructions and then output to the port by the 'BANK + OP' instructions. Note that any bit cannot be set. The data bit that corresponds to the flag bit to be reset should be set to '0' and the remaining data bits should be set to '1'. This data should be first set in the AC and then output to the interrupt request register by the 'BANK + OP' instructions.<br>• At the reset, all the flags except for the timer 1 interrupt request flag (TM1F) are set to all '0'.<br>• The SIOF is reset the moment when the serial data transfer is started. | • No flag is reset after interrupt processing terminates. Every time when a certain interrupt processing is performed, be sure to reset the flag that corresponds to the interrupt source. Note that if the interrupt request flag needs to be reset, it should be confirmed that the master interrupt enable flag, and at the same time the individual interrupt enable flag that corresponds to that interrupt source are both reset or either one is reset.<br>• All the flags are reset at the HOLD mode start-up.<br>• Be sure not to issue the 'BANK + SPB/RPB' instructions to the interrupt request register. |

## Considerations on Program Evaluation

- The application programs for the LC65404A should be evaluated on the evaluation chip (LC65999 or LC65PG20X/40X) with the following considerations in mind.

| Item type | Item | Function | | Consideration |
|---|---|---|---|---|
| | | Production chip | EVA chip | |
| Function Settings | RAM capacity | RAM capacity of 256 x 4 bits | The desired RAM capacity can be selected by using the RC and RC2 pins. | Set the RC and RC2 pins properly in accordance with the production chip RAM capacity. |
| | Stack levels | 8 levels | The desired stack level can be set by the STC pin. | Set the STC pin properly in accordance with the production chip setting. |
| | Output type of ports C and D | Pch high-voltage withstand input/output | The circuit type of ports C and D can be set to the Pch high-voltage withstand input/output or the Nch medium-voltage withstand input/output by the C/FLSEL pin. | Set the C/FLSEL pin properly in accordance with the production chip circuit type. |
| Optional functions | Oscillation circuit | Connect the desired oscillator with pins OSC1 and OSC2. | If the EVA chip board is used for program evaluation, the desired oscillator can be selected by using the jump switch on the board. The simulation chip has the same optional selection as the production chip. | [EVA chip board] Set the jumper switch properly in accordance with the production chip option setting. [simulation chip] Connect the same oscillation as that of the production chip to pins OSC1, OSC2. |
| | Output level of ports C and D at the reset | 4-bit simultaneous select. The output level of all the four bits of the port C or D can be set to the 'H' or 'L' at the same time. | Port C can set to the 'H' or 'L' by the CHL pin while port D by the DHL pin. | Set the CHL and DHL pins properly in accordance with the production chip option setting. |
| | Watchdog reset function | The watchdog reset function based on the time base timer can be selected. | The watchdog function can be activated or inactivated by using the WDC pin. | Set the WDC pin properly in accordance with the production chip option setting. |
| | AC zero cross detection circuit | The AC zero cross detection circuit can be internally added to the PF3/INT0 pin. | The AC zero cross detection circuit can be internally activated by the ACZ/$\overline{\text{INT0}}$ pin. | Set the ACZ/$\overline{\text{INT0}}$ pin properly in accordance with the production chip option setting. |
| | Port output type: PU and OD | The output type of each port pin can be set to the PU or OD (on a single-bit manipulation basis). | No pull-up resistor output can be selected. All the port pins are set to the Nch OD output type. | [EVA chip board] Connect the 10kohm of external resistor to the target port. [Simulation chip] Connect a resistor to the target port of the user application board. |
| | PU resistor | This resistor is used with the port pin that enters the high impedance state (HI-Z OFF) at the 'L'-level output. | Since this is a resistor externally added, the impedance level remains unchanged at the 'L' level output. | On the production chip, only the leakage current flows into the Pch Tr. at the 'L' output. However, please note that the current flow continues through the pull-up resistor on the EVA chip. |
| | Port output type: PD and OD | The output type of each port pin can be set to the OD or PD (on a single-bit manipulation basis). | No pull-down resistor can be selected. All the port pins are set to the Pch OD output type. | [EVA chip board] Connect the 100kohm of external resistor to the target port. [Simulation chip] Connect the external resistor to the target port of the user application board. Note that the user application board should have its own load power supply. |

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| Item type | Item | Function | | Consideration |
|---|---|---|---|---|
| | | Production Chip | EVA Chip | |
| Oscillation | Main clock oscillation constant | [Crystal oscillation] and [Ceramic oscillation] If the guaranteed constant listed in this catalog is used, the standard oscillation frequency is produced. | [Crystal oscillation] and [Ceramic oscillation] The EVA chip differs from the production chip in oscillation circuit design and characteristics. In addition, the oscillation may be unstable due to wire capacitance. | [Crystal oscillation] and [Ceramic oscillation] External constants should be fine-adjusted according to the evaluation environment. |
| Electrical Characteristics | Oscillation frequencies of main clock | The oscillation frequency characteristics are shown in this catalog. | The EVA chip differs from the production chip in circuit design and characteristics. | The detailed evaluation should be performed on the ES and CS. |
| | Operation current and Standby current | The current characteristics are shown in this catalog. | The EVA chip differs from the production chip in circuit design and characteristics. | The standby current cannot be evaluated in detail. However, the standby function can be confirmed in the manner as shown in the manual. Be sure to check the standby function in that way. The characteristics should be evaluated in detail on the EC and CS. |
| | Operating power supply voltage | The operating power supply voltage range is shown in this catalog. | The power supply voltage range is limited to the the range for the EPROM and other LSIs. | The EVA chip should operate in the operating power supply voltage range of $V_{DD}$=5V ±5%. The operating voltage range of the EPROM and other LSIs should not be exceeded. This means that the functions in the entire operating range of the production chip cannot be evaluated. |
| | Operating ambient temperature | The operating ambient temperature is shown in this catalog. | Guaranteed temperature range: 10 °C to 40 °C | The operating temperature range of the EVA chip and the simulation chip should be from 10 °C to 40 °C. |
| Function | ROM capacity | The LC65404A has the 4Kbyte ROM. This means that the JMP and BANK + JMP instructions allow program to jump to the entire ROM area. Note that the SB + JMP instructions cannot be used. | Up to 8Kbytes of ROM can be externally added to the chip. The SB + JMP, BANK + JMP and JMP instructions allow program to jump to the entire ROM area. | It should be confirmed that the application program size is less than 4K bytes. |


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