

SANYO

No.2622B

L78LR05

150mA, 5V 5-Pin Voltage Regulator
with Reset Function

Overview

The L78LR05 is a voltage regulator IC that performs the reset signal generating function when the power supply of a microcomputer system is turned ON/OFF. The L78LR05 is convenient for battery backup system at the time of power failure. The reset threshold voltage V_{RT} is ranked as shown below.

V_{RT} rank	B	C	D	E	F	G	H
V_{RT} (V)	4.8	4.5	4.2	3.9	3.6	3.3	3.0

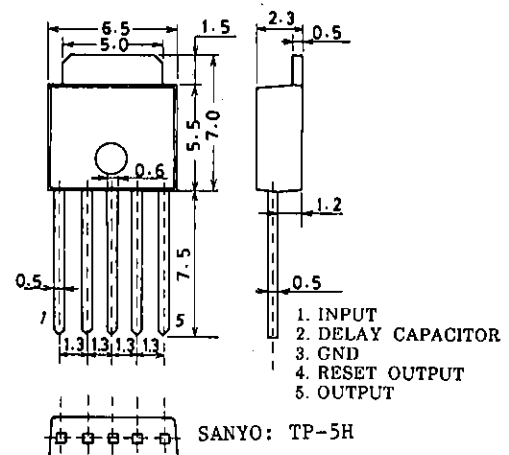
Applications

- Prevention of malfunction that may occur when the power supply of a microcomputer is turned ON/OFF.
- Measures taken against abnormal operations that may occur at the time of instantaneous break of power supply
- Direct battery backup for SRAM

Features

- 5V, 150mA output
- Capable of generating a microcomputer reset signal
- No battery-regulator switching circuit required at the battery backup mode (Output leakage current: $2\mu\text{A}$ or less)
- An external capacitor can be used to set the reset output delay time.
- Applicable to the power supply of CMOS, NMOS microcomputers
- Especially suited for use as an on-board regulator for a microcomputer system
- Small-sized power package TP-5H permitting the equipment to be made compact
- The allowable power dissipation can be increased by being surface-mounted on the board.
- Capable of being mounted in a variety of methods because of various lead forming versions available
- On-chip protectors (overcurrent limiter, ASO protector, thermal protector)

Package Dimensions (unit: mm)



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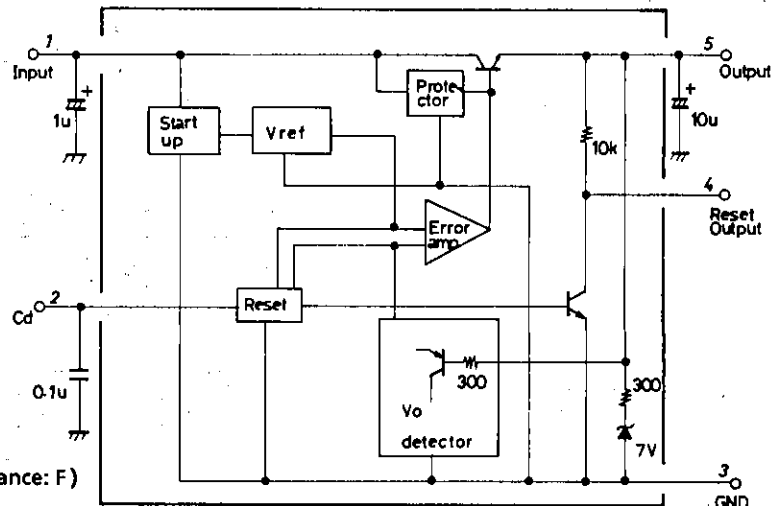
Maximum Ratings at Ta = 25°C				unit
Maximum Input Voltage	V _{IN} max		25	V
Allowable Power Dissipation	P _d max	(No fin)	1.0	W
Operating Temperature	T _{opr}		-30 to +80	°C
Storage Temperature	T _{stg}		-55 to +150	°C

Operating Conditions at Ta = 25°C				unit
Input Voltage	V _{IN}		7.5 to 20	V
Output Current	I _{OUT}		1 to 150	mA

Operating Characteristics at Ta = 25°C, V_{IN} = 10V, I_{OUT} = 40mA, c_{in} = 1μF, c_o = 10μF

			min	typ	max	unit	
Output Voltage	V _{OUT1}	T _j = 25°C	4.8	5.0	5.2	V	
	V _{OUT2}	7V ≤ V _{IN} ≤ 20V, 1mA ≤ I _{OUT} ≤ 70mA	4.75		5.25	V	
Line Regulation	ΔV _o LINE1	T _j = 25°C, 7V ≤ V _{IN} ≤ 20V		6.0	75	mV	
	ΔV _o LINE2	T _j = 25°C, 8V ≤ V _{IN} ≤ 20V		3.0	50	mV	
Load Regulation	ΔV _o LOAD1	T _j = 25°C, 1mA ≤ I _{OUT} ≤ 100mA		9.0	60	mV	
	ΔV _o LOAD2	T _j = 25°C, 1mA ≤ I _{OUT} ≤ 40mA		3.0	30	mV	
Current Dissipation	I _{CC}	T _j = 25°C, I _{OUT} = 100mA		1.4	3.4	mA	
Current Dissipation Variation	ΔI _{CC} LINE	8V ≤ V _{IN} ≤ 20V		0.12	1.5	mA	
	ΔI _{CC} LOAD	1mA ≤ I _{OUT} ≤ 40mA		0.01	0.1	mA	
Output Noise Voltage	V _{NO}	10Hz ≤ f ≤ 100kHz, I _o = 1mA		80		μV	
Temperature Coefficient of Output Voltage	ΔV _{OUT} /ΔT _j	I _{OUT} = 1mA, T _j = 25 to 125°C		±0.5		mV/°C	
Ripple Rejection	R _{rej}	T _j = 25°C, f = 120Hz, 8V ≤ V _{IN} ≤ 18V		79		dB	
Dropout Voltage	V _{DROP}	T _j = 25°C		1.5	2.2	V	
Output Short Current	I _{OSC}	T _j = 25°C	150	300	450	mA	
"H"-Reset Output Voltage	V _{ORH}	T _j = 25°C	4.8	5.0	5.2	V	
"L"-Reset Output Voltage Reset Threshold Voltage	V _{ORL}	T _j = 25°C, V _{IN} = 3V, I _o = 1mA		10	200	mV	
	V _{RT}	B	T _j = 25°C	4.60	4.8	4.95	V
		C		4.30	4.5	4.65	V
		D		4.00	4.2	4.35	V
		E		3.70	3.9	4.05	V
		F		3.40	3.6	3.75	V
		G		3.10	3.3	3.45	V
		H		2.80	3.0	3.15	V
Reset Threshold Hysteresis Voltage		V _{RTH}			50	100	200
Reset Output Delay Time	t _d	c _d = 0.1μF	7.5	10	12.5	msec	
Output Pin Leakage Current	I _O LEAK	V _{IN} = 0, V _o = 6V	0.001	2		μA	
Reset Output Pin Leakage Current	I _{OR} LEAK	V _{IN} = 0, V _{OR} = 6V	0.001	2		μA	

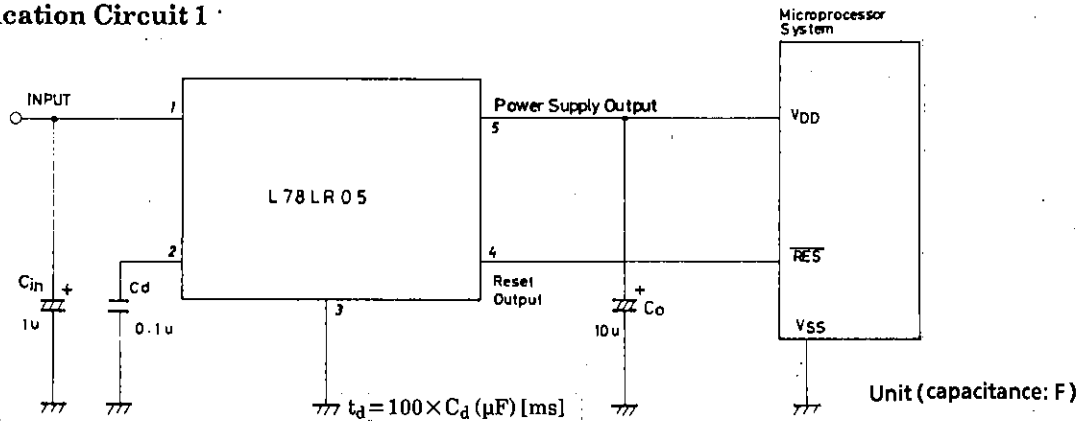
Equivalent Circuit Block Diagram



Unit (resistance: Ω, capacitance: F)

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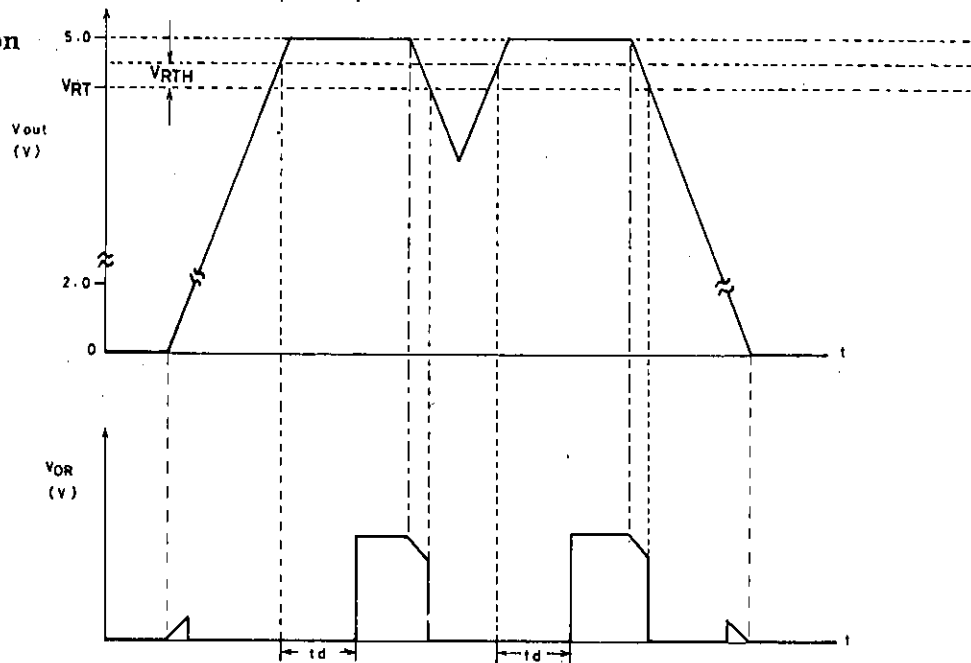
Sample Application Circuit 1



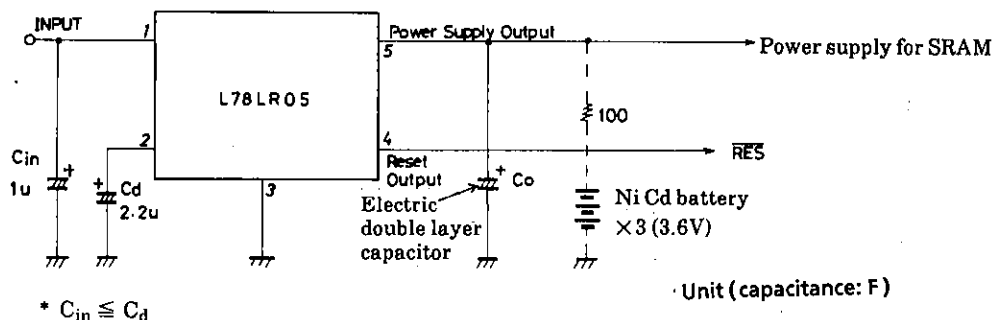
Note 1: When the capacitance of C_d is large, the capacitor may not discharge completely, causing t_d to be made shorter than a set value. If this is a problem, either connect a high speed diode (DS442) between pin2 (anode side) and pin5 (cathode side) or ensure an adequate discharge time by using values for capacitors C_{in} and C_d such that $C_{in} > C_d$.

Note 2: If a pull-up resistor is connected to the reset output pin externally, it is possible to cause a sink current up to 4mA to flow.

Reset Operation



Sample Application Circuit 2 (Direct battery backup)



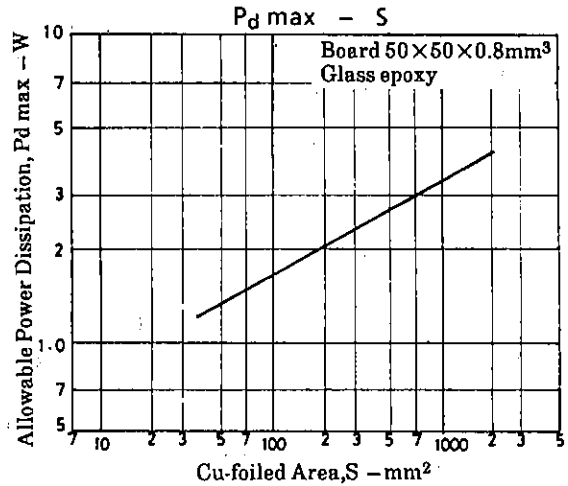
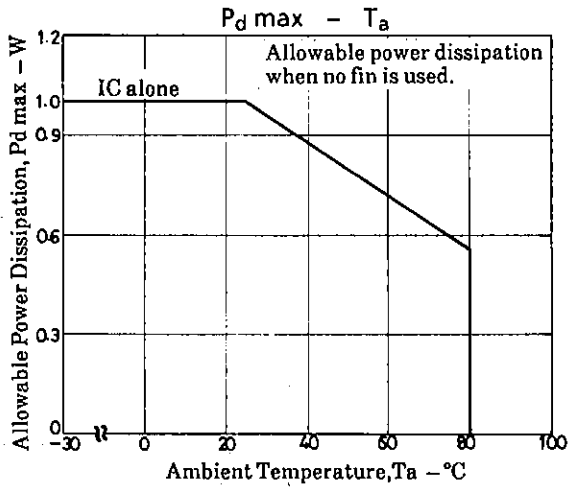
Since the leakage current at the output pin (pin5) of the L78LR05 is so low as 2μA or less, a backup circuit can be implemented by connecting an electric double layer capacitor (super capacitor: NEC, gold capacitor: Matsushita Electric) or a Ni Cd battery direct to the output pin. Since a reverse blocking diode, which has been so far connected to the output pin, is not required, a regulated power-supply voltage can be supplied to a load during the steady-state operation, without voltage drop caused by the diode and effects of temperature characteristics, current characteristics of the diode. No battery-regulator switching circuit is required at the battery backup start mode.

Note 3: The capacitance of reset output signal delay capacitor C_d must exceed that of input capacitor C_{in} . If the capacitance of C_d is small, a reset pulse signal may be generated once when the main power source is turned off (at the battery backup start mode).

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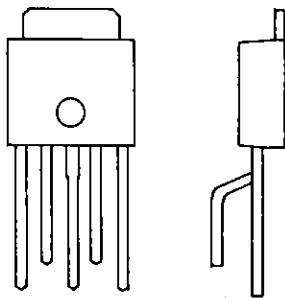
Allowable Power Dissipation

The allowable power dissipation is 1.0W ($T_a=25^\circ\text{C}$) with no fin attached. When the L78LR05 is surface-mounted on a hybrid IC board or printed circuit board, a high allowable power dissipation can be obtained, though it is placed in a small-sized package. Shown below is the relationship between the Cu-foiled area and the allowable power dissipation when the L78LR05 is surface-mounted on a glass epoxy board ($50\times 50\times 0.8\text{mm}^3$).

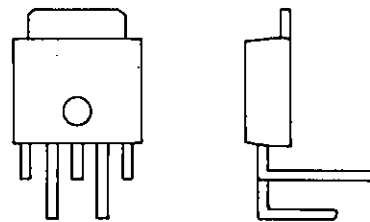


* The measured values of P_d represent the values measured when solder on the Cu-foiled area is all wet.

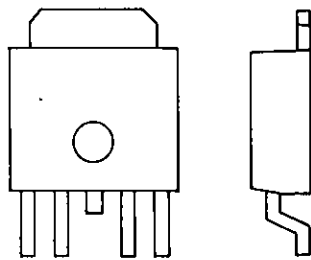
Lead Formings



MA forming

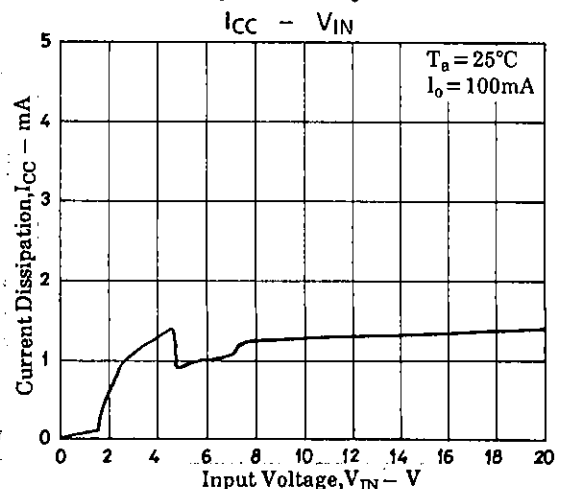
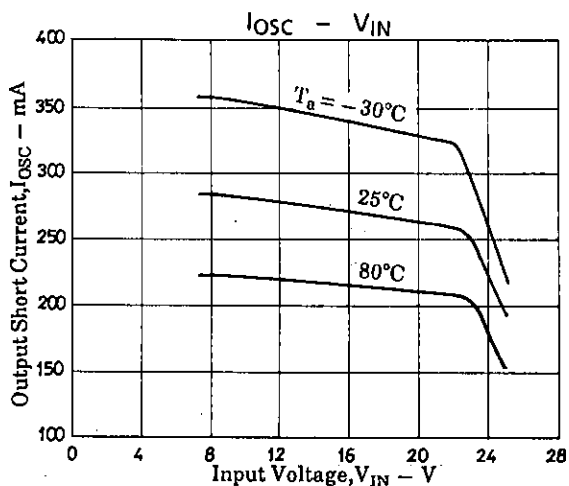
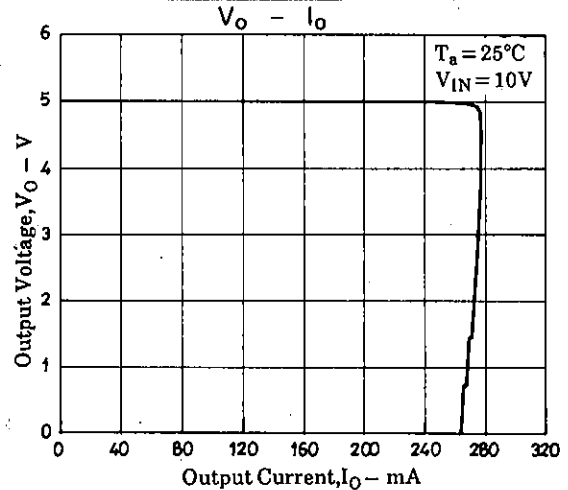
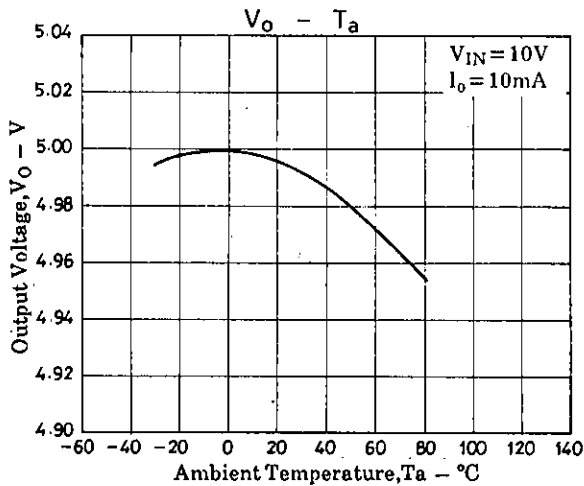
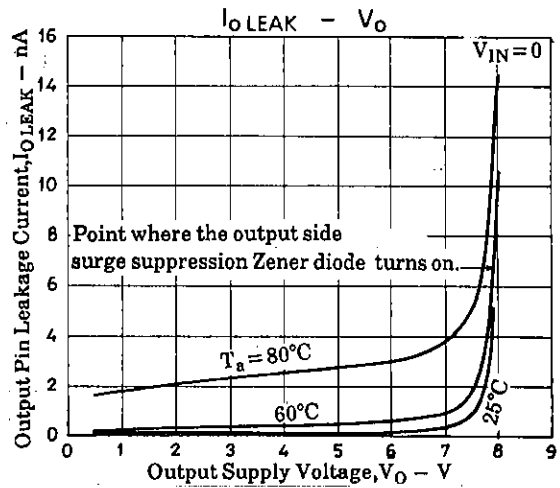
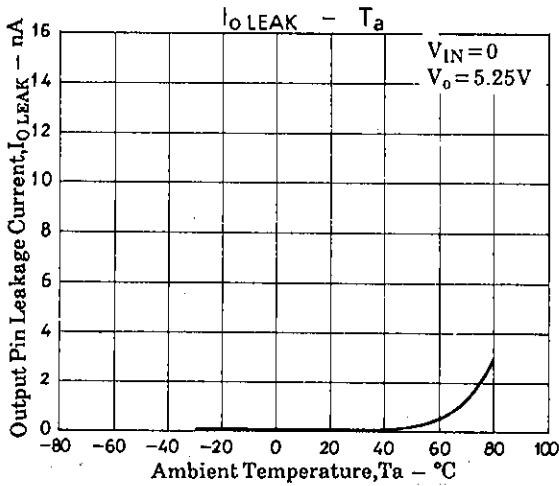
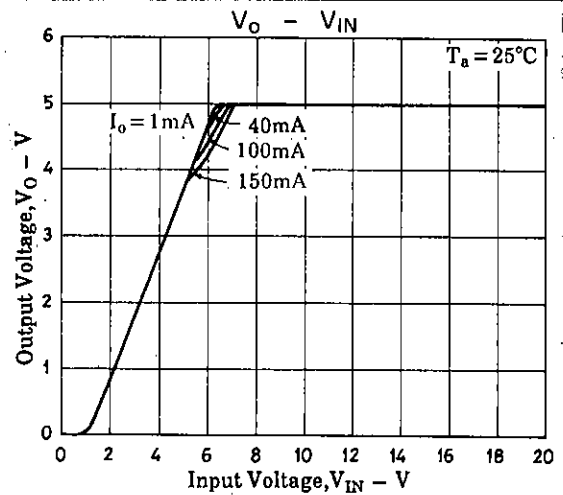
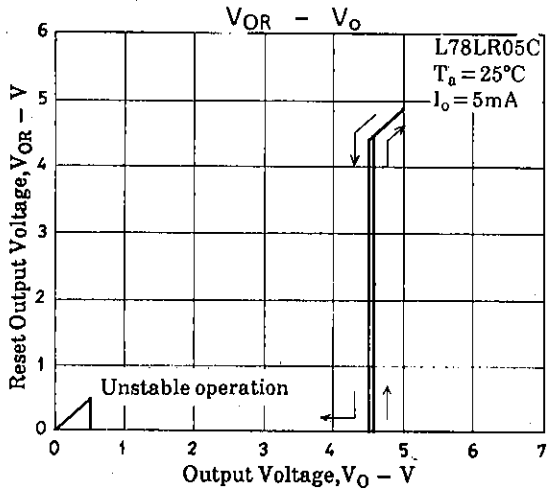


LR forming

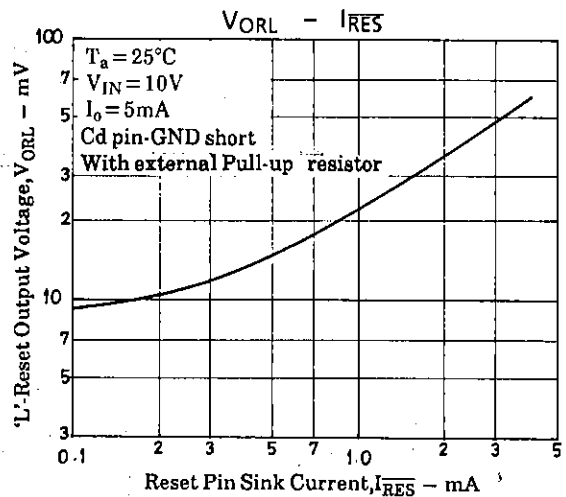
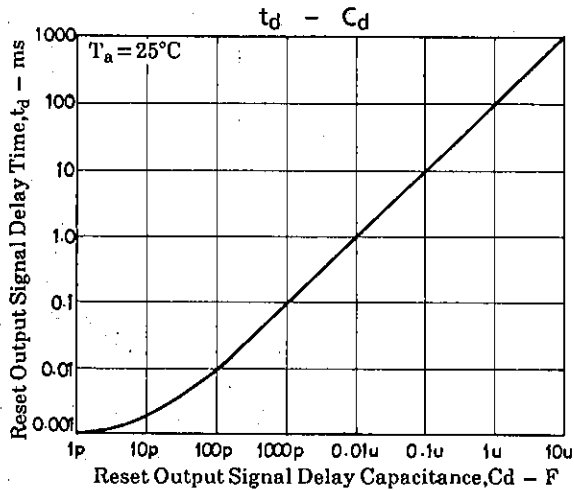
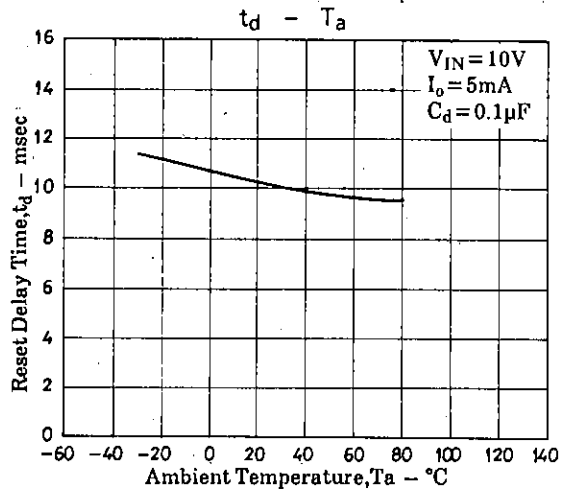
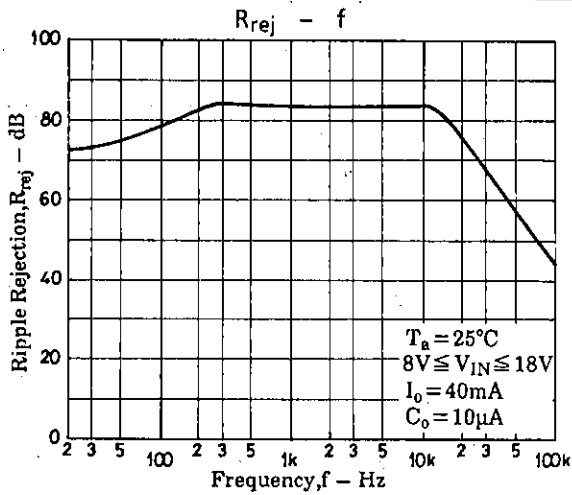


FA forming

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