Ordering number: EN※4604A

CMOS LSI

No.※4604A

LC8211

Halftone Processing IC for Fax,Copier and Scanner

Preliminary

Overview

The LC8211 inputs the multi-level image data output from the LC8210 (multi-level image processing IC), and performs a process to create high quality binary image data. The LC8211 can be applied to OA equipments such as G3 and G4 facsimiles, image file systems, digital photocopiers and image scanners. The multi-level data is segmented into areas of character, photographs and screened halftone areas, and performs binary coding using various advanced processing methods.

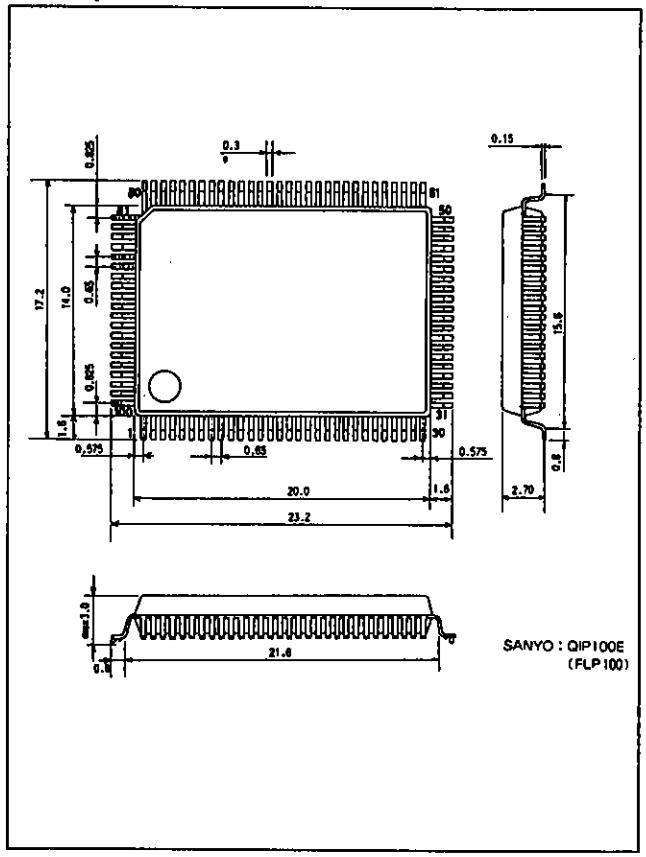
Features

- No. of processed pixels 8192pixels/line max. The number of pixels can be set in pixel units.
- Processing speed : 200ns/pixel max
- Document segmentation (characters, photographs, screened halftone areas)
- Simple binary coding process (fixed threshold, density adaptive threshold)
- Simulated halftone process
  Structural dither method (64-tone) Dither threshold value can be set.
  Error diffusion method (64-tone)
- Image reduction Image data compression, black fine line retention, white fine line retention
- Single 5V power supply and low power consumption using CMOS

Package Dimensions

(unit : mm)

3151-QIP100E



Specifications

Absolute maximum ratings at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		– 0.3 to + 7.0	V
Input/output voltage	V_I, V_O		– 0.3 to V_{DD} + 0.3	V
Operation ambient temperature	Topr		– 30 to + 70	°C
Storage ambient temperature	Tstg		– 55 to + 125	°C
Soldering heat resistance		10s	235	°C

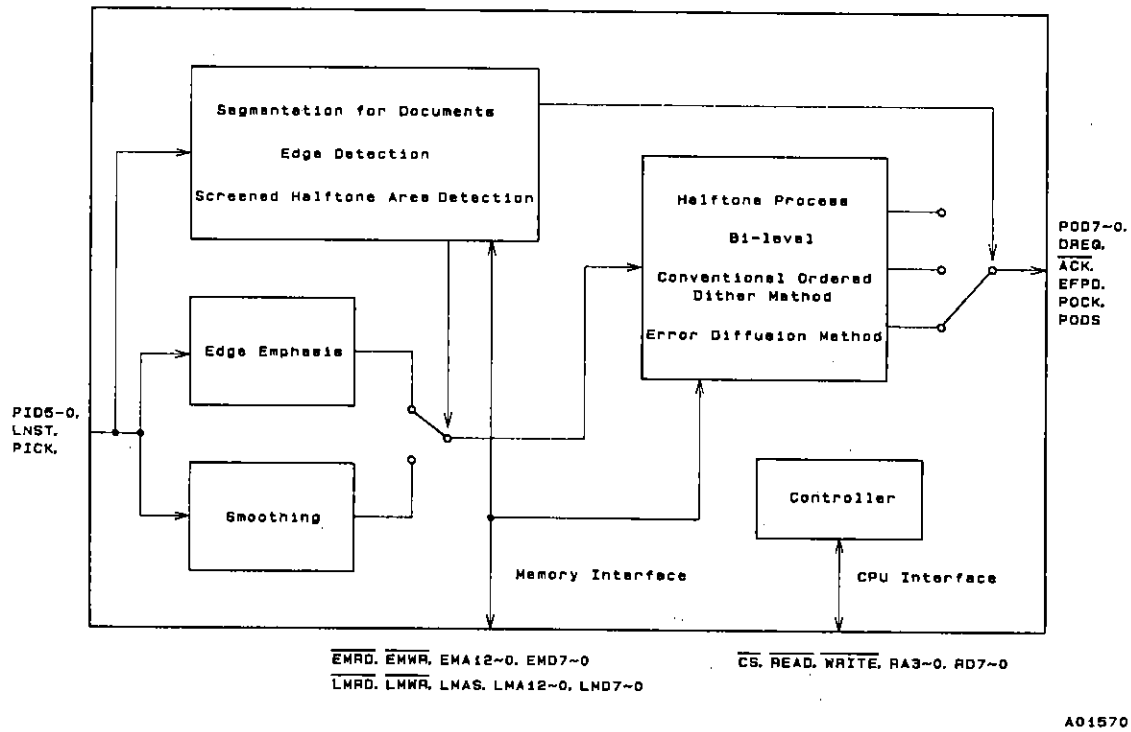
Allowable Operating Ranges at Ta = −30 to +70°C, GND = 0V

Parameter	Symbol	Ratings			Unit
		min	typ	max	
Power voltage	V_{DD}	4.5		5.5	V
Input voltage	V_{IN}	0		V_{DD}	V

DC Characteristics at Ta = −30 to +70°C, GND = 0V, V_{DD} = 4.5 to 5.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	V_{IH}		2.2			V
Input low level voltage	V_{IL}				0.8	V
Output high level voltage	V_{OH}	I_{OH} = −3mA	2.4			V
Output low level voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Current consumption	I_{DD}	V_{DD} = 5.0V SYSCLK = 20MHz		15	23	mA

Block Diagram



Pin Functions

Type					
I	Input pin	B	Bidirectional pin	NC	Not connected
O	Output pin	P	Power pin		

Pin No.	Pin name	Type	Function
99	RD0	B	The CPU interface data bus terminal. RD7 is the MSB terminal, and RD0 is the LSB terminal.
100	RD1	B	
1	RD2	B	
2	RD3	B	
3	RD4	B	
4	RD5	B	
5	RD6	B	
6	RD7	B	
7	RA0	I	The CPU interface address bus terminal. RD3 is the MSB terminal, and RA0 is the LSB terminal.
8	RA1	I	
9	RA2	I	
10	RA3	I	
11	$\overline{CS}$	I	CPU interface chip select signal terminal
12	$\overline{READ}$	I	CPU interface READ signal terminal
13	$\overline{WRITE}$	I	CPU interface WRITE signal terminal
14	$\overline{RESET}$	I	System reset terminal
15	GND	P	Ground terminal
16	VDD	P	Power terminal
17	LMD0	B	Line memory data bus terminal. LMD7 is the MSB terminal, and LMD0 is the LSB terminal.
18	LMD1	B	
19	LMD2	B	
20	LMD3	B	
21	LMD4	B	
22	LMD5	B	
23	LMD6	B	
24	LMD7	B	
25	GND	P	ground terminal

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Pin No.	Pin name	Type	Function
26	LMA0	O	Line memory address bus terminal LMA12 is the MSB terminal, and LMA0 is the LSB terminal.
27	LMA1	O	
28	LMA2	O	
29	LMA3	O	
30	LMA4	O	
31	LMA5	O	
32	LMA6	O	
33	LMA7	O	
34	LMA8	O	
35	LMA9	O	
36	LMA10	O	
37	LMA11	O	
38	LMA12	O	
39	LMAS	O	Line memory line identification terminal
40	GND	P	Ground terminal
41	VDD	P	Power terminal
42	$\overline{\text{LMRD}}$	O	Line memory READ terminal
43	$\overline{\text{LMWR}}$	O	Line memory WRITE terminal
44	EMD0	B	Error diffusion memory data bus terminal EMD7 is the MSB terminal, and EMD0 is the LSB terminal.
45	EMD1	B	
46	EMD2	B	
47	EMD3	B	
48	EMD4	B	
49	EMD5	B	
50	EMD6	B	
51	EMD7	B	
52	GND	P	Ground terminal
53	EMA0	O	Error diffusion memory address bus terminal EMA12 is the MSB terminal, and EMA0 is the LSB terminal.
54	EMA1	O	
55	EMA2	O	
56	EMA3	O	
57	EMA4	O	
58	EMA5	O	
59	EMA6	O	
60	EMA7	O	
61	EMA8	O	

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Pin No.	Pin name	Type	Function
62	EMA9	O	Error diffusion memory address bus terminal EMA12 is the MSB terminal, and EMA0 is the LSB terminal.
63	EMA10	O	
64	EMA11	O	
65	EMA12	O	
66	VDD	P	Power terminal
67	GND	P	Ground terminal
68	$\overline{\text{EMRD}}$	O	Error diffusion memory READ signal terminal
69	$\overline{\text{EMWR}}$	O	Error diffusion memory WRITE signal terminal
70	PID0	I	Multi-level image data input terminal PID5 is the MSB terminal, and PID0 is the LSB terminal.
71	PID1	I	
72	PID2	I	
73	PID3	I	
74	PID4	I	
75	PID5	I	
76	PICK	I	Multi-level image data transfer clock
77	LNST	I	Multi-level image line synchronous signal
78	POD0	O	Binary image data parallel data bus POD7 is the new data, and POD0 is the old data.
79	POD1	O	
80	POD2	O	
81	POD3	O	
82	POD4	O	
83	POD5	O	
84	POD6	O	
85	POD7	O	
86	POD5	O	Binary image data serial data bus
87	POCK	O	Binary image data serial transfer clock
88	EFPD	O	Binary image data output valid period signal
89	VDD	P	Power terminal
90	GND	P	Ground terminal
91	DREQ	O	DMA data request signal
92	$\overline{\text{ACK}}$	I	DMA acknowledge input
93	CLKIN	I	System clock
94	MTP	O	Motor drive timing signal
95	NC	NC	
96	NC	NC	
97	TEST	I	Test terminal (normal grounding)
98	GND	P	Ground terminal

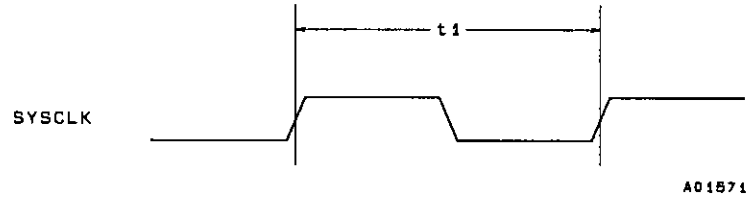
AC Characteristics

When GND=0V, V_{DD}=4.5 to 5.5V, Ta=−30 to +70°C, C_L=50pF and high level voltage is 2.2V and low level voltage is 0.8V.

Input Clock

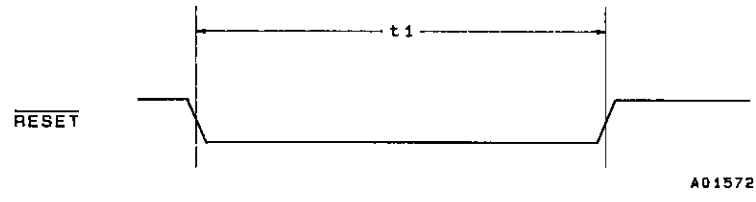
Parameter	Symbol	Ratings			Unit
		min	typ	max	
Cycle time of input signal SYSCLK	t1	50			ns

Note : The clock duty must be set to 50%.



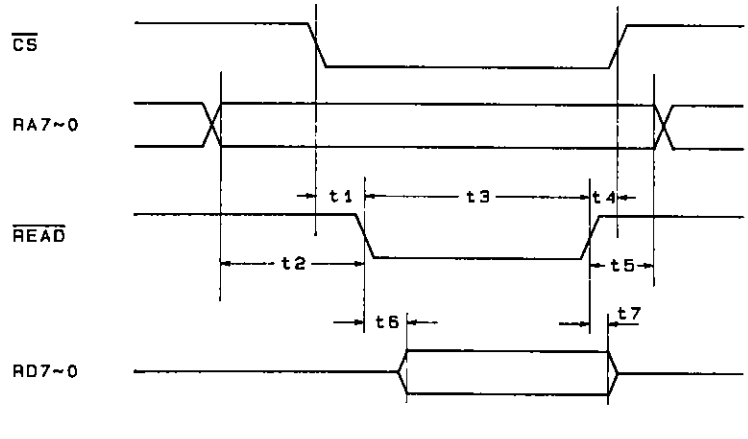
Reset

Parameter	Symbol	Ratings			Unit
		min	typ	max	
Downward pulse width of input signal $\overline{RESET}$	t1	500			ns



CPU Interface (READ)

Parameter	Symbol	Ratings			Unit
		min	typ	max	
For $\overline{READ}$ ↓, $\overline{CS}$ setup time	t1	20			ns
For $\overline{READ}$ ↓, RA7 to 0 setup time	t2	20			ns
$\overline{READ}$ pulse width	t3	50			ns
For $\overline{READ}$ ↑, $\overline{CS}$ hold time	t4	20			ns
For $\overline{READ}$ ↑, RA7 to 0 hold time	t5	20			ns
For $\overline{READ}$ ↓, RD7 to 0 delay time	t6			40	ns
For $\overline{READ}$ ↑, RD7 to 0 delay time	t7	0		20	ns



CPU Interface (WRITE)

Parameter	Symbol	Ratings			Unit
		min	typ	max	
For WRITE ↓, CS setup time	t1	20			ns
For WRITE ↓, RA7 to 0 setup time	t2	20			ns
WRITE pulse width	t3	50			ns
For WRITE ↑, CS hold time	t4	20			ns
For WRITE ↑, RA7 to 0 hold time	t5	20			ns
For WRITE ↑, RD7 to 0 setup time	t6	20			ns
For WRITE ↑, RD7 to 0 hold time	t7	10			ns